ARCADIA FD-MAPS: simulation, characterization and perspectives for high resolution timing applications

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on behalf of the ARCADIA collaboration

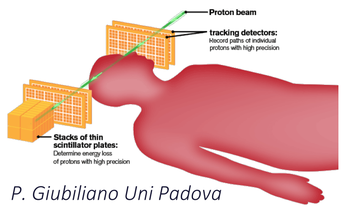
ARCADIA

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

Goals and status of the ARCADIA project

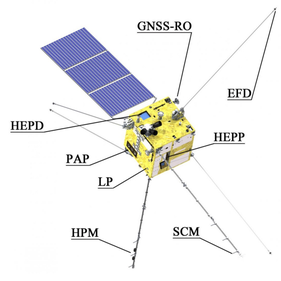
Main objective
Development of large (1.2×1.2)cm^2 demonstrator chip of 512×512 fully depleted monolithic pixels with 25µm pitch.

Targeted applications
- future high energy experiments
- space applications
- medical and industrial scanners



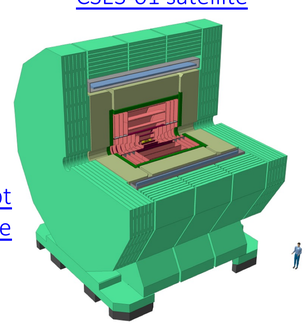
P. Giubiliano Uni Padova

Specifications
- low power consumption 5-20mW/cm^2
- hit rates up to 10-100MHz/cm^2
- scalable matrix size up to 24cm^2
- radiation tolerance 10-100krad / 10^{11}-10^{12} neq/cm^2
- full signal processing within 1-10µs



CSES-01 satellite

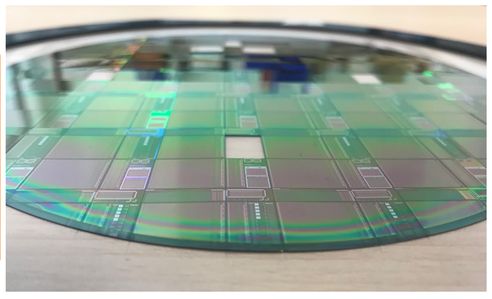
CLD detector concept for FCC-ee



Timeline & Production

		wafers	d_{Si} [µm]
1st run delivered	June 2021	12	50/100/200
2nd run delivered	March 2022	11	50/100
3rd run – final layout	June 2022	12	50/../200
3rd run predicted arrival	end 2022		

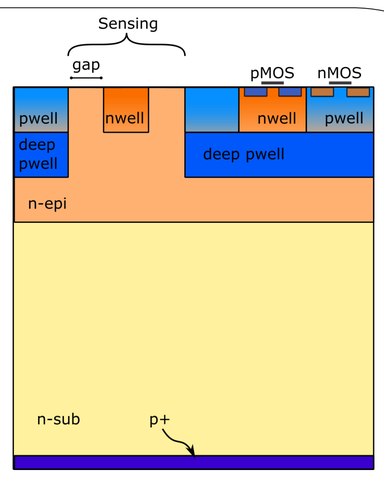
ARCADIA 1st run 8'' wafer



ARCADIA sensor concept

- Fully depleted substrate with low front bias → charge collection via drift
- n-in-n device
- pn-junction on backside
- depletion voltage applied through backside, only low bias voltage from top
- low-resistive epi layer delays the onset punch-through currents
- backside processing (diode + GR) for thick sensors (> 100µm)

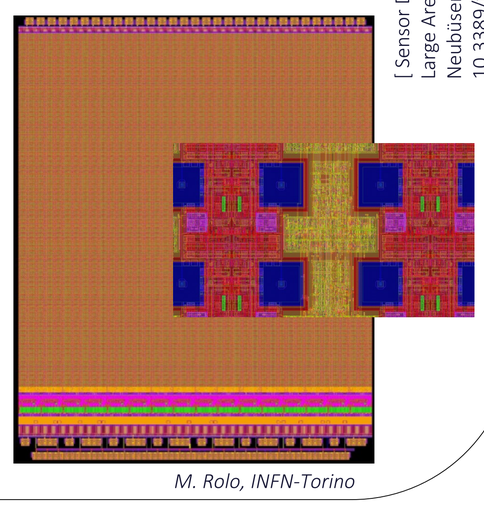
Concept first realized in SEED project



[Sensor Design Optimization of Innovative Low-Power, Large Area FD-MAPS for HEP and Applied Science, C. Neubüser et al. Front. Phys. 9:625401. doi: 10.3389/fphy.2021.625401]

Main Demonstrator (MD) chip

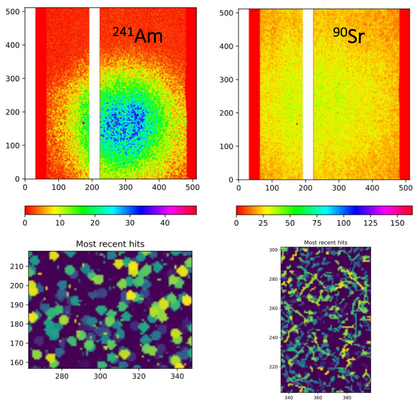
- matrix core 512×512 pixels of 25µm pitch
- pixels are ~(50/50)% analogue/digital
- 2 types of front-ends
- sensor diode about 20% of total area
- clock-less matrix (to minimize power dissipation)
- global shutter with serial readout
- output fully digital

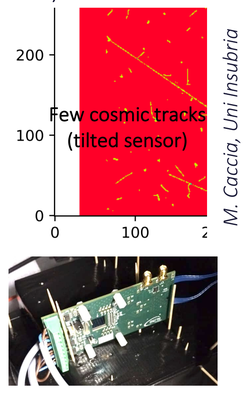


M. Rolo, INFN-Torino

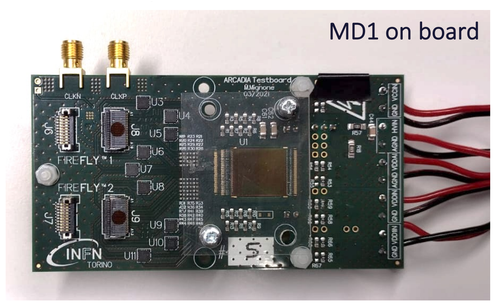
Results of 1st Engineering run

Main Demonstrator functional
- DAQ up and running
- Debugging ongoing (sources of additional leakage currents found and eliminated)
- first tests of a MD1 (200µm thickness) with sources and cosmic rays





M. Caccia, Uni Insubria

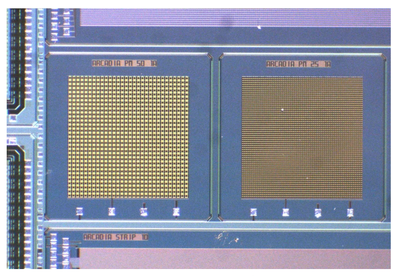


- Further tests with more chips **ongoing**

Variety of passive pixel matrices
- Tests of pixels with (10/25/50)µm pitch from different wafers in different thicknesses
- Tests with different designs of pixels of same pitch
- Radiation study with X-rays from 10krad to 10Mrad

→ *results will be presented at iWORID 2022*

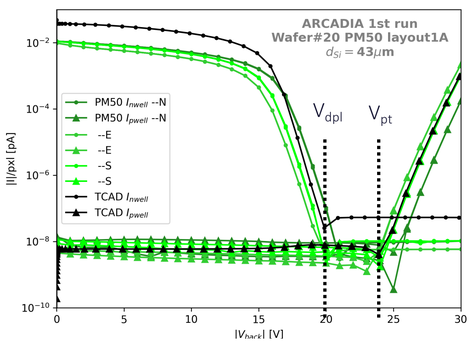
Microscopic picture of two 1×1mm^2 passive matrices with pixels of 50 and 25µm pitch



T. Corradino, Uni Trento

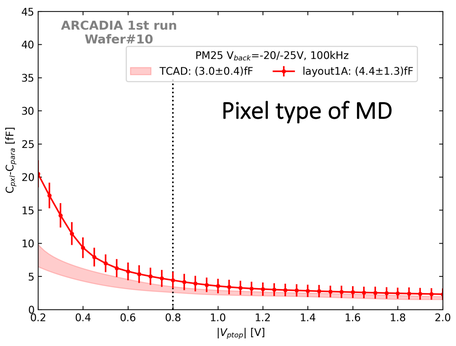
Matching of TCAD simulations

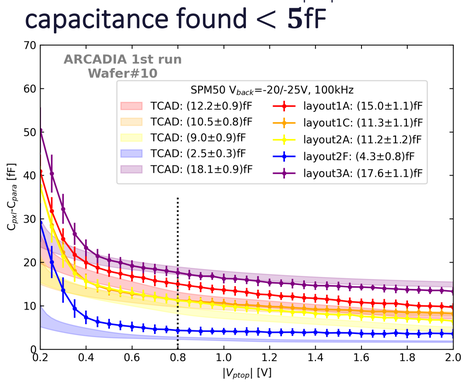
- IV/CV measurements from 4 positions of each wafer
- TCAD input parameters (substrate doping, epi-layer thickness, total thickness) varied within uncertainty given by foundry
- Found excellent agreement with the IV measurements, and depletion V_{dpl} and punch-though voltages V_{pt}
- Parameters matched for each wafer type individually



Capacitance measurements

- Depletion voltage varied from -20 to -25V
- At operating point of V_{ptop} =0.8V the **single pixel capacitance found < 5fF**

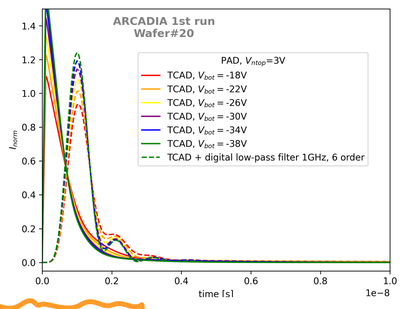




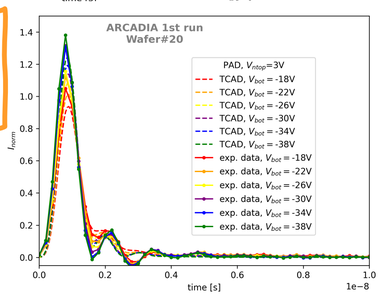
- Tested different pixel geometries, optimised in simulation for low capacitance or fast charge collection
- Trends found in simulation (including oxide charges), confirmed in data
- 50µm pixel with < 5fF

TCT measurements

Focused IR laser, 1GHz bandwidth oscilloscope on $(500\times500)\mu m^2$ pad
- Strong impact of 1GHz oscilloscope, which can be well reproduced in simulation with digital low pass filter
- TCAD simulation based on matched parameters per wafer

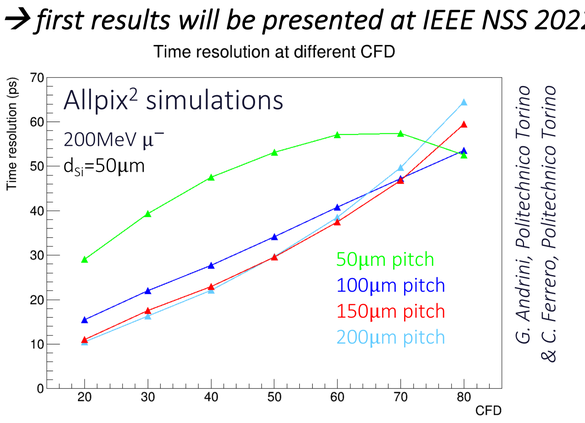


95% charge collection in:
- < 1.4ns in d_{Si}=50µm
- < 5ns in d_{Si}=100µm



- Pad-like MAPs in 50µm pitch for chip optimised for timing implemented in 2nd run

→ *first results will be presented at IEEE NSS 2022*



G. Andrini, Politechnico Torino & C. Ferrero, Politechnico Torino

Intrinsic timing resolution in Allpix^2 simulations for MIPs
- < 20ps for constrant fractions < 40% for pixel pitches > 100µm in d_{Si}=50µm

Summary

- Successful 2 production runs, w/ and w/o backside processing in n-type and p-type (with 50µm n-type epitaxial substrate) wafers
- Passive pixel matrices used for characterization of different pixel layouts, and to study impact of oxide charges
- Successful reproduction of operating voltages in TCAD within the process uncertainties
- Single pixel capacitances of MD1 (25µm pitch) < 5fF
- First particles seen by MD1
- Design of specialized timing chip completed, integrating pad-like pixels with expected 95% charge collection in 1.4ns

Outlook and plans – 3rd run

- Design of new test-structures ongoing: gated diodes on front side for oxide charge concentration measurements, diodes for epi-layer doping profiles, and ***new large pixels including a charge multiplication layer***

Acknowledgments

The research activity presented has been carried out in the framework of the ARCADIA experiment funded by the Istituto Nazionale di Fisica Nucleare (INFN), CSN5. Additionally, the author would like to thank T. Corradino and H. M. Postlethwaite, who have performed most of the measurements presented.