ARCADIA FD-MAPS: simulation, characterization and perspectives for high resolution timing applications

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on behalf of the ARCADIA collaboration

Goals and status of the ARCADIA project

Main objective
Development of large (1.2 x 1.2)cm² demonstrator chip of 512 x 512 fully depleted monolithic pixels with 25µm pitch.

Targeted applications
• future high energy experiments
• space applications
• medical and industrial scanners

Specifications
• low power consumption 5-20mW/cm²
• hit rates up to 10-100kHz/cm²
• scalable matrix size up to 24cm²
• radiation tolerance 10-100krad / 10¹¹-10¹² ng/cm²
• full signal processing within 1.5ns

Timeline & Production

<table>
<thead>
<tr>
<th>Step</th>
<th>Date</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st run delivered</td>
<td>June 2021</td>
<td>wafers dF [μm] 12, 50/100/200</td>
</tr>
<tr>
<td>2nd run delivered</td>
<td>March 2022</td>
<td>11, 50/100</td>
</tr>
<tr>
<td>3rd run – final layout</td>
<td>June 2022</td>
<td>12, 50/…/200</td>
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<tr>
<td>3rd run predelivered</td>
<td>end 2022</td>
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ARCADIA sensor concept

- Fully depleted substrate with low front bias
- Charge collection via drift
- np junction on backside
- Depletion voltage applied through backside, only low bias voltage from top
- Low-resistive epi layer delays the onset punch-through currents
- Backside processing (diode + GR) for thick sensors (> 100µm)

Concept first realized in SEED project

Main Demonstrator (MD) chip

- matrix core 512 x 512 pixels of 25µm pitch
- pixels are ~50/50 analogue/digital
- 2 types of front ends
- sensor diode about 20% of total area
- clock-less matrix (to minimize power dissipation)
- global shutter with serial readout
- output fully digital

Results of 1st Engineering run

Main Demonstrator functional
- DAQ up and running
- Debugging ongoing (sources of additional leakage currents found and eliminated)
- first tests of a MD1 (200µm thickness) with sources and cosmic rays

Further tests with more chips ongoing

Variety of passive pixel matrices
- Tests of pixels with (10/25/50)µm pitch from different wafers in different thicknesses
- Tests with different designs of pixels of same pitch
- Radiation study with X-rays from 10krad to 100krad

Results will be presented at iWORID 2022

TCT measurements

Focused IR laser, 1GHz bandwidth oscilloscope on (50x) 500µm pad
- Strong impact of 1GHz oscilloscope, which can be well reproduced in simulation with digital low pass filter
- TCAD simulation based on matched parameters per wafer

Pad-like MAPs in 50µm pitch for chip optimised for timing implemented in 2nd run

First results will be presented at IEEE NSS 2022

Summary

- Successful 2 production runs, w/ and w/o backside processing in n-type and p-type (with 50µm n-type epitaxial substrate) wafers
- Passive pixel matrices used for characterization of different pixel layouts, and to study impact of oxide charges
- Successful reproduction of operating voltages in TCAD within the process uncertainties
- Single pixel capacitances of MD1 (25µm pitch) < 5fF
- First particles seen by MD1
- Design of specialized timing chip completed, integrating pad-like pixels with expected 95% charge collection in 1.4ns

Outlook and plans – 3rd run

- Design of new test-structures ongoing: gated diodes on front side for oxide charge concentration measurements, diodes for epi-layer doping profiles, and new large pixels including a charge multiplication layer

Acknowledgments

The research activity presented has been carried out in the framework of the ARCADIA experiment funded by the Istituto Nazionale di Fisica Nucleare (INFN), CSEnte. Additionally, the author would like to thank T. Corradino and H. M. Postlethwaite, who have performed most of the measurements presented.