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Timespot1: an ASIC for high-resolution timing and high-rates in 28-nm CMOS technology

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Trackers in high-energy experiment of the next generation must cope with unprecedented high rates and track densities. This poses the need for timing information at the pixel level, high readout frequency and radiation hardness. 28-nm CMOS technology appears having the whole set of characteristics to satisfy such experimental requirements.

Within the TimeSPOT project, we have developed a complete 28-nm CMOS ASIC to elaborate technical solutions about the challenging issues of such complex future detectors.

The ASIC, named Timespot1, features a 32x32 channels hybrid-pixel matrix and integrates one analogue front-end, one discriminator and one high-resolution time-to-digital converter per pixel. The system aims to achieve a timing resolution of 30 ps or better at a maximum event rate of 3MHz per channel with a Data-Driven interface. Power consumption can be programmed to range between 1.2W/cm2 and 2.6 W/cm2. The present paper illustrates the experience and the results gained in the design and tests of the ASIC. Future possible developments are also addressed.

Collaboration

TimeSPOT Collaboration

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