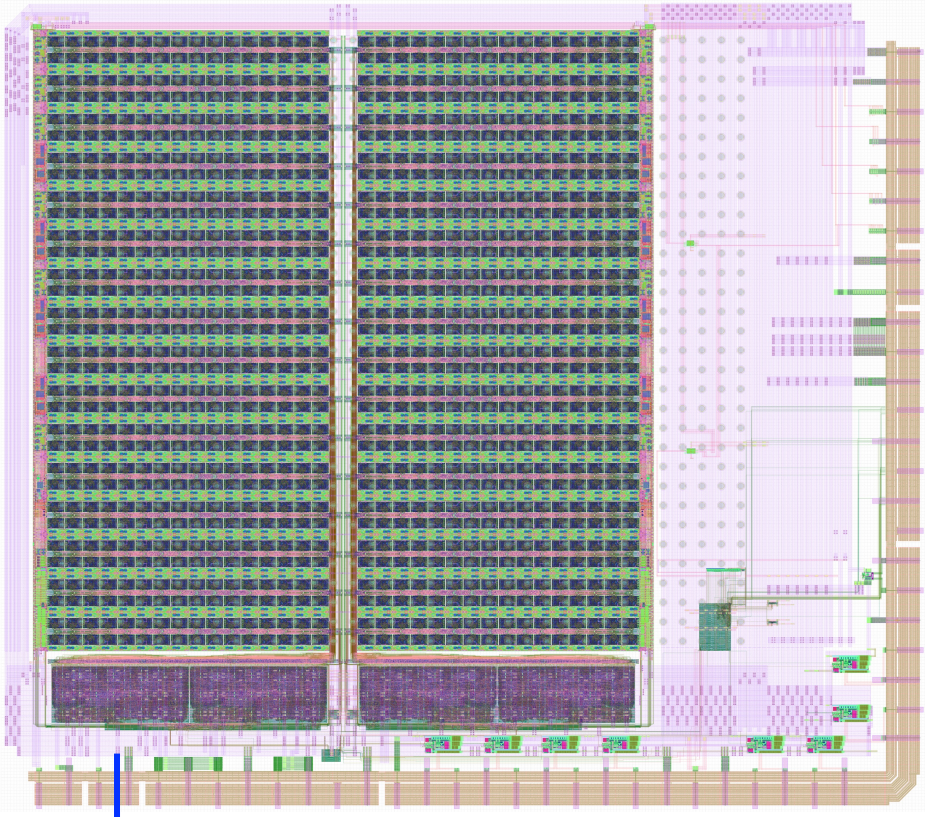
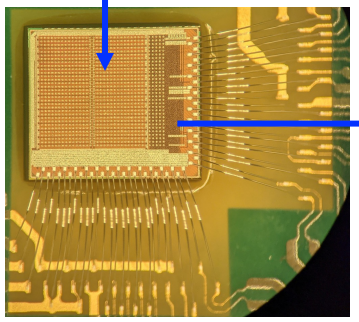
Timespot1: an ASIC for high-resolution timing and high rates in 28-nm CMOS technology





Bonded Timespot1 ASIC

TS1-PCB 120x80 mm^2

Reduced size (32x32 = 1024 pixels, total area 6 mm^2),
Complete set of functionalities for pixel readout with timing
Max sustainable rate 3 MHz/pixel (1 TDC per pixel)
(1.8 x 1.8) mm^2 sensitive area. 50 µm pixel pitch (in y direction)
3-side abuttable matrix (xy pitch on sensor side is 55 µm)

- **640 MHz master clock**
- **Digital row: 16x2 TDC each** + Controls, Conf. registers, I^{2}C I/F
- **Analog row (16x2 AFE each)**
- **Analog (service) column. Each contains:** 1 Band-Gap circuit, 5x Σ–Δ DACs (producing analog levels used by pixels), Programmable bias cell (for power consumption), bias replicas with source followers.
- **8x LVDS driver** (each @1.28 Gbps)

Results on timing performace (time resolution σ_{TA})

- **TDC: $\sigma_{TA} \approx 20$ ps, in average**, with a relatively wide dispersion across the channels of the ASIC (around 5 ps rms)
- TDC simulated $\sigma_{TA} < 10$ ps. Worsened timing performance and dispersion due to the master clock jitter inside the pixel matrix. More accurate clock distribution is needed.
- **AFE: $\sigma_{TA} \approx 40$ ps, in average**. However, this value is limited by the performance of the TDC, which bias the estimate of the AFE resolution towards higher values.
- Identified bug on the Offset Compensation mechanism, which prevent the setting of the discriminator threshold towards nominal low values. The intrinsic AFE performance appears below 20 ps. The bug is easily recoverable by design.
- The next version of the ASIC is in preparation