H2GCROC: Design and Performance of a Dedicated Very Front-End ASIC for SiPM readout of the CMS High Granularity Calorimeter.

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Abstract

The H2GCROC ASICs are dedicated very front-end electronics designed to readout the High Granularity Calorimeter (HGCAL), which will replace the present end-cap calorimeters of the Large Hadron Collider (LHC) for the Compact Muon Solenoid collaboration (CMS). The H2GCROC ASIC was especially designed to readout the SiPMs coupled to the scintillating tiles of the back hadronic sections, where the radiation constraints are less severe. Inside the chip, the front-end preamplifier is adapted for the SiPM’s higher signal level, excepting pC/MIP range. The chip was received end of 2020 and extensively tested since then, in the lab and test beam. This work examines the very front-end design and performance, including timing performance with the sensor.

H2GCROC Architecture

- Radiation-hardened TSMC 130nm CMOS chip.
- 72 reading out standard cells, 2 channels for MIP calibration, and 4 channels not connected for common-mode noise elimination.
- DAC path. Circular buffer RAM, store ADC, ToT and ToA data.
- Trigger path. Sum of 4(9) channels, linearization, compression over 7 bits.
- DAC protocol for slow control.
- Fast commands. 320 MHz clock and 40 MHz extracted.
- The Current Converter applies a reduction in the current before the input preamplifier; its design is based on the input stage of the KLa2 chip from Heidelberg University.
- The CC shows good linearity over the full range of attenuation.
- Leakage compensation and calibration. The CC has a tuning DC voltage at the input to compensate for breakdown voltage fluctuations on SiPMs due to temperature changes and production tolerances.
- The VCC can be tuned in a small range to adjust the sensor gain and compensate between the channels.
- At the CC input, a calibration circuit can be used for internal or external injection on the ASIC.
- The internal injection uses a 12bit DAC going from 0 to 2.5 V and converting the signal into charge with two selectable capacitances (3 pf for low range and 120 pf for high range).
- C1 can be configured with 3 bits from 0 to 35 pC to add a capacitance that improves the linearity of ToT.
- The current injected by Ileakage (Ileak) is automatically compensated by Ie.
- Leakage currents (Ileak), produced by radiation, are expected to be up to 1mA.
- A 6bit DAC (delta) can inject a current with a configuration variable of 2 bits to adapt the dynamic range to compensate Ileakage as on the table.
- 32 reading out standard cells, 2 channels for MIP calibration, and 4 channels not connected for common-mode noise elimination.
- DAC path. Circular buffer RAM, store ADC, ToT and ToA data.
- Trigger path. Sum of 4(9) channels, linearization, compression over 7 bits.
- DAC protocol for slow control.
- Fast commands. 320 MHz clock and 40 MHz extracted.
- Amplification. The preamplifier gain output duration can be adapted to the MIP signal.
- The default configuration is good for single-photon measurement and for calibration.
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- Charge measurement. The ADC measure the charge in the linear part of the PA.
- While ToT triggers, ADCm has the full data of the charge (next bunch crossing).
- ADC linearity of 99.7% from 160 pC to 20 pC range with Physics configuration.
- Time measurement. The ToA time walk of 16 ns from 0 to 20 pC charge injection.
- Noise of 40 ps measured for small charge injection.
- Noise of 20 ps at 40 pC charge injection and up to 320 pC (full range).
- The two discriminators can be calibrated with two external trigger inputs available.
- Diaphragm and absorptive lenses to reduce the light injection to the SiPM.
- MIP signal injected equal to 15 p.e. (555 fC) using the default configuration of PA gain and minimum attenuation of CC gain.
- Single-photon pixels measured with default configuration and phase 13 selected.