Contribution ID: **194** Type: **Poster**

High resolution filtering and digitization system for cryogenic bolometric detectors

Friday, 27 May 2022 15:54 (1 minute)

Next-generation cryogenic bolometric detectors, like those used for the CUPID and CROSS experiments for the search of neutrinoless double beta decay, will also identify the type of the interacting particle by measuring the amount of scintillation light produced in the crystals. Light signals are characterized by a faster response with respect to heat signals and will thus require different characteristics of the readout electronics. The signal filtering and digitization for these experiments will be based on a custom solution comprised of several analog-to-digital boards interfaced to Altera Cyclone V SoC FPGA modules installed on the backplane of the DAQ crates. Each analog-to-digital board hosts 12 channels that allow signal digitization up to 25 ksps per channel and an effective resolution of 21 bits at 5 ksps. The anti-aliasing filter cut-off frequency can be digitally adjusted with 10 bits of resolution from 24 Hz to 2.5 kHz and thus adapted to a wide range of detectors. The SoC FPGA modules control all the acquisition parameters through a Python-based server, and are responsible for the synchronization of the analog-to-digital boards and for the data transfer to the storage, using the RTP protocol on a standard Ethernet interface. Each FPGA module manages the data coming from 8 boards, offering excellent scalability. In this contribution, we will present an overview of the new filtering and digitization system, a detailed characterization of its performance, and the results of the first tests with real detectors during CUPID and CROSS test runs.

Collaboration

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Session Classification: Front End, Trigger, DAQ and Data Mangement - Poster session