High resolution filtering and digitization system for cryogenic bolometric detectors

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Next generation 0υ2β bolometric experiments

Next generation experiments for the search of neutrinoless double beta decay (0υ2β), like **CUPID** or **CROSS**, will greatly improve their sensitivity by introducing **particle identification techniques** to reject α background in the region of interest.
The most promising technique is the detection of **scintillation light** by coupling a scintillating crystal containing the 0υ2β candidate to a Ge or Si light-to-phonon detector, thus read out with the same bolometric technique as the crystal.
The lower amount of light produced by α particles with respect to β/γ allows them to be identified and rejected.
Other improvements will consist in the adoption of **high Q-value** 0υ2β candidates, like ^{100}Mo (Q ~ 3 MeV), the use of **enriched crystals**, higher active mass, and others.

New challenges on the readout

Light signals will have rise time **below 1 ms**, much faster than heat signals in the main crystal. In addition to that, ^{100}Mo has a **high pile-up rate** due to 2υ2β background.
This will pose new challenges on the readout:

- **Higher bandwidth:** the spread in the detector characteristics requires adjustable analog cut-off frequencies, up to 2 kHz, and sampling rates, up to 10 ksps.
- **Higher resolution:** the adoption of light detectors, which have lower baseline noise, and a quieter cryogenic setup will require a readout with lower noise and higher resolution.
- **Lower power and space:** channels will triplicate from previous experiments, so power and space must be reduced.

Low pass filter and digitization board

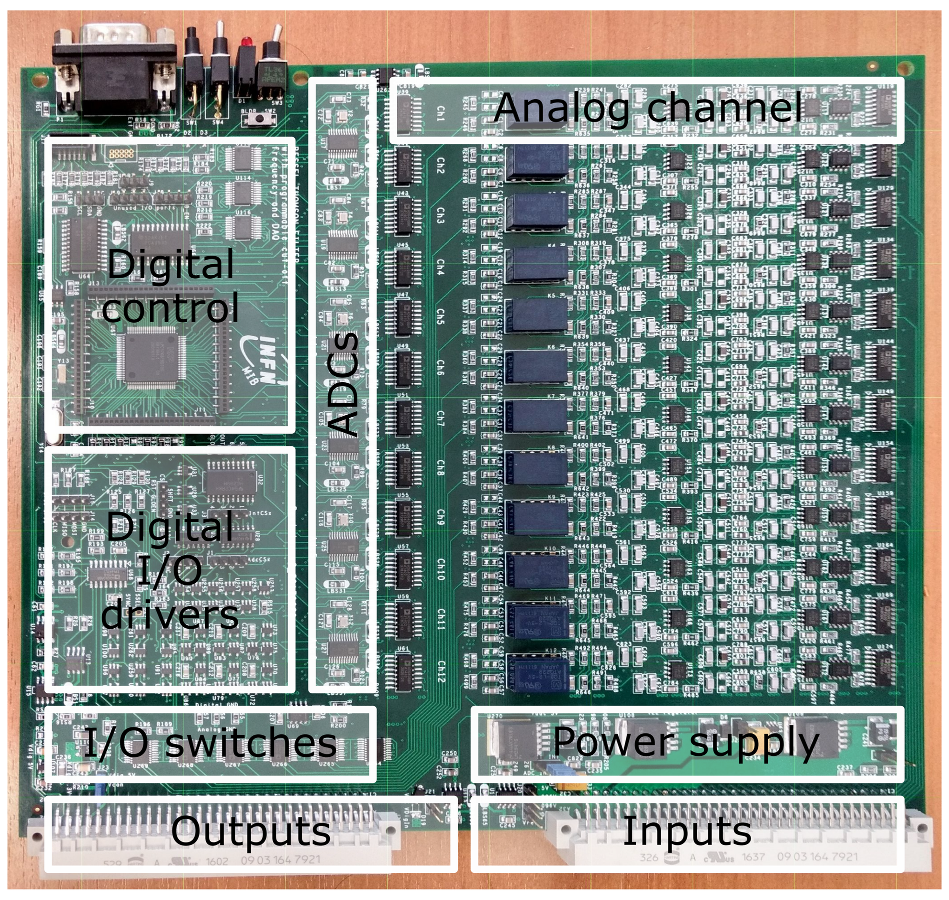

Figure 1: Photo of the low pass filter and DAQ board (12 channels)

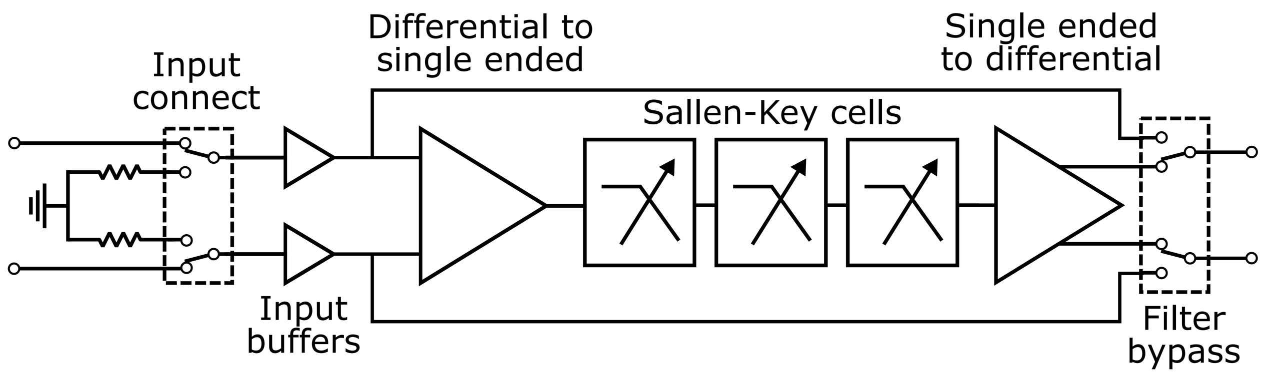

Figure 2: Analog filtering block with programmable cut-off frequency

The board has 12 channels, each one equipped with a 6-pole Bessel-Thomson low pass filter with 10-bit **digitally selectable cut-off frequency** from 24 Hz up to 2.5 kHz. The board is equipped with 24-bit ΔΣ ADCs which are able to digitize the signals up to **25 ksps** per channel in 12-channel mode or 250 ksps in 6-channel mode.

Channels	12
Power supply	± 12 V, + 5.5 V
Power consumption	250 mW/channel
Filter	6-pole Bessel-Thomson
Cut-off frequency	24 Hz - 2.5 kHz
Cur-off frequency resolution	10 bit
Input differential signal	± 10 V
Gain	1 V/V
Noise (analog)	< 7 µV RMS
PSRR (DC to 10 kHz)	-70 dB
CMRR (DC to 100 Hz)	-70 dB
ADC resolution	24 bit
Maximum sampling frequency	25 kHz (250 kHz with 6 ch.)
Cumulative sampling frequency	1.5 MHz
Effective resolution (1 kHz)	22 bits
Effective resolution (5 kHz)	21.3 bits
Effective resolution (25 kHz)	19.7 bits
Offset drift	10 µV/°C (1 ppm/°C)
Gain error (calibrated)	20 ppm
Gain drift	10 ppm/°C

Table 1: Specifications and performance

Selected measurements

Boards were fully qualified both on the analog part and on the digital part. The system (FPGA included) requires **250 mW/channel** with grounded inputs and 337 mW/channel with 5 V DC input signal.

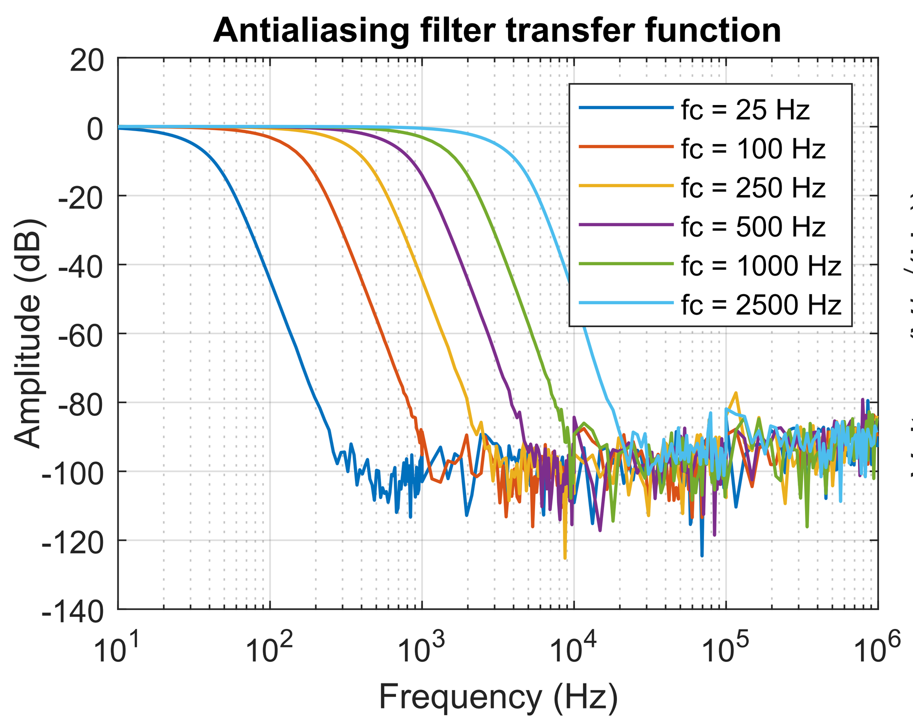

Figure 3: Analog filter transfer function at different cut-off frequency settings

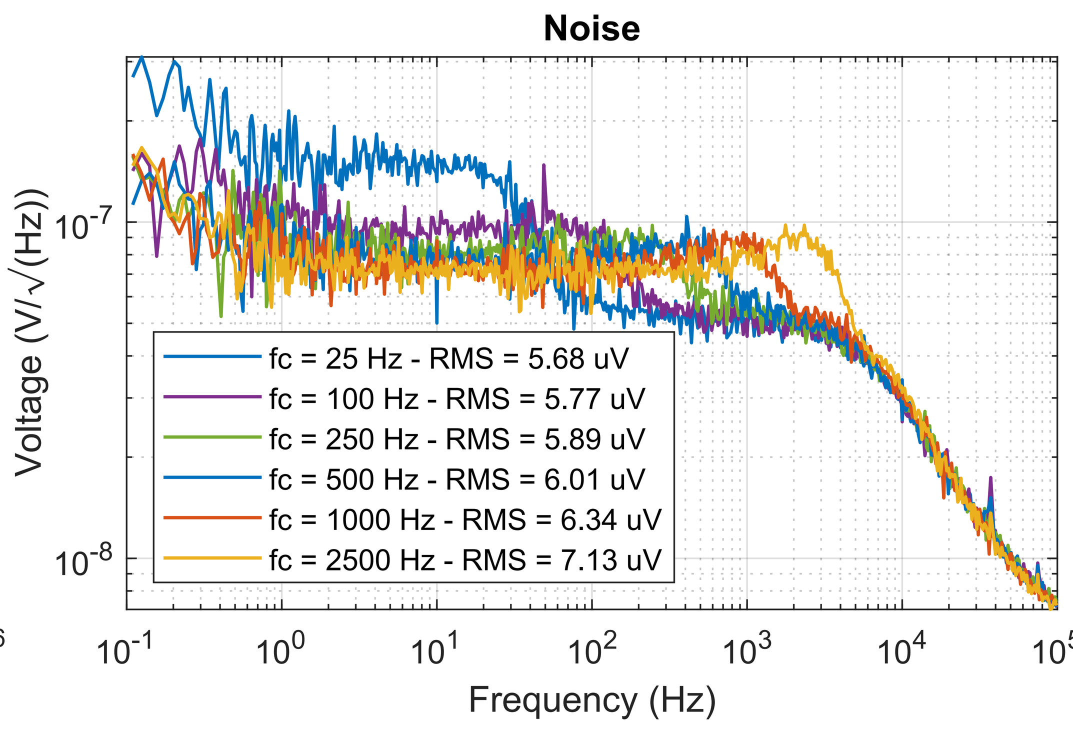

Figure 4: Analog noise spectra at different cut-off frequency settings

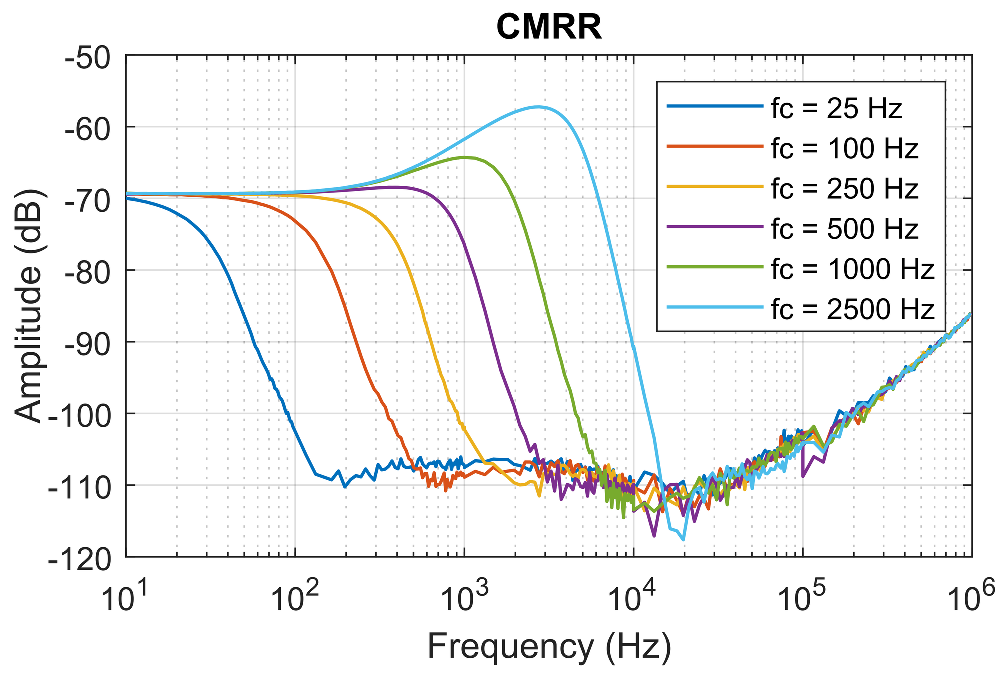

Figure 5: Common mode rejection ratio at different cut-off frequency settings

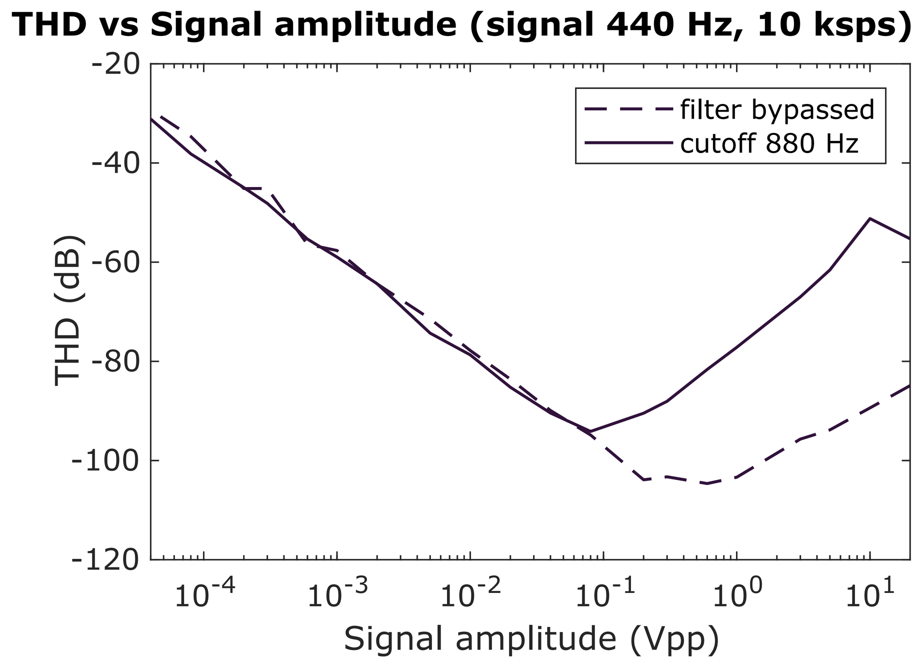

Figure 6: THD+N as a function of signal amplitude, signal 440 Hz and 10 ksps

Data transfer and slow control

An FPGA module (Enclustra Mars MA3) manages the **continous data stream through UDP** (RTP) to the storage system. Slow control server is based on Python and ZeroMQ, running on the **FPGA SoC**.

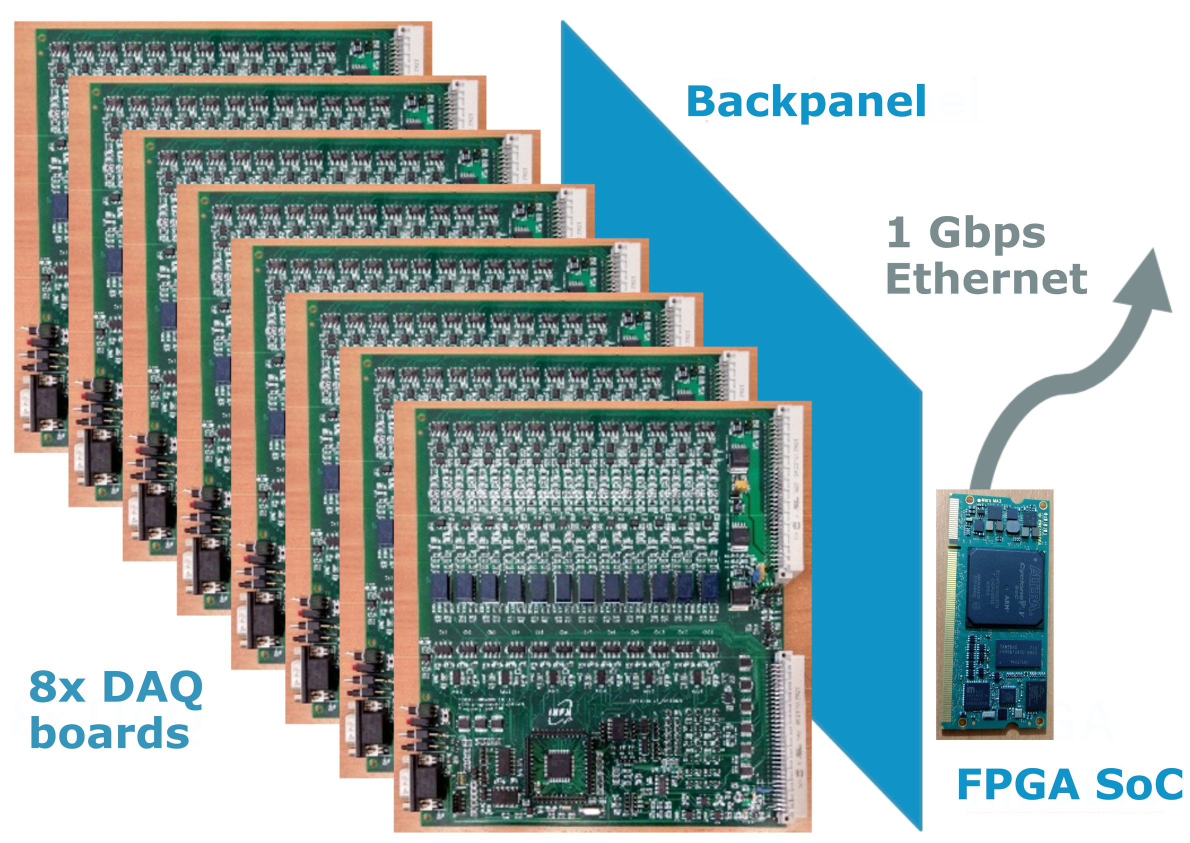

Figure 7: Back-end block schematic

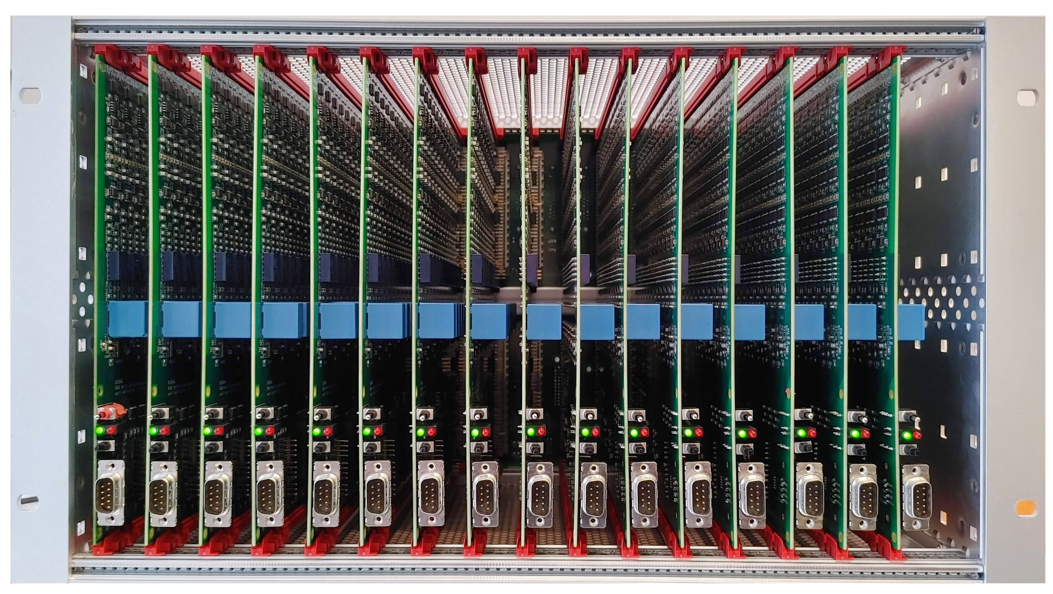

Figure 8: Full crate with 16 boards (192 channels)

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