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DCR and crosstalk characterization of a bi-layered 24x72 CMOS SPAD array for charged particle detection

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Single Photon Avalanche Diodes (SPADs) are getting rising attention in the field of optical sensing systems, since they can offer outstanding time and space resolution in a wide set of applications. In addition, SPADs can take advantage of CMOS planar technology, which enables the integration of both sensor and processing electronics in the same chip.
This work will present the results from the characterization of a SPAD based sensor, fabricated in a 150 nm CMOS technology, for charged particle tracking. In order to compensate for the relatively high dark noise mostly deriving from using a non-custom technology, two chips of SPADs were vertically interconnected by means of bump bonding techniques, to make up a dual layer structure. The detection system is based on the coincidence of signals coming from the two different layers of SPAD sensors. If a particle passes through both the sensing elements of a bi-layer cell, the two pulses overlap with each other and a coincidence signal is generated. On the other hand, obtaining overlapping signals as a consequence of dark pulses is unlikely, due to the statistical nature of noise. Dark count rate (DCR) measurements, performed on both independent single layer and dual layer chips, featured respectively a median value approximately equal to 2 $Hz/\mu m^2$ and 100 $\mu Hz/\mu m^2$, therefore demonstrating the beneficial impact of the two-layer approach on noise performance.
In the conference paper, measurement results relevant to crosstalk featured by single and dual layer chips will be discussed. The structure under test consists of 1728 cells with a pitch of 50 μm. Different measurement procedures, described in the final paper, have been used to study the crosstalk contribution coming from pixels highly affecting the noise performance of the neighboring ones. Eventually, some considerations about crosstalk probability will be provided.

Collaboration

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