DCR and crosstalk characterization of a bi-layered 24×72 CMOS SPAD array for charged particle detection

- Two chips of Single Photon Avalanche Diodes (SPADs), fabricated in 150 nm CMOS technology, were vertically interconnected by means of bump bonding technique, to make up a dual layer structure, aiming low noise and reduced material budget, in view of applications to charged particle tracking.
- An array of 24×72 SPADs, with an active area of 44×24 µm² was characterized in terms of dark count rate (DCR) and crosstalk. DCR measurements performed on both single and dual layer chips have demonstrated the beneficial impact of a bi-layer structure.
- From crosstalk measurements, significative DCR degradation, mainly due to a set of 9 particularly noisy pixels, was observed. The screamer pixels were found to affect mostly the DCR of adjacent sensors, since emitted photons are more likely to be absorbed in the closer SPADs as compared to the farther ones.
- RTS measurements were performed at different excess voltages, with a period of 115 s for a total amount of time equal to 23 days. Two-level, three-level and four-level fluctuations were observed.