DCR and crosstalk characterization of a bi-layered 24×72 CMOS SPAD array for charged particle detection

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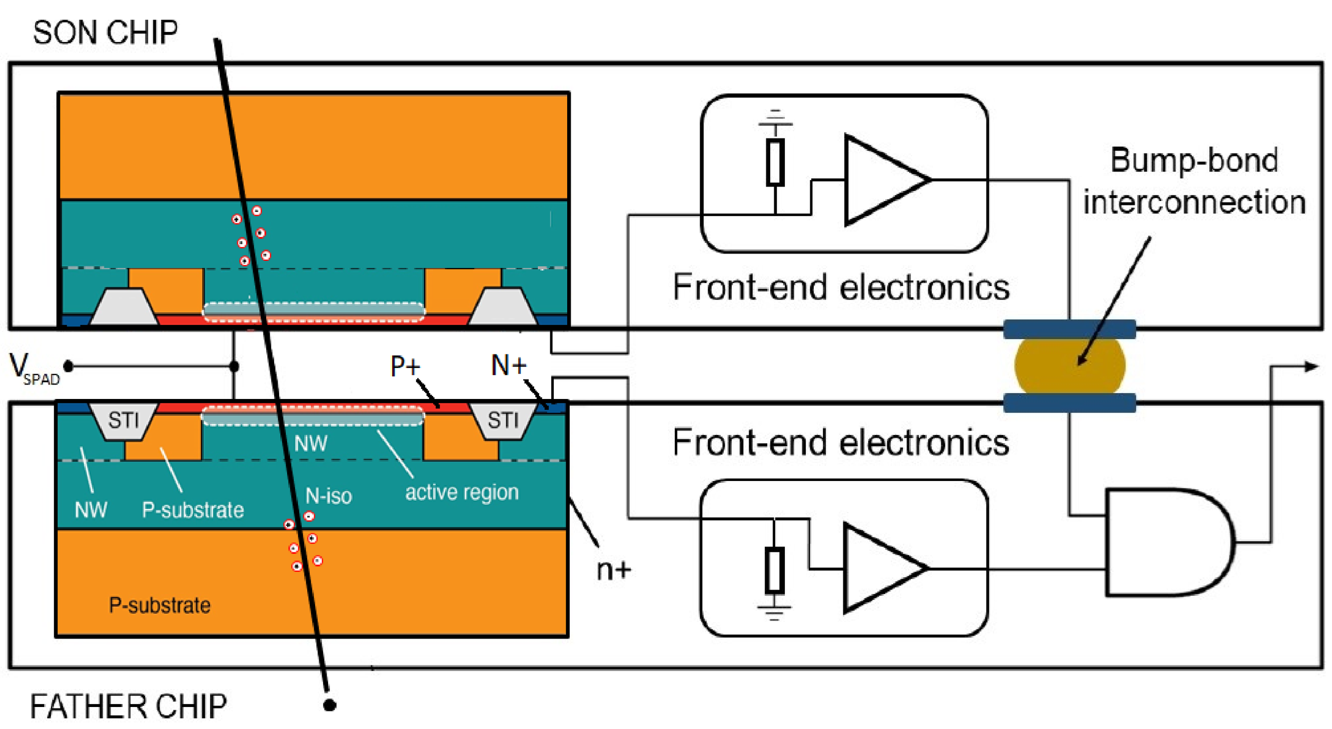
INTRODUCTION

At the state of the art, single photon avalanche diodes (SPADs) are largely used in a wide set of imaging applications involving single photon counting and event timing. Recently, the remarkable SPAD features, most notably spatial and time resolution, have been investigated in view of applications to charged particle tracking. The implementation of SPADs in standard CMOS technologies has enabled the development of high density monolithic detectors integrating both the sensing elements and the readout electronics in a common substrate. The main drawback coming from using a non-custom technology is represented by the relatively high dark noise, expressed in terms of dark count rate (DCR), which may jeopardize the detector capability as charged particle detectors.

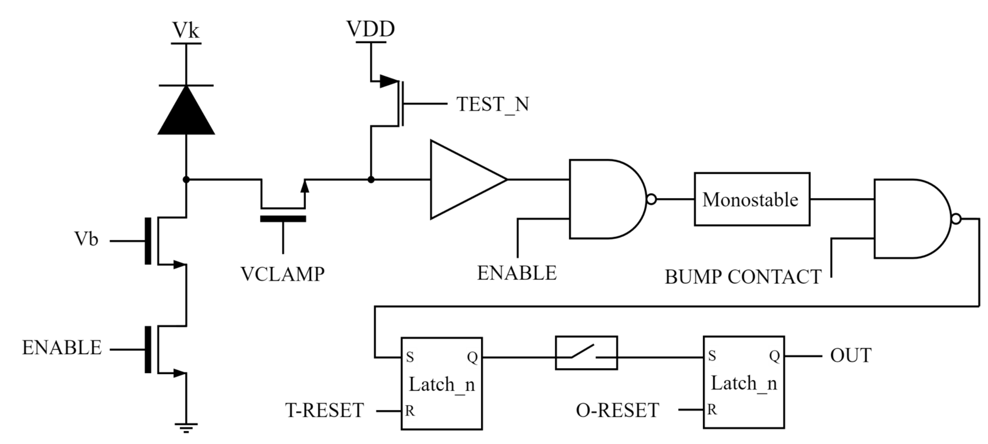
THE ASAP APPROACH

In order to compensate for the relatively high dark noise featured by CMOS SPADs, two chips are vertically interconnected by means of bump bonding techniques, thus resulting in a dual layer structure. The detection system is based on the coincidence of signals coming from the two different layers of SPAD sensors. An output signal is generated as a result of a particle crossing both the sensing elements of a bi-layer cell.



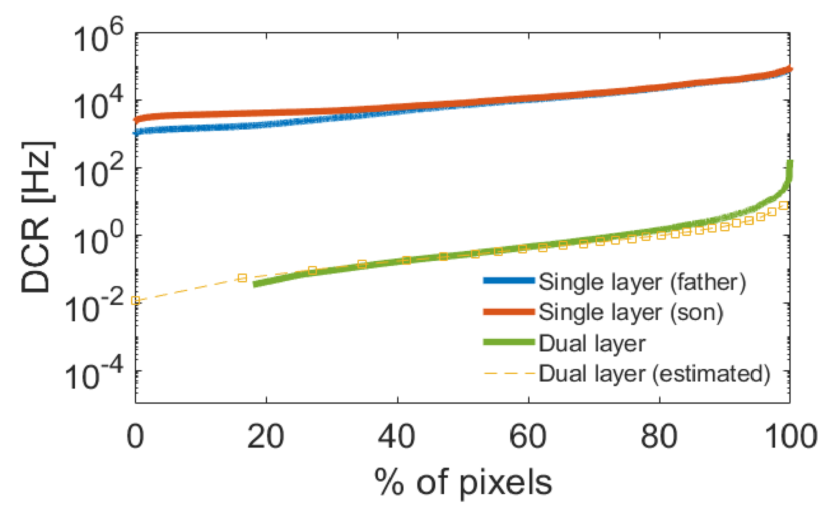
THE APIX2LF CHIP

The APIX2LF chip was fabricated in a 150 nm CMOS technology. Different array structures have been integrated in this chip.



The array under test consists of 24×72 SPADs, having a pitch of 50 µm and an active area of 44×24 µm^2. Each pixel is provided with a front-end circuit including a monostable circuit and a 1-bit memory.

DCR MEASUREMENTS

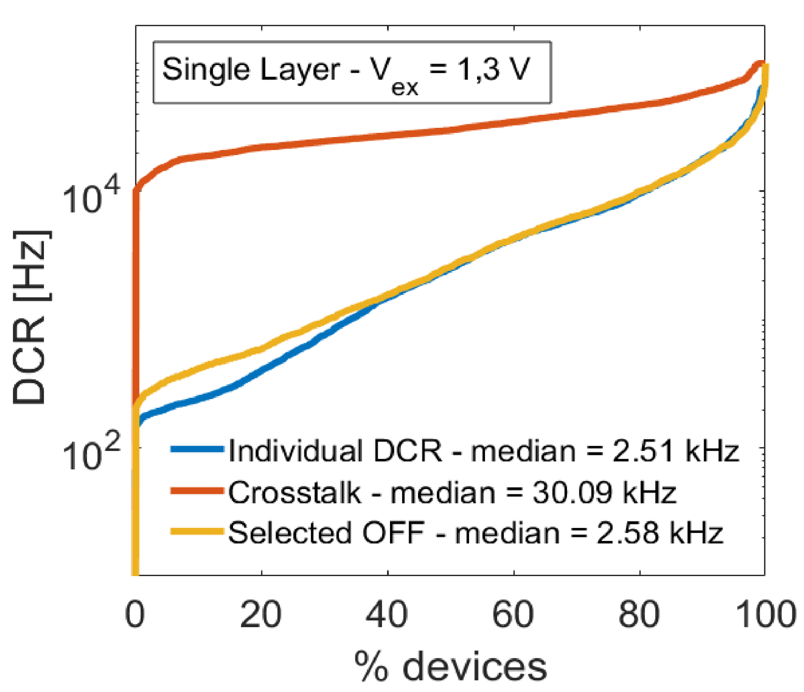


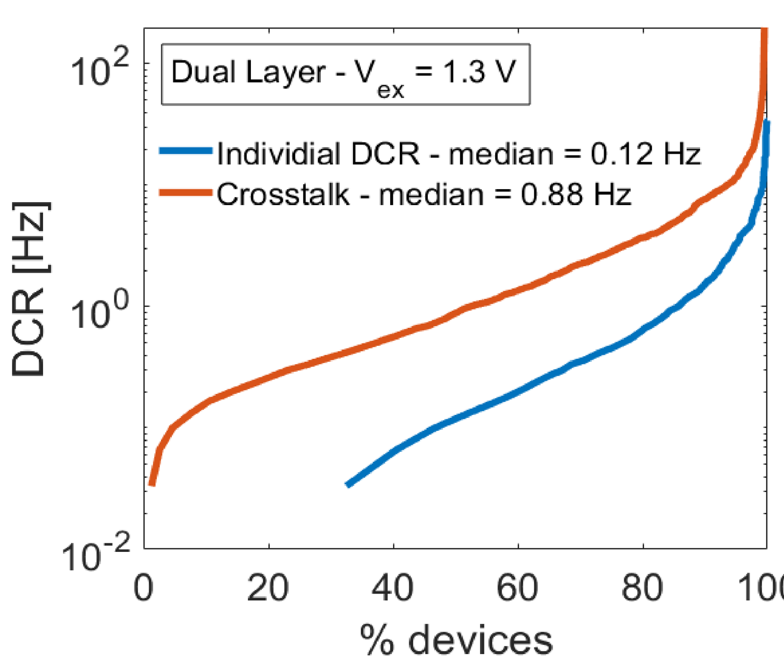
For the dual layer structure the expected DCR is:

$$DCR_{DUAL} = 2 \times DCR_1 \times DCR_2 \times \Delta t,$$

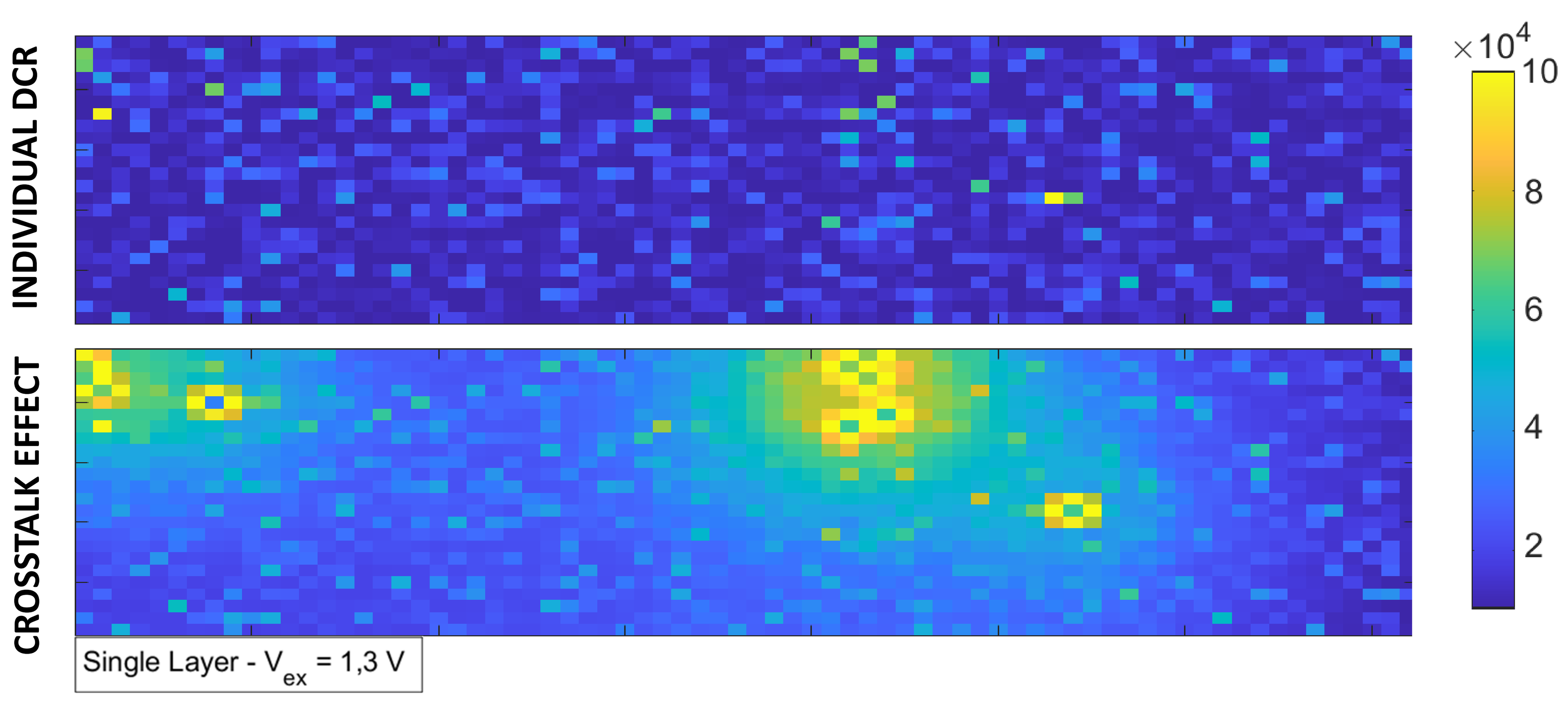
where Δt is the coincidence window. DCR measurements performed on both single and dual layer chips have demonstrated the beneficial impact of a bi-layer structure.

CROSSTALK MEASUREMENTS





- **Individual DCR** measurements were performed by switching on only the quenching circuit and the readout network of the selected SPAD.
- For the **crosstalk** measurements, all the pixels in the array were kept enabled when the DCR of each SPAD was being individually evaluated. In both single and dual layer chips, significant noise degradation was observed, due to the emission of secondary photons.
- A third measurement was carried out by **selectively** switching off a group of 9 SPADs marked as "screamers". The resulting curve is very similar to the first one, thus demonstrating the effectiveness of a small group of noisy pixels in degrading the DCR performance of the entire array.



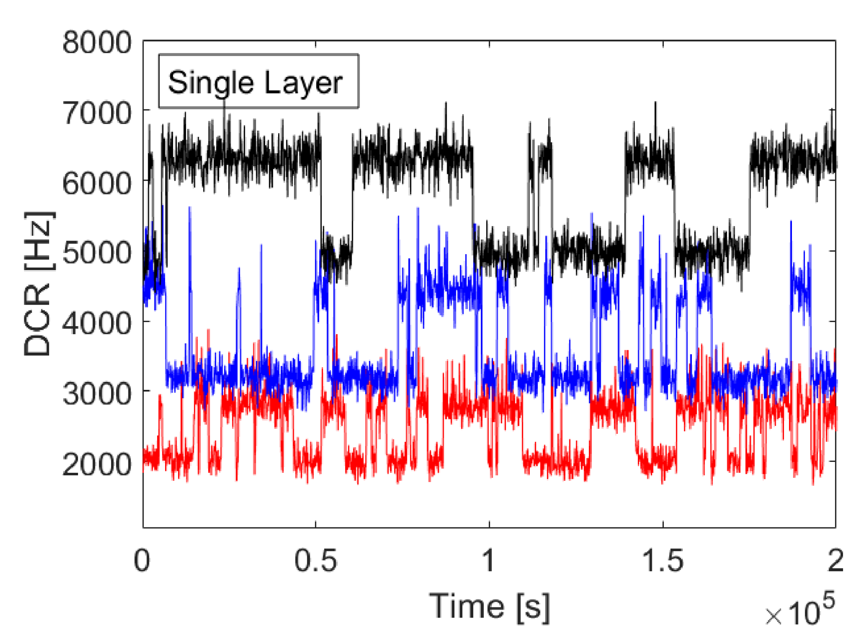
0.513	1.253	0.708	0.675	0.671
0.264	1.156	6.657	3.396	0.748
1.508	4.45	SCREAMER	2.53	1.242
0.774	0	4.271	2.392	0.648
0	1.047	0.466	0.532	0.414

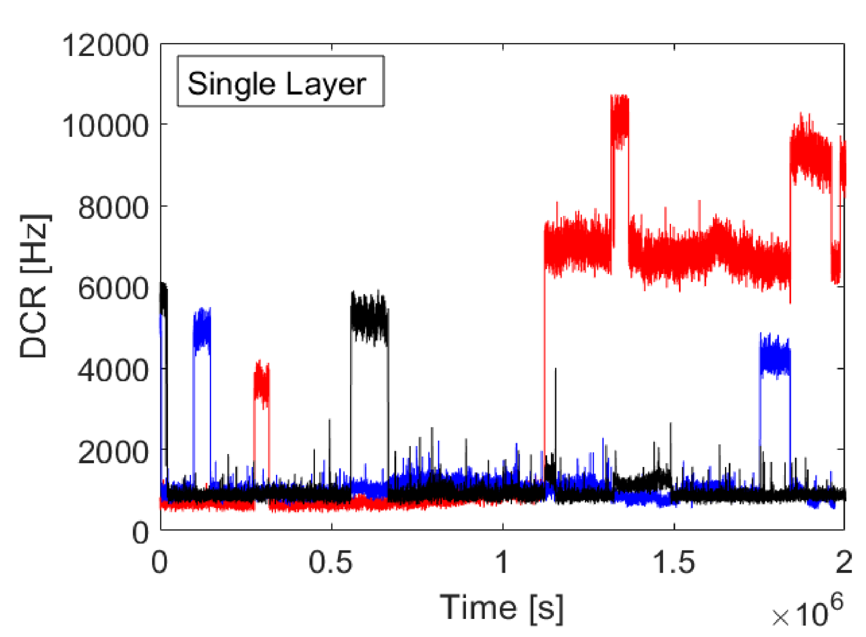
Crosstalk probability measurements were performed on a number of screamer pixels. The noisy SPADs, one per measurement, were left free to produce dark pulses, while the DCR of a subset of neighboring sensors was measured, one pixel at a time. In such a way, an emitter-detector pair is formed. The crosstalk probability was calculated as

$$Crosstalk\ probability\ [\%] = \frac{DCR_{current\ pixel,\ screamer\ on} - DCR_{current\ pixel,\ screamer\ off}}{DCR_{screamer}}$$

As expected, the screamer pixel was found to affect mostly the DCR of adjacent sensors, since photons emitted by the central device are more likely to be absorbed in the closer SPADs, as compared to the farther ones.

RTS MEASUREMENTS





Repeated DCR measurements, at different excess voltages (1.5 V, 2 V, 2.5 V), were performed with a period of 115 s for a total amount of time equal to 23 days. A large number of SPADs was found to be affected by RTS phenomena in DCR. Two-level, three-level and four-level fluctuations were observed.