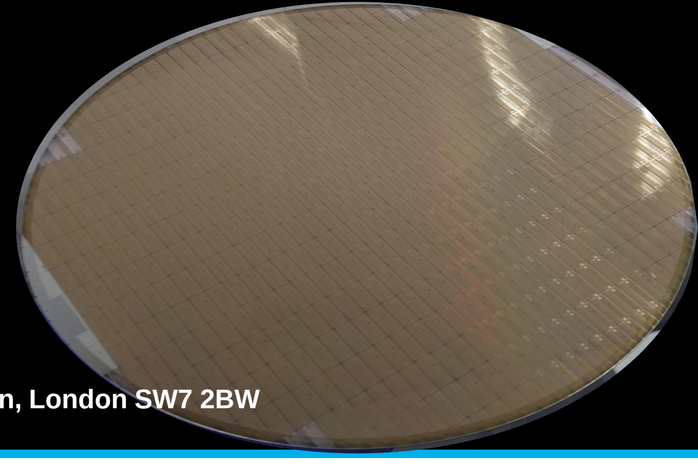
Studies of the CBC3.1 readout ASIC for CMS 2S-modules



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Outline

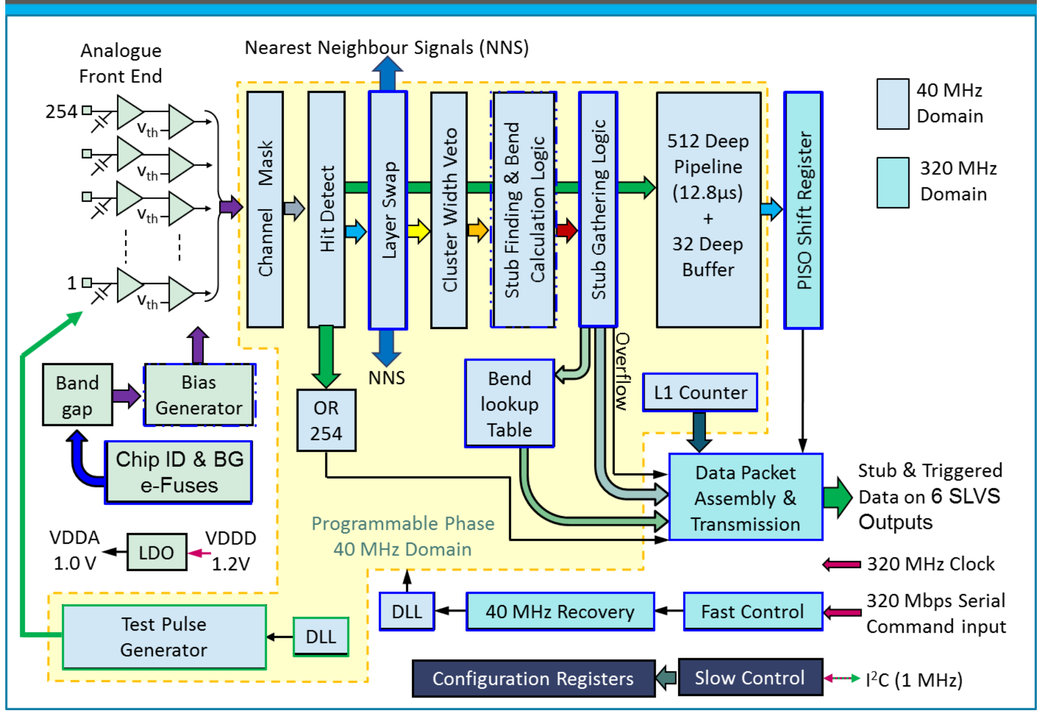
The CBC3.1 is the final version of the CMS Binary Chip for readout of the outer radial region of the upgraded CMS Tracker at the High Luminosity LHC. The CBC provides front-end readout of “2S-modules” which identify “stubs”, or short track vectors made of hits in adjacent sensor layers. The CBC transmits two kinds of data off-chip: hit data on receipt of a L1 trigger, and ”stub” data at the 40 MHz beam crossing rate to contribute to the trigger. Data transmission is at 320 Mbps.

The CBC development was completed in an engineering run in 2018 and two pre-production lots delivered in 2019. Large scale manufacture began in May 2021 and 270 production wafers have been received.

Issues were raised when some wafers were tested at low temperature (-30°C) and probing was suspended for investigation. After studies, some additional tests were added and the probing restarted.

The system can test two wafers per day; 70 wafers have already been probed. To accelerate the probing, another station is in preparation, but delayed by a bike accident and a climbing accident.

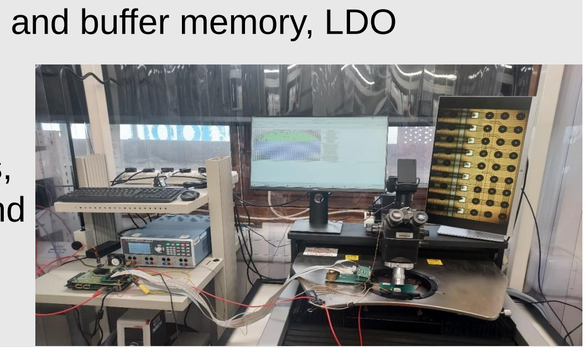
CBC 3.1 architecture



Wafer probing system

The setup is at Imperial College London. A PC is connected to the wafer prober and dedicated interface electronics to CBC. The chuck position on the station is set and a series of tests are performed on each die automatically. For a whole wafer, this takes 7.5 hours.

Tested functions are currents, I2C registers, 320 MHz serial data lines, pipeline and buffer memory, LDO bandgap and output voltage, offset tuning, channel masks, s-curves, gain, DLL, Fast Command Interface, stub logic, and channel masks.

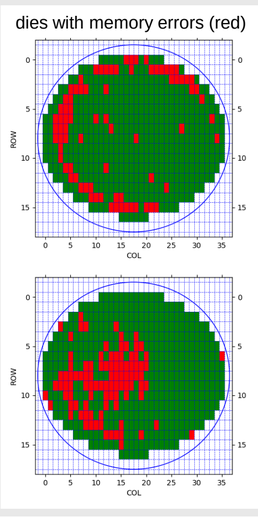


Issues found in low temperature tests

Wafer probing was not intended to be performed at low temperature, but was undertaken to study yield issues and check performance at CMS operating temperatures. It was challenging to achieve humidity control and good probe contact quality, but 28 wafers from 2 pre-production lots and 4 production lots have been tested at -30°C. The low temperature tests found rare memory bit errors in some lots, and occasional corruption of some I2C registers under certain conditions.

Further investigation found that I2C errors could be mostly be identified at room temperature by operating the chip at the lowest DC voltage.

Both issues have been found to be correlated with non-optimal manufacture as indicated by low overall yield and circular yield patterns on the wafers as shown in the figures. Normally failing chips are randomly distributed on the wafers.



Results of investigation of the memory errors and I2C malfunctions

Memory errors (hit data) are very rare and related to lot production quality, but would have negligible impact on tracker hit occupancy even if the worst case rate were normal. Many of the chips which show this error at the low temperature are found to show errors in redundant data which was not checked in the original test at room temperature. This test is added to remove possible defective chips due to non-optimal manufacture.

I2C register errors

To deal with more than 256 addresses, a paging scheme is adopted. The page is controlled by a special register at address 0 which does not belong to either page. Corruption is observed when a write operation is conducted on page 2 or when writing the register at address 0 to change the page. An address decoder is located next to each offset register and the page bit and write lines are close to each other. The long paths and the line alignment is suspected to be sensitive to the process quality.

A simplified summary of I2C register corruption is:

- Single-channel threshold offset tuning values in page 2 are affected and the number of those registers depends on the temperature and VDDD
- In multiple checks, the corrupted register is usually the same one but it is not the same register on every chip, and each register has different corruption rate on the write operation.
- There is a strong correlation between I2C failures at minimal supply voltage and low T results and most chips with the error can be rejected by a stress test at VDDD = 1.1V with tolerable impact on the yield (>75% is the target)
- As seen in the Fig(a), if the stress test at low VDDD is added to the original test, the remaining channels with an error at low T are fewer than 5 per wafer. Each wafer has 478 dies, and each chip has 254 channels. As shown in the Fig.(b), estimated impact on occupancy would be < 10^{-4} compared to an expected occupancy of 1-2%.

Figure (a)

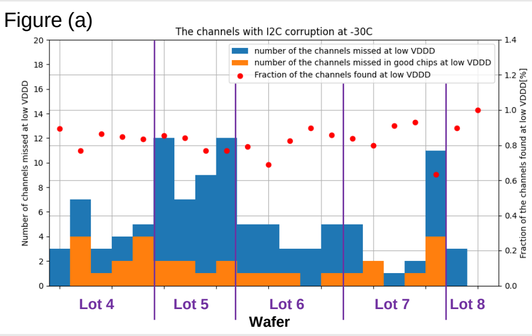
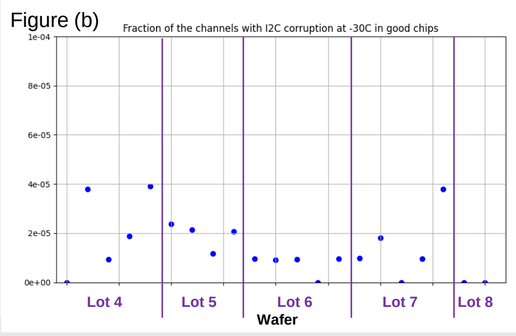
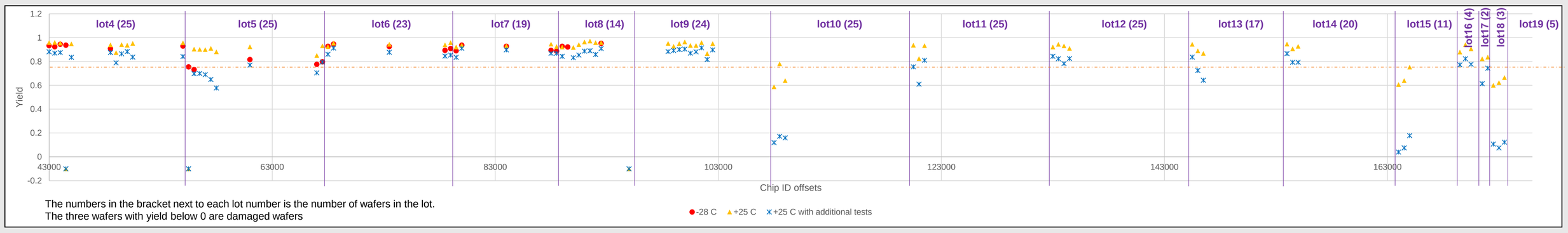


Figure (b)



Yield and conclusion



75 CBC3.1 wafers (3 are damaged) from 16 production lots have been tested. Some of those wafers were tested at low temperature and tested again at room temperature with new additional tests which successfully identify chips with malfunctions. Both faults are strongly correlated with non-optimal manufacturing quality, although subtle features of the design may also be implicated. Some strong lot to lot variations are evident in the yield results above. Neither fault will have a significant impact on tracker occupancy during operation.