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## 28 nm CMOS analog front-end channels for future pixel detectors

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This work discusses the design of analog front-end circuits for future, high-rate pixel detector applications. The front-end design activity is being carried out in the framework of the INFN Falaphel project, aiming at the development and integration of silicon photonics modulators with high speed, rad-hard electronics in a 28 nm CMOS technology. The project targets the tracker of the hadronic Future Circular Collider (FCC-hh) experiments, with the opportunity to replace the inner pixel systems of the high-luminosity LHC experiments after 2030.

Two front-end architectures are being developed, one with Time-over-Threshold digitization of the input signal and the other based on in-pixel flash ADCs. The first architecture includes a charge sensitive amplifier (CSA) featuring a Krummenacher feedback network for detector leakage current compensation. The CSA output is connected to a comparator implemented by means of a differential pair driving a common source output stage. In the second version of the front-end, a novel, clocked comparator is being developed and conceived to dramatically reduce the threshold dispersion of the front-end.

The conference paper will include a thorough description of the analog processors being developed. The main analog performance parameters, as obtained from circuit simulations and including equivalent noise charge, threshold dispersion and time-walk, will be presented.

### Collaboration

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