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28 nm CMOS analog front-end channels for future pixel detectors

INFN Falaphel project

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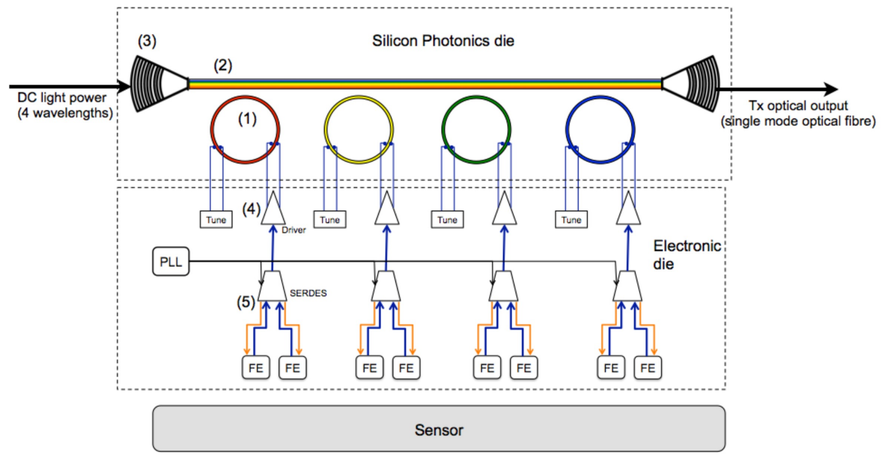
Introduction

Next generation pixel readout chips for high energy physics (HEP) experiments will be exposed to **extremely high levels of radiation** and **particle rates**.
The state of the art of pixel front-end electronics for HEP is currently given by the chips developed by RD53. They are fabricated in a **65 nm** CMOS technology, that proved to be capable of addressing the requirements of ATLAS and CMS pixels at the HL-LHC. The **28 nm** CMOS is the next major industrial node after 65 nm, and the HEP microelectronics community in general is oriented to 28 nm for future developments.
This work discusses the design of analog front-end circuits for future, high-rate pixel detector applications. The front-end design activity is being carried out in the framework of the INFN Falaphel project, aiming at the development and integration of silicon photonics modulators with high speed, rad-hard electronics in a 28 nm CMOS technology. The project targets the tracker of the hadronic Future Circular Collider (FCC-hh) experiments, with the opportunity to replace the inner pixel systems of the high-luminosity LHC experiments after 2030.

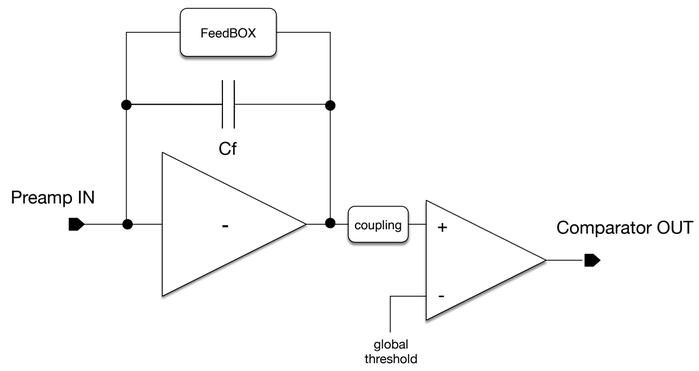
The INFN Falaphel project



- INFN funded project (CSN5) 2021-2023 (830 kEuros, 35 people and ~13 FTE)
- **Participant institutes:** INFN Padova, INFN Pavia, INFN Pisa, Scuola Superiore S. Anna di Pisa, Dip. Ingegneria Informazione UniPisa, Dip. Fisica UniMilano
- **Goal**: Development and integration of Silicon Photonics modulators with high speed, rad-hard electronics in 28 nm
- **Demonstrator**: 100 Gb/s (4x 25 Gb/s) link possibly integrated with a matrix of front-end channels each featuring an area of **25x50 µm²**

Two front-end architectures being investigated

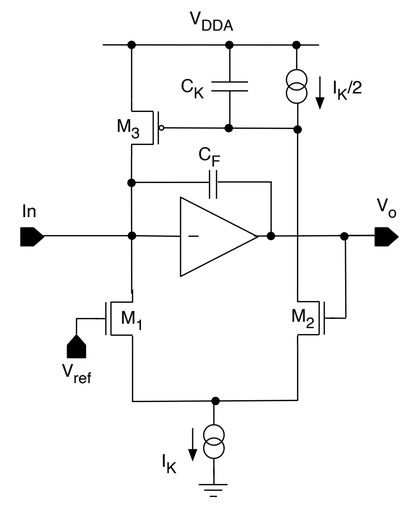
- **Time-over-Threshold (ToT)** based front-end → preamp + DC coupled comparator, with ToT A/D conversion of the signal + threshold tuning DAC
- **Flash ADC** based front-end → preamp + AC coupled bank of auto-zeroed comparators implementing the flash A/D conversion

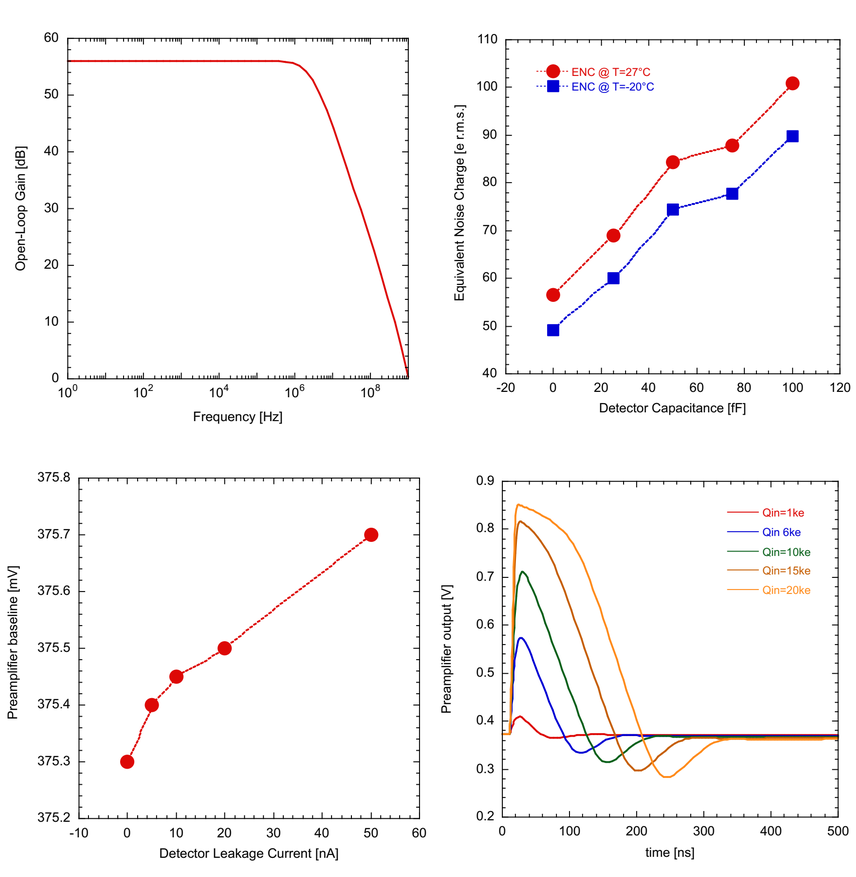


ToT based front-end

- **Single amplification stage** for minimum power consumption
- **Krummenacher feedback** to comply with the expected large increase in the detector leakage current
- **DC coupled comparator** driving a ToT counter
- 4-bit current-mode **threshold tuning DAC**
- Overall **current consumption**: ~4 uA → 3.6 µW **power consumption** @ V_{DD}=0.9 V

Charge sensitive amplifier

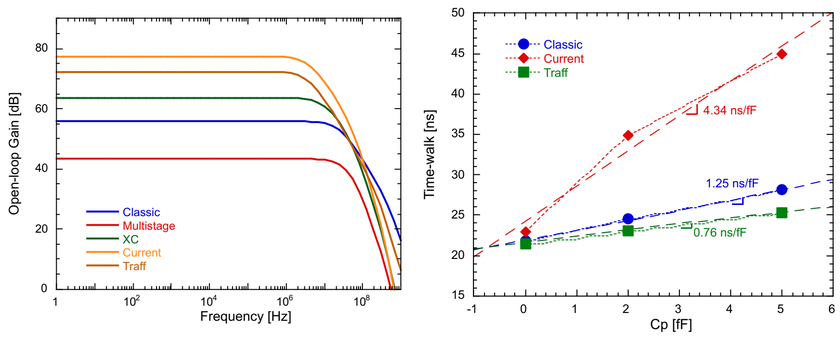




- **Regulated cascode** forward gain stage:
  - DC Open Loop gain → 56 dB
  - Cutoff frequency → ~2 MHz
- **Leakage compensation** circuit works fine for detector current up to 50 nA
- **Equivalent noise charge** (ENC) smaller than 105 e_{rms} for $C_{d,max}$ =100 fF

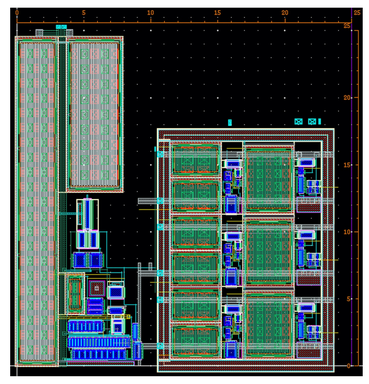
Comparator

- Different comparator architectures have been investigated
- Overall **time-walk** evaluated for three comparator versions
- Schematic-level simulations (ideal preamp with 20 ns peaking time)
- **Parasitic capacitance** (Cp) added to the main nodes of the comparators



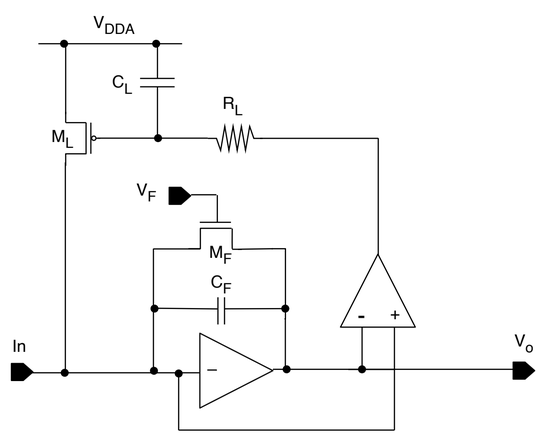
Flash ADC based front-end

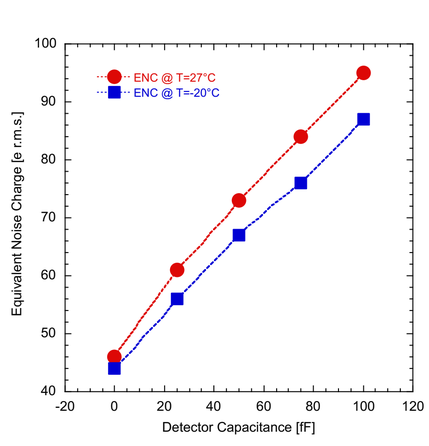
- **Single amplification stage** for minimum power consumption
- **Detector leakage compensation** based on an opamp in the feedback network of the preamp
- AC coupled comparators implementing **flash ADC**
- **Auto-zeroed comparators**, operated with 40 MHz clock. The implementation is ideally insensitive to device threshold voltage mismatch → threshold tuning DAC not required
- Overall **current consumption**: 3.8 uA → 3.4 µW **power consumption** @ V_{DD}=0.9 V



Layout of the analog front-end Preamplifier (left) + 2 bit Flash ADC (right)

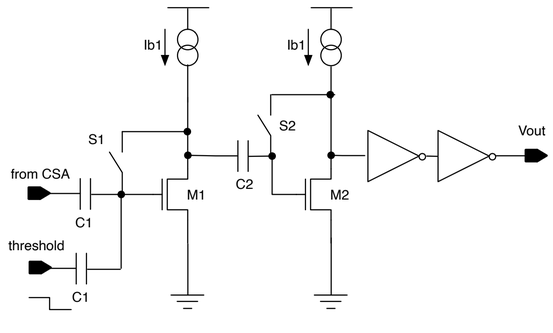
Charge sensitive amplifier

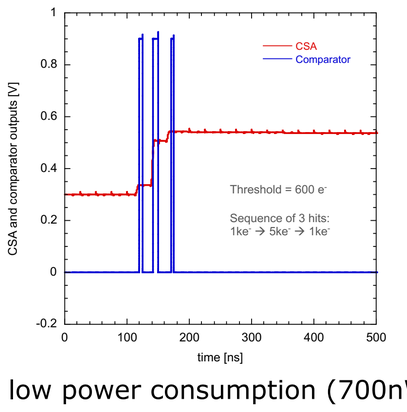




- Same **regulated cascode** gain stage as for the ToT-based FE, with an additional **common source output stage** needed to face kick-back noise from comparator
- **Equivalent noise charge** (ENC) smaller than 100 e_{rms} for $C_{d,max}$ =100 fF

Comparator





- Clocked, **auto-zeroed** comparator featuring low power consumption (700nW)
- **Zero dead-time**, low threshold dispersion (< 35 e r.m.s.)