The front-end electronics upgrade of the CMS ECAL Barrel

Fabio Cossio (INFN Torino) on behalf of the CMS Collaboration

PM2021 – 15TH Pisa Meeting on Advanced Detectors – 22-28 MAY 2022

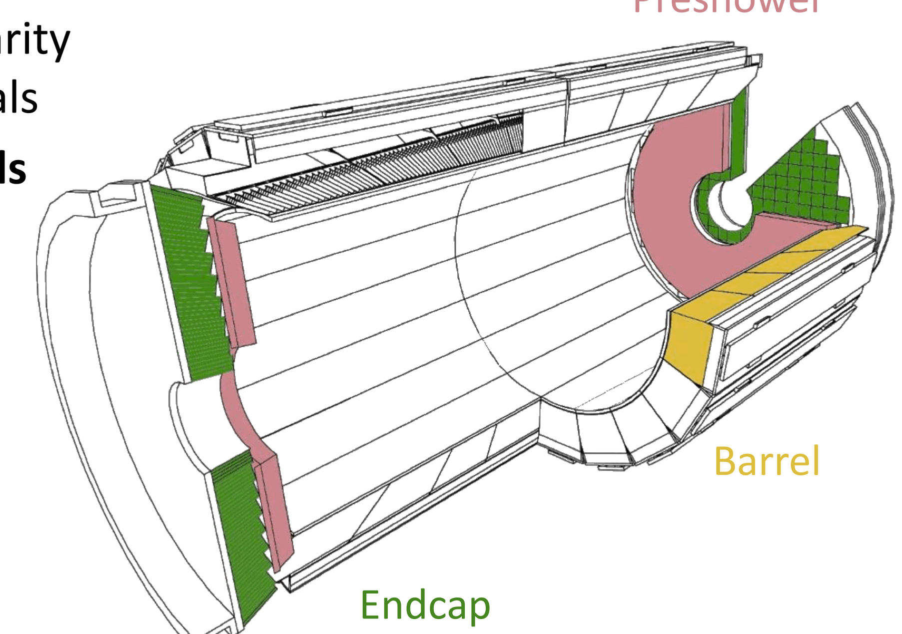
INFN
Istituto Nazionale di Fisica Nucleare

Introduction

The CMS Electromagnetic CALorimeter (ECAL)

Compact, homogeneous and hermetic high-granularity crystal e.m. calorimeter based on scintillating crystals

- 61.2k (Barrel) + ~14.6k (Endcaps) **$PbWO_4$ crystals**
- $t_{75\%}$ = 25 ns, X_0 = 8.9 mm, r_M = 2.19 cm



ECAL Barrel

- **APD sensors** readout
- 36 supermodules, 1700 crystals each
- 2448 readout units, made of **5x5 crystals**
- 5 VFE cards/unit, 5 channels/VFE
- Multi Gain PreAmplifier (MPGA) x1, x6, x12 gain, CSA + 40ns RC-CR shaper
- 12-bit, 40 MS/s ADC, dynamic range 40MeV – 1.5TeV

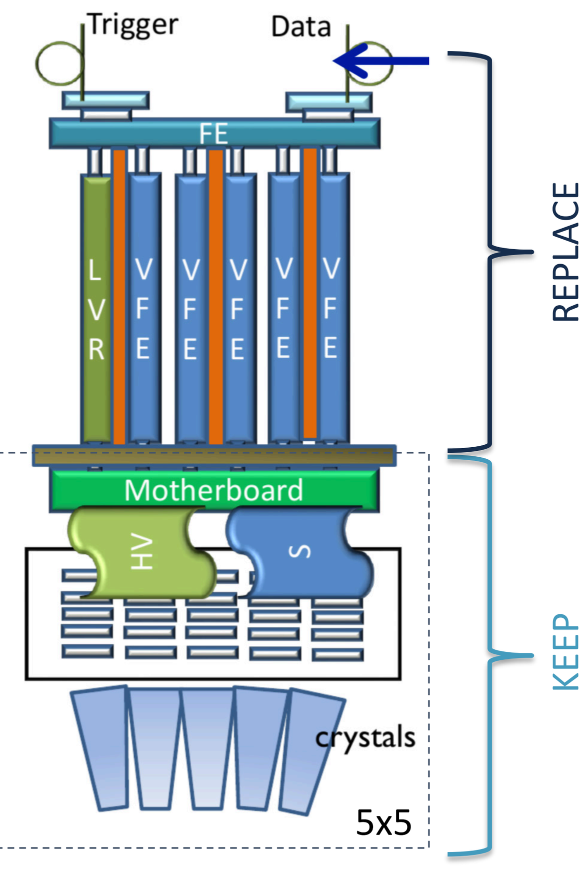
} LEGACY ELECTRONICS

HL-LHC ECAL Upgrade

- Design luminosity: 5–7.5 x $10^{34}cm^{-2}s^{-1}$
- High pileup: 140–200 p-p interactions in a single Bunch Crossing
- x10 design integrated luminosity

Radiation-induced detector ageing affects *crystal transparency* and *APD dark current*

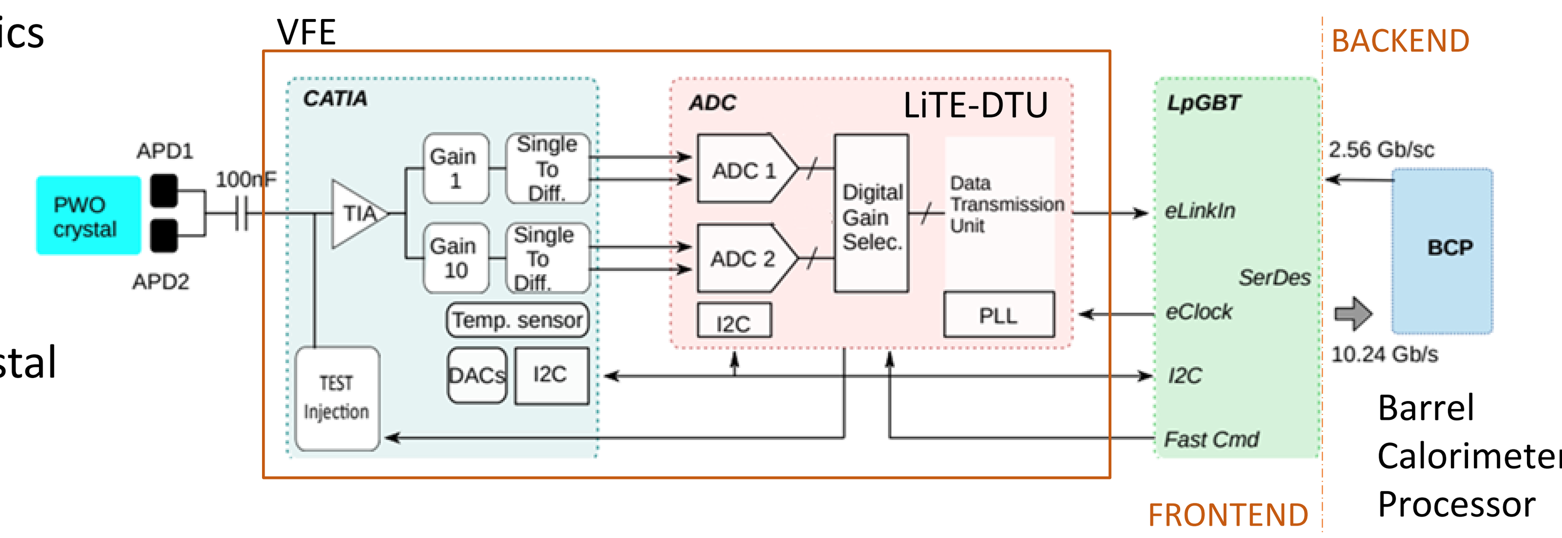
- **ECAL Endcap**: replace with a completely new detector (HGCAL)
- **ECAL Barrel**: reduce operating temperature from 18°C to 9°C to mitigate APD leakage current and increase light yield (keep crystals and APDs)



ECAL Barrel Electronics Upgrade

Redesign of VFE, FE and off-detector electronics to cope with new CMS trigger and DAQ requirements:

- L1 trigger latency: 4.5μs → 12.5μs
- L1 trigger rate: 100kHz → 750kHz
- Trigger granularity: 5x5 crystals → one crystal



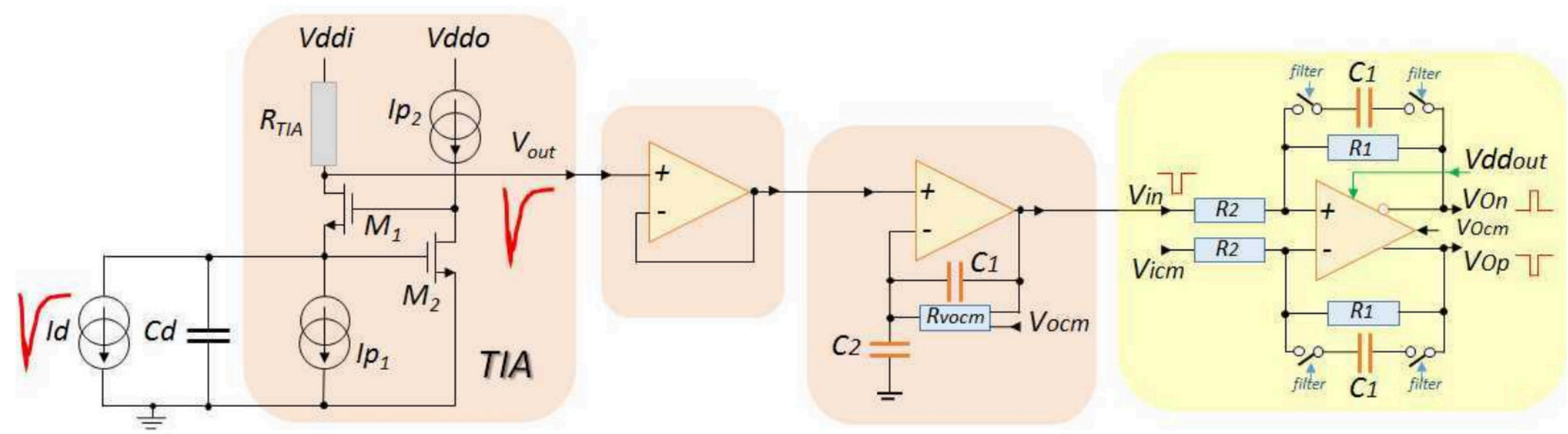
Two new, cascaded ASICs for faster FE electronics:

- Lower APD noise from leakage current
- Precision time measurement (30 ps resolution for H → γ γ photons) for improved primary vertex identification and reduced pile-up
- Better rejection of APD "*spikes*" → on the fly pulse shape discrimination

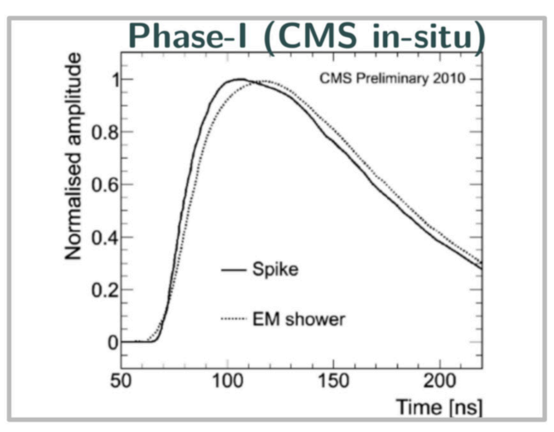
Front-end Electronics

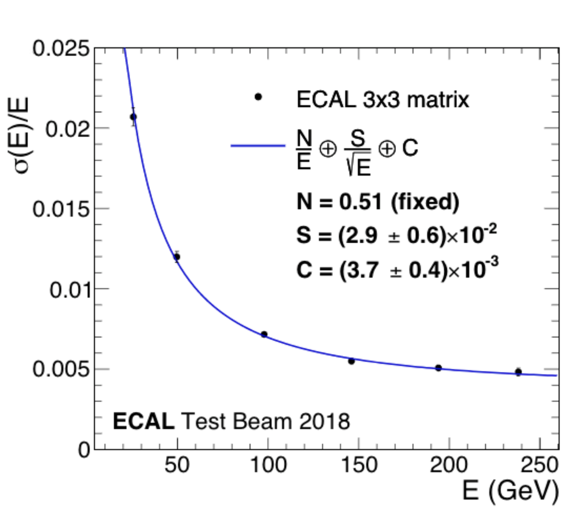
CATIA: Calorimeter Trans-Impedance Amplifier

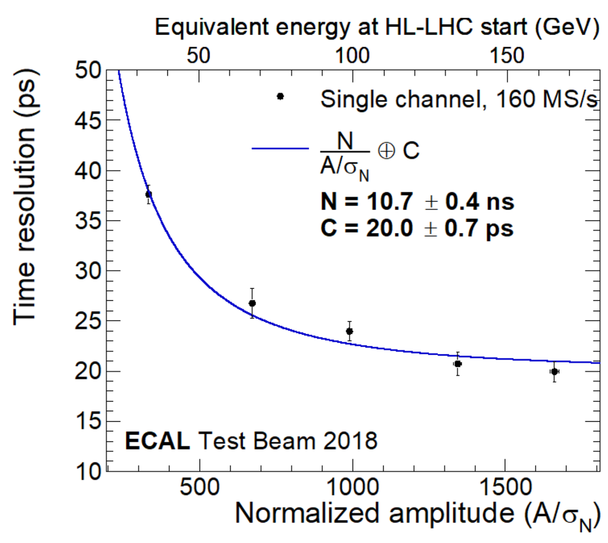
Single sensor readout system chip based on Trans-Impedance Amplifier (TIA)

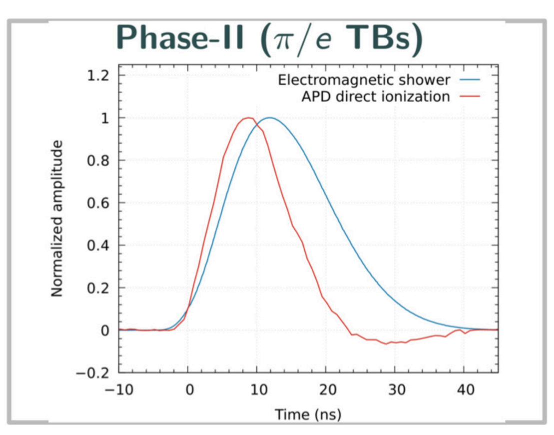


- Designed by CEA Saclay, 130 nm CMOS technology
- RCG input stage → very low Z_{in} and 35 MHz bandwidth
- **Dual gain**: 10x and 1x → 50 MeV – 2 TeV dynamic range
- Test pulse injection for gain and linearity calibration
- Output differential buffers with pedestal control









LiTE-DTU: Lisboa and Torino ECAL Data Transmission Unit

2x 12-bit, 160 MS/s ADCs

- IP block from commercial company
- time-interleaved 80 MHz SAR ADCs
- ENOB: 10.2 @ 50 MHz

Lossless data compression

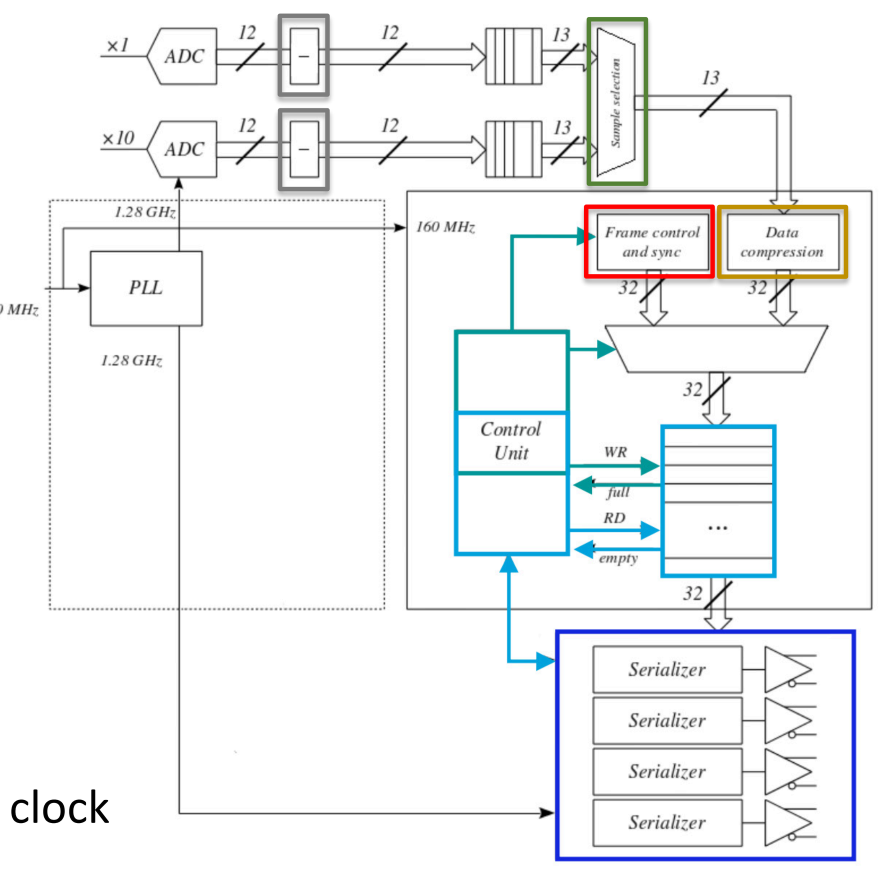
- 6 bits for signals < 2.4 GeV
- bw occupation: 2.08 Gb/s → 1.08 Gb/s
- fit in one lpGBT e-link (1.28 Gb/s bw)
- latency < 350 ns

PLL block from lpGBT to generate 1.28 GHz clock

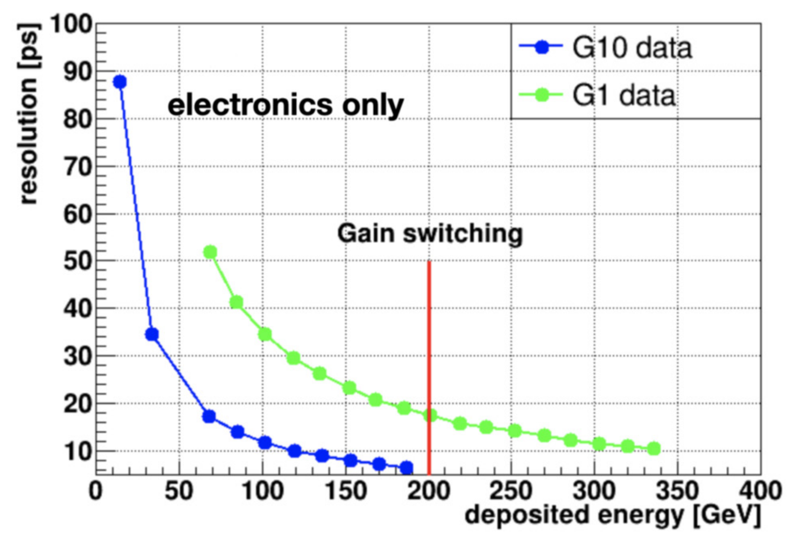
65 nm CMOS technology

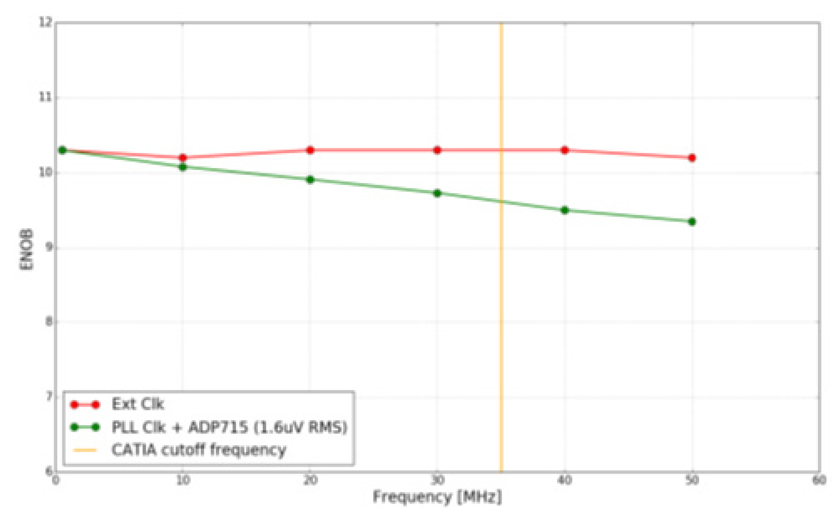
TID tolerance up to 20 kGy

SEU-protected logic



Arithmetic Baseline subtraction
Look-ahead gain selection
Data compression
Frame generation
Serial transmission





Conclusions and Outlook

The challenging conditions of HL-LHC require a complete re-design of the CMS ECAL Barrel electronics

- Faster FE electronics (~4x bandwidth, 4x sampling rate) → ~30 ps time resolution, PU effects mitigation and "*spikes*" suppression
- L1 trigger hardware moved off-detector for maximum flexibility → single crystal granularity

Very good performance already from ASICs prototype versions

Integration tests of ECAL Barrel electronics show good compatibility

Promising results from first tests of pre-production ASICs with improved performance and new features

Preparation for integration tests at larger scales: ~400 channels system for Fall 2022 test beam

ASICs mass production foreseen in 2022-23

Full installation during LHC Long Shutdown 3 (2024-2026)