Electrical Characterization of Pre-Production Staves for the ATLAS ITk Strip Detector Upgrade

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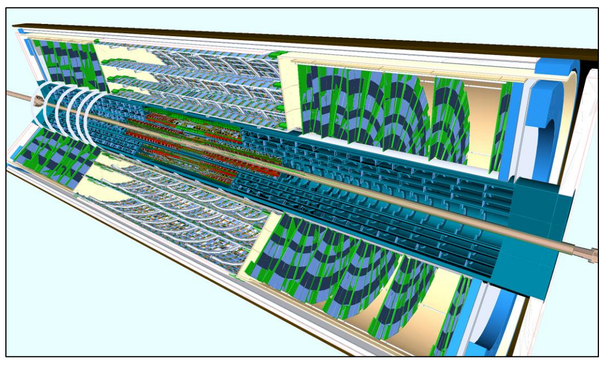
ABSTACT

The ATLAS experiment is currently preparing for an upgrade of the inner tracking detector for High-Luminosity LHC operation, scheduled to start in 2029. The new detector, known as the Inner Tracker or ITk, employs an all-silicon design with five inner Pixel layers and four outer Strip layers. The staves are the building blocks of the ITk Strip barrel layers. Each stave consists of a low-mass support structure that hosts the common electrical, optical and cooling services as well as 28 silicon modules, 14 on each side. To characterize the stave, a set of electrical and functional measurements have been performed both at room and at cold temperatures. At this conference, the results of the first fully instrumented pre-production staves assembled at Brookhaven National Laboratory will be presented.

INTRODUCTION

- The new all Silicon, ATLAS Inner Tracker (ITk) will replace the current ATLAS inner Detector for the High Luminosity LHC.
- HL-LHC : nominal luminosity $\mathcal{L}_{peak}$ ~ 7*10^{34} s^{-1} cm^{-2}, $\mathcal{L}_{Integrated}$ ~ 3000(4000) fb^{-1} and Pileup of ~200 per 25 ns.
- The ITk is made up of barrels and endcaps centered around the interaction point, covering the pseudo rapidity range from -4 to +4



ITk Pixel Detector

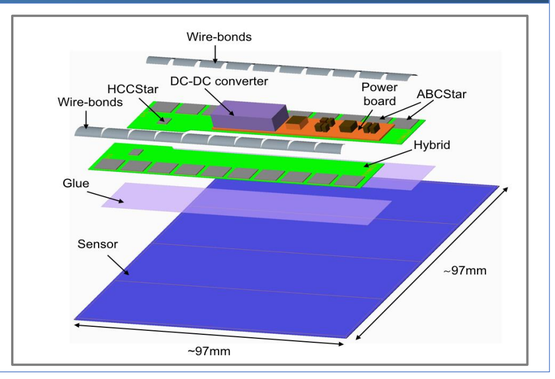
- 5-barrel layers including a section with inclined sensors
- End-Cap(EC) system containing individually located rings

ITk Strip Detector

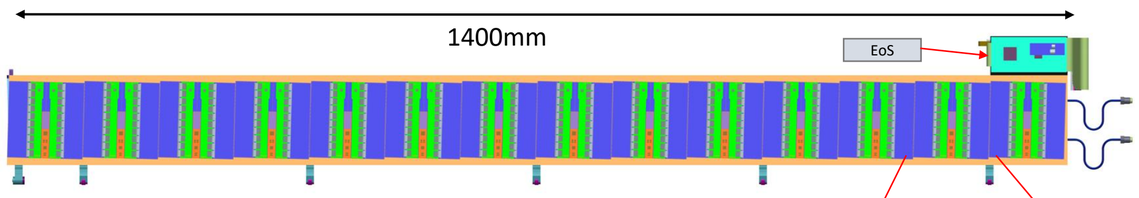
- 4-barrel layers
- End-Cap(EC) system with 6 rings on both sides

SILICON STRIP MODULES

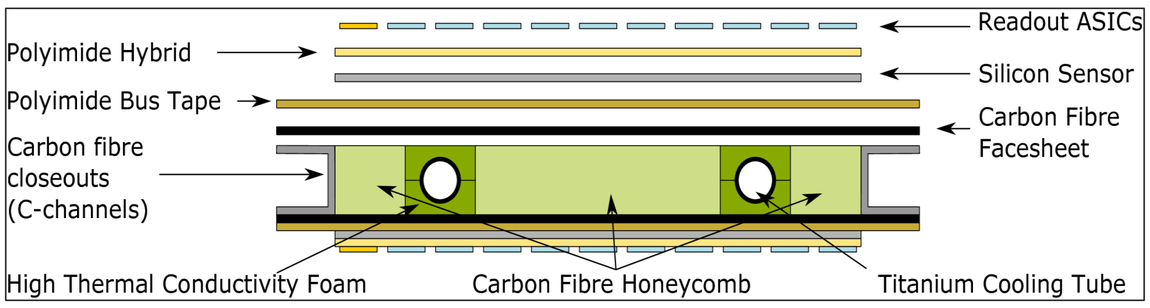
- Building blocks of the ITk strip detector.
- Consists of the Silicon microstrip sensor, one (for long strip, LS strip length 48.20mm) or two (for short strip SS strip length 24.10mm) PCBs called Hybrid and one Power board responsible for delivering Low Voltage power through the DC-DC buck Converter and also hosts the monitoring and controller chip AMAC.
- The hybrid hosts readout ABCStar and the controller chip called HCCStar.



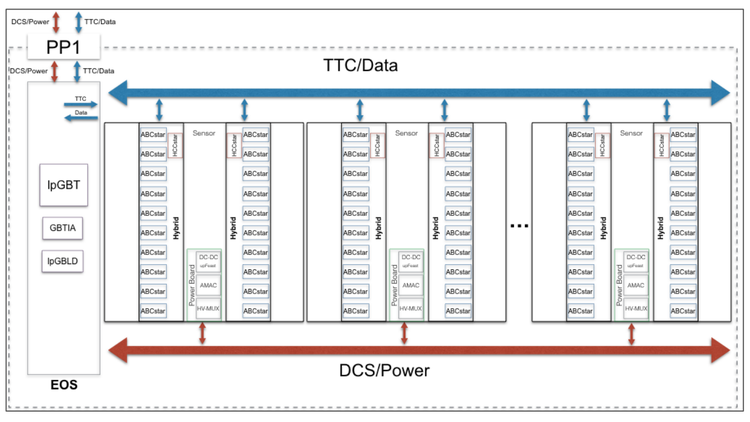
ITk BARREL STAVES



- **Staves** are the Barrel support structure for the modules.
- It hosts the common electrical, optical connections and cooling services.
- 28 Barrel modules on each stave (14 modules per side)
- Made up of a low-mass composite carbon fiber support structure
- End of Substructure (EoS) at one end of the Stave



Above: Schematic of the internal structure of the stave core, with the silicon sensors and ASICs .



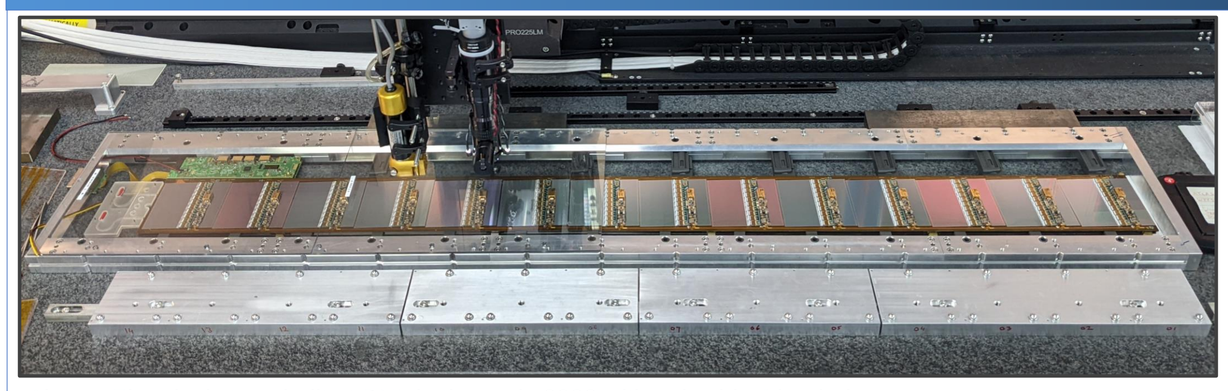
Left: Overview of the electronics components of the ITk Strip Detector located within the active area of the detector. Timing, Triggering and Control (TTC), power and DCS are interfaced to the stave/petal at the EoS card

ITk BARREL STAVES ASSEMBLY AT BNL

- In the assembly stage, modules are precisely glued on the stave-core while making the electrical connections at the same time.
- The Stave was assembled at BNL with the LS modules with ABCStarV1.
- Mounting was only done for the side J.
- Mounting on the side L will be done in May.

Right : Side J of LS stave being assembled at BNL.

STAVE TESTING SETUP

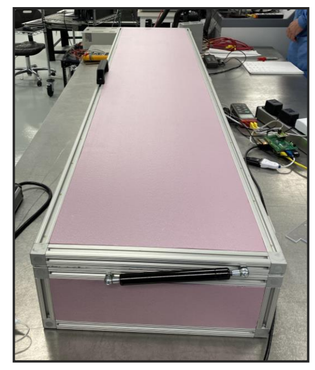


Above: Electrical stave built at BNL in the early 2022 with only side J loaded

- The Stave is tested in the coldbox which acts a Faraday cage with Relative Humidity and Temperature control.
- Cooling of the stave is done with the SPS chiller, ISEG SHR and Instek Power supply units for HV and LV respectively.

Data Acquisition

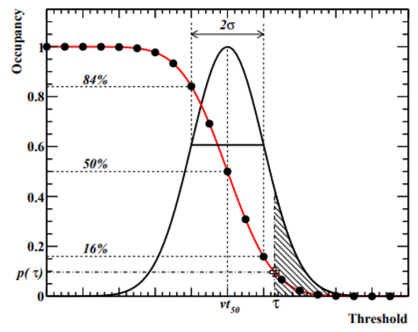
- The EoS hosts the **Low Power Giga Bit Transceiver** (lpGBT), a radiation tolerant ASIC that is used to implement multipurpose high speed bidirectional optical links between the DAQ (Genesys or FELIX) and the front-end ASICs.
- The data from the lpGBT is decoded at the DAQ, which is then passed on to the DAQ software(ITSDAQ or YARR) for analysis.



Above: Stave Coldbox

Front-End Characterization

- When a particle passes through the sensor, signal from the strips is transmitted to the front-end ASICs.
- **Strobe Delay** is used to scans over the possible delay values of charge injection with respect to the system clock.
- **Response Curve** is used to measure the response of the front end (in mV or DAC counts) to the injection of a calibration charge. Output of varying the trim-DAC threshold is an S-curve for a given charge. Threshold at which Occupancy is 50% is called **vt50**. Standard deviation of the erf-fit to the S-Curve is the **Output Noise**. **Input Noise** is calculated from the **Chip-Gain** (slope of vt50 vs charge plot) and output noise for each charge variation.

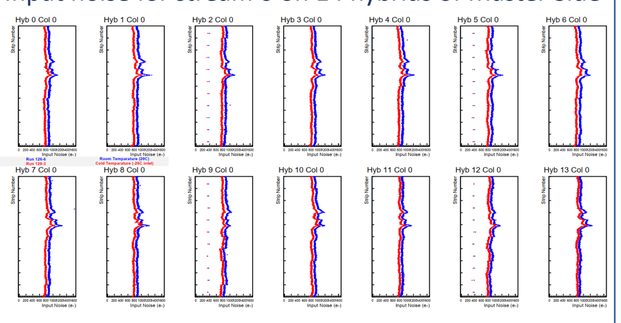


Above: Output at the trim-DAC for a given charge [2].

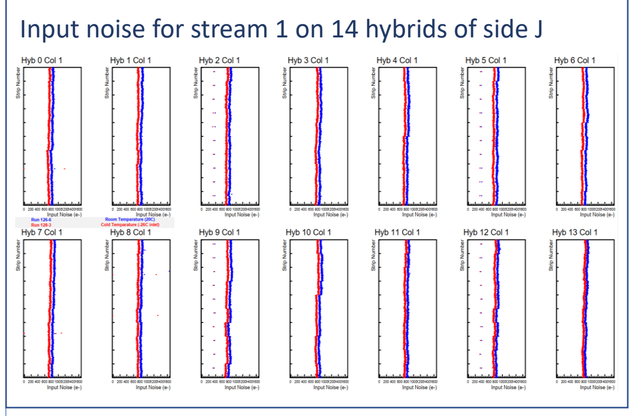
STAVE TESTING RESULTS

The stave was tested at T=20C and T=-26C (temperature of the coolant at stave inlet) and V bias of -400V. Uniform noise performance was observed for all the modules on the side J.

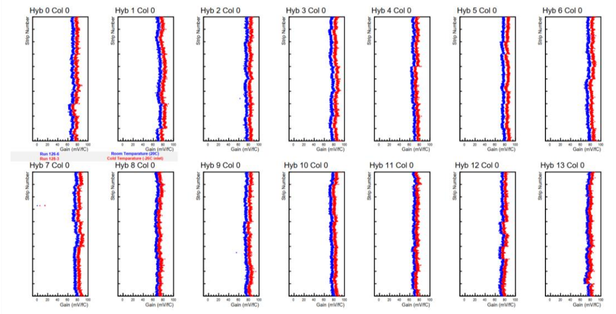
Input noise for stream 0 on 14 hybrids of Master Side



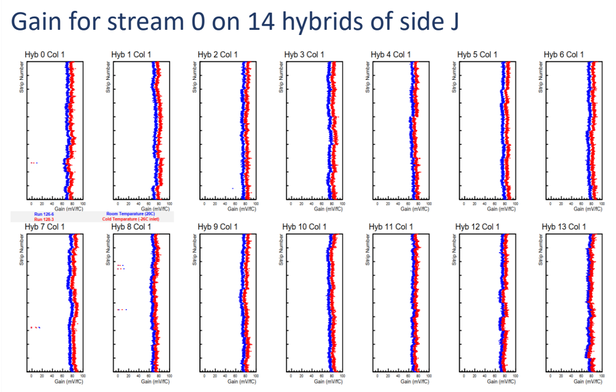
Input noise for stream 1 on 14 hybrids of side J



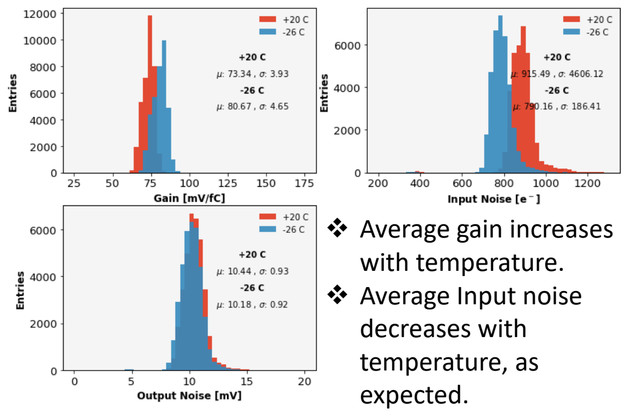
Gain for stream 0 on 14 hybrids of side J



Gain for stream 0 on 14 hybrids of side J



Variation with Temperature (all channels combined)



- Average gain increases with temperature.
- Average Input noise decreases with temperature, as expected.

CONCLUSION

- The noise is as expected (from other tests), indicating that the testing setup does not introduce any additional noise.
- The noise performance over the modules on the side J was uniform. No anomalous behavior was observed.
- The side J of the stave is loaded for now, the slave side will be loaded in May 2022.
- Once finished the stave will be shipped to CERN for further testing.

REFERENCE

[1] The ATLAS Collaboration, “Technical Design Report for the ATLAS Inner Tracker Strip Detector”, Tech. Rep. CERN-LHCC-2017-005, ATLAS-TDR-025, CERN, 2017.

[2] The ATLAS Collaboration, “Electrical results of double-sided silicon strip modules for the ATLAS Upgrade Strip Tracker”, ATL-UPGRADE-PUB-2012-002

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