PisaMeeting2021 - La Biodola, Elba, 22-28 May 2022

The DAQPATH readout system of the Serenity boards for the CMS Phase-II Upgrade

Guido Magazzù, Paolo Prosperi

INFN, Sezione di Pisa

The Serenity boards are ATCA custom boards used in the readout of the CMS detectors in the High Luminosity LHC upgrade. Each board can handle up to 144 optical input links (up to 25Gb/s each) and supports up to two high-performance FPGAs. In certain applications the Serenity board is required to aggregate raw events (FE data) from the detector on every L1 accept and route this event fragment to the central DAQ system. The architecture and behaviour of the DAQPATH firmware that collects and merges FE data and manages their transmission to the DAQ system over output optical 25Gb/s links are here described.

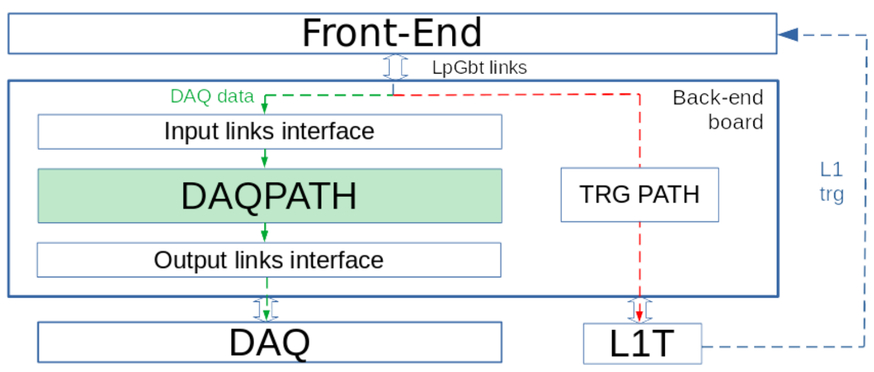


Fig.1 - FE data management in BE boards

For detector-facing Serenity boards, DAQ data from the FE links are received upon every L1 accept and decoded by FE interface blocks. DAQ data packets and associated information are temporarily stored into 3 buffers per channel. When all input buffers are not-empty, the main FSM that controls the token ring architecture of the DAQPATH starts the sequential readout of the input buffers and merges data from them into packets that feed the 25 Gb/s output link interface. The DAQPATH could also manage the transmission to the DAQ system of trigger data temporarily stored in local buffers and associated to the incoming L1 trigger.

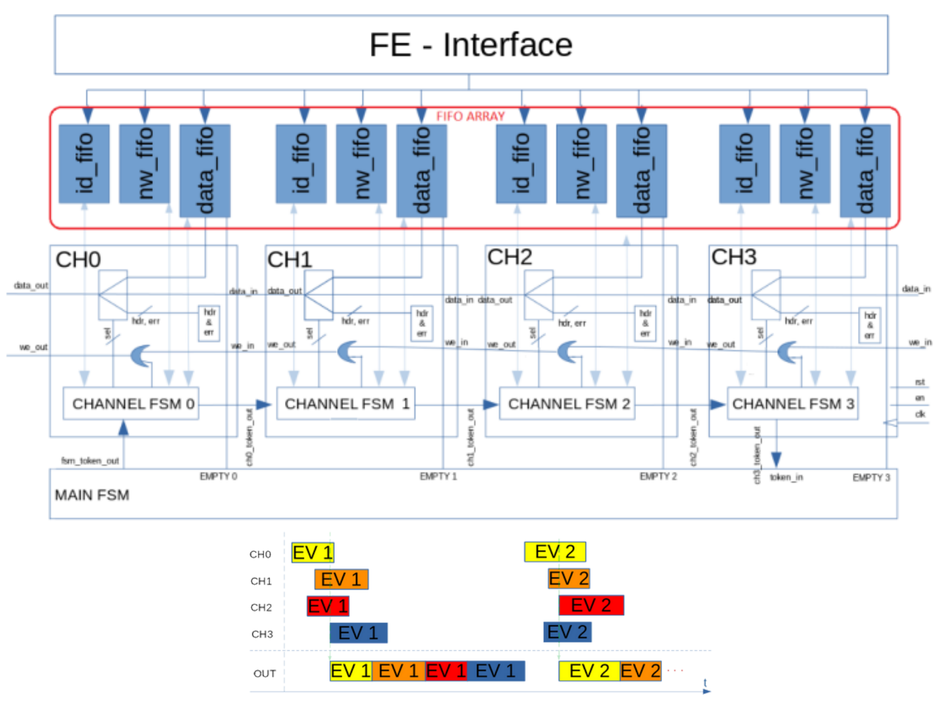


Fig.2 - DAQPATH architecture and data timing

The DAQPATH system has a modular and parametric structure: each DAQPATH module feeds one output link with data from a programmable number of input channels, that can be organized in groups and pipelined to meet timing requirements.

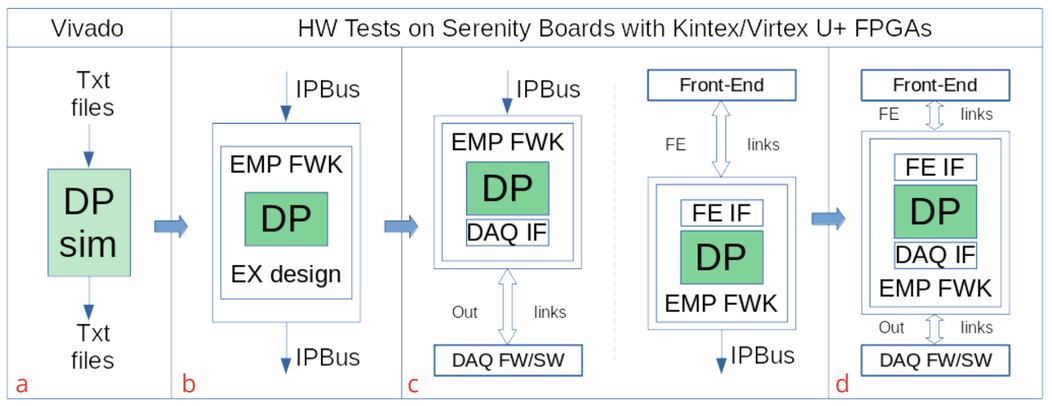
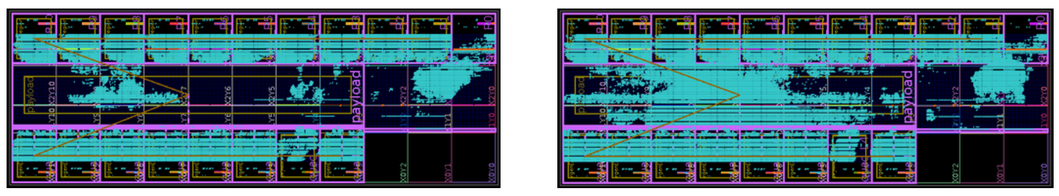


Fig.3 - Design validation/development flow

A first version of the DAQPATH FW (v1.0) has been validated with functional simulations in Vivado (3a) and hardware tests on Serenity boards with Xilinx Ultrascale+ FPGAs where the core logic, including the DAQPATH, runs at a 360MHz clock frequency. Hardware tests used IPBus buffers (i.e FIFOs accessible via IPBus protocol - 3b). Tests with input data from FE modules to IPBus output buffers and with data from IPBus input buffers to DAQ boards (3c) are on-going. Full chain tests (i.e. data from FE to DAQ - 3d) are forseen in the near future.
The DAQPATH firmware (v1.0) with example designs will be available soon as a tool-kit for users within EMP framework official repository.



4 channels (950 CLBs) **32 channels (5950 CLBs)**

Fig.4 - Floorplans including DAQPATH firmware implemented on a Kintex Ultrascale+ device KU15P