FEEM summary

Architecture

Distributed over two submodules: Primary (PRIM) and Auxiliary (AUX) Modules due to:

- Isolate Digital/power areas from analogue part
- Long path for analogue trace => isolated from possible sources of noise
- Encased into a metal casing for protection and for attaching to the SIPMs

Very compact form factor due to SCT Camera requirements: 274 mm x 46 mm for each submodule

Highly complex PCB: 14 layers, blind and buried vias
64 analogue channels (32+32 CHs)

T5TEA chip for triggering task

TARGET-C chip :1 GSa/s, 10 bits effective

Handles preamplifier (SMART chip) for SiPM

Prototype main goals:

- Demonstrate the performances of new FEEM: noise, distortion, reliability etc.
- Preparing the next production of the FEEMs

Conclusion

First prototypes available and their will be test in summer 2022

At the end of august 2022 result on the prototype will be issued

Beginning of autumn 2022 first bunch of FEEMS

End of 2022 full production (200 FEEMs)will be expected to be delivered