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Front End Electronics Module Design for the Schwarzschild-Couder Telescope (SCT) Camera

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Abstract:

The future ground-based gamma-ray observatory Cherenkov Telescope Array will feature multiple types of imaging atmospheric Cherenkov telescopes, each with thousands of pixels. The Schwarzschild-Couder Telescope has been proposed as medium-sized telescope within this large project. It is expected to provide a better field of view and image resolution compared to the traditional single mirror optics. An initial prototype camera equipped with 1600 pixels (out of the 11328 total pixels) was installed in 2018. A major upgrade is planned to fully equip the telescope camera with improved SiPM sensors and a new Front End Electronics Module, devoted to reading, sampling and handling the data coming from the pixels. To be affordable, camera concepts for these telescopes have to feature low cost per channel and at the same time meet the requirements for CTA in order to achieve the desired scientific goals.
One of the crucial points is the design of electronics devoted to reading, sampling and handling the data coming from the pixels. We present a new design board (called Front End Electronics module), equipped with TeV Array Readout with GSample/s sampling and Event Trigger chip. This is an application-specific integrated circuit designed to read out fast analog signals with a sampling frequency typically 1 GSample/s. The new Front End Electronics module houses four TARGET chips and a Xilinx Artix7 FPGA, devoted to set up the TARGET chips and the circuitry on board. Also, it is designed to be connected to the main backplane and uses high-speed serial links, such as Gbit Ethernet, to manage and send digitized data retrieved from the TARGET chips. The board is also designed to house or communicate with an external ASIC for the pre-amplification of the input analog signals that shapes the signals to set the correct DC-offset and amplification factor.

Introduction

One of the most effective techniques to detect gamma rays at very high energies is the imaging of Cherenkov light from atmospheric showers. This field is soon to be revolutionized by the advent of the Cherenkov Telescope Array (CTA), which is meant to improve the sensitivity by about an order of magnitude, to extend the energy range, from a few tens of GeV to above 100 TeV, with enhanced angular and energy resolutions over existing imaging atmospheric Cherenkov telescope (IACT) systems.

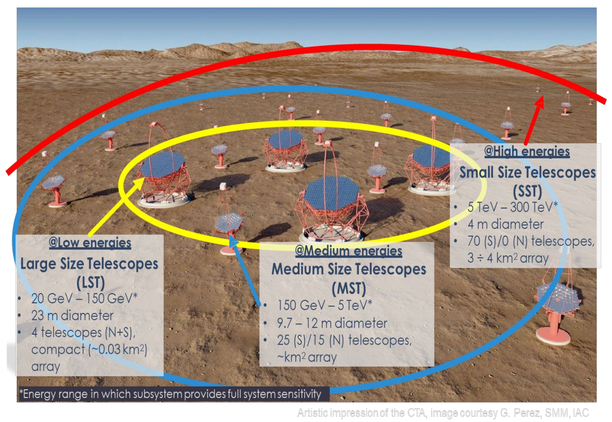
A large number of telescopes required to reach the performance aimed at for CTA calls for innovative ways to reduce their cost. The Schwarzschild-Couder Telescope (SCT) [3] is one of the proposed solutions as medium-sized telescope that offers dual-mirror optics along with a compact camera design enabled by modern photosensors like SiPM sensors. This helps to bring down the costs by reducing the area that needs to be instrumented with photosensors to achieve the desired field of view.

One of the most important features is the analog to digital sampling and read-out of the signal coming from the photosensors. For this aim, a new Front End Electronics Module FEEM has been developed to house an ASIC, named TARGET, especially developed for this scope.

TARGET is the acronym of TeV Array Readout Electronics with GSamples/s sampling and Event Trigger. This is an application-specific integrated circuit (ASIC) designed to read out fast analog signals with a sampling frequency typically 1 GSample/s. In its latest version, TARGET-C, it is devoted to the sampling, storing and digitization phases by means of a Wilkinson Analog to Digital conversion (ADC). Due to a large number of channels (16 channels), low cost per channel, a deep buffer for trigger latency and window-selected read-out, the TARGET-C is ideally suited for developing readout systems with thousands of channels.

The triggering task is performed by a specific ASIC (T5TEA), which implements the analog sum of the input signals in four independent groups of four adjacent channels, comparing the sums to a user-defined threshold and providing four differential outputs.

The FEEM (Front End Electronics module) is capable of reading 64 photodetector pixels and connected to a backplane via Gbit Ethernet, to manage data retrieved from the target chips.



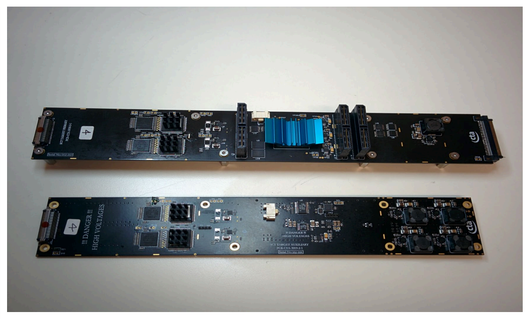
Artistic impression of the CTA, image courtesy G. Perez – SMM, IAC

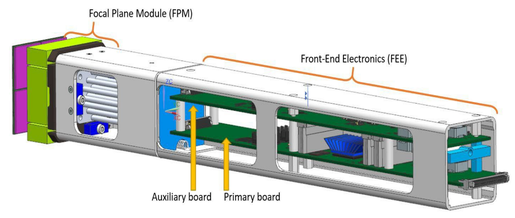
II. FRONT END ELECTRONICS MODULE: ARCHITECTURE AND STRATEGY

The new FEE Module is divided into two submodules, called Primary (PRIM) and Auxiliary (AUX). Each one houses two TARGET-C and two T5TEA, for a total of 64 channels that can be read simultaneously (32 channels per submodule). The submodules are stacked up together and connected via three connectors, as reported on the right in the figure above. The underlying strategy to use two submodules is for having a well-separated area for analogue and digital/power circuitries. In addition, the path of each analogue channel is very long and so there is the possibility of picking up noise. Last, the dimension of a single submodule does not have to exceed 274 mm length and 46 mm width, for having a compact camera to install into the telescope. Hence, a combined module of two submodules is necessary to comply with all requirements.

Once that the submodules are stacked up, they are encapsulated in a metallic cage that is used as a structured to defend the submodules and to attach the photosensor matrix.

On the right, in the figure below shows the FEE module into the metallic cage. The entire block represents a single slice of SCT camera.





III. PRIMARY SUBMODULE and AUXILIARY SUBMODULE

Primary submodule

A schematic block of the PRIM submodule is reported on the image below in the top part. PRIM submodule houses two T5TEA and two TARGET-C chips, so that up to 32 analog channels can be digitized and stored in parallel.

A Xilinx Artix-7 FPGA (XC7A100T-FGG484) is embedded and is responsible to set-up the TARGET-C and T5TEA chips that require a complex setting operation to be ready to trigger (T5TEA), sample and store (TARGET-C) data coming from the analog connector. Furthermore, the FPGA retrieves the digitized data and format and send them – via Gbit Ethernet, through the backplane connector, that is used to insert the single FEE module in the main backplane that gathers all the data coming from all the FEE modules.

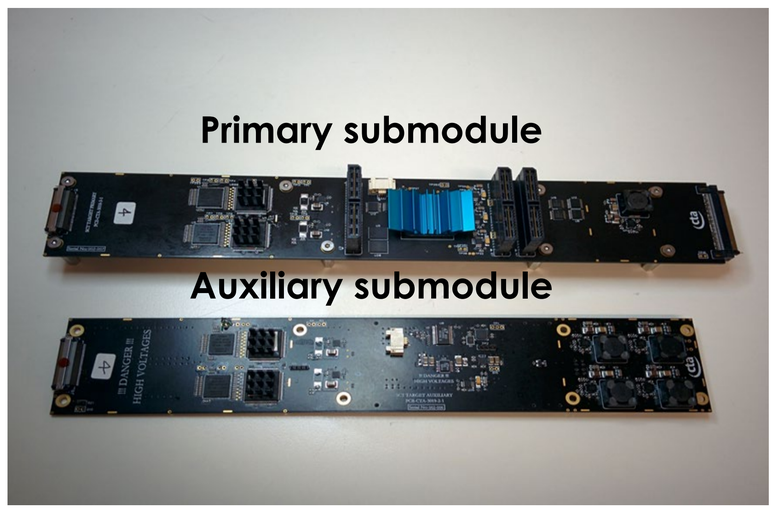
Moreover, FPGA interfaces a uC – devoted to manage a Peltier cell housed in the AUX submodule – to cool the SiPM and stabilize the temperature around 25 degree.

Auxiliary submodule

A schematic block of the AUX submodule is reported on the image below in the bot part. AUX submodule houses two T5TEA and two TARGET-C chips, so that up to 32 analog channels can be digitized and stored in parallel.

On the bottom side, three connectors are placed to stack up the AUX submodule with the PRIM one.

On the top right side, there are all the circuitries devoted to the power supplies; this area is well-isolated from all the area (on the left) that is interested by the analogue paths.



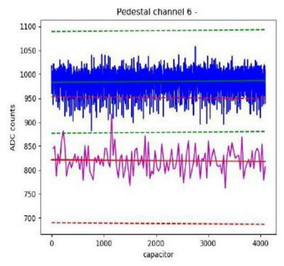
FEEM NOISE PERFORMACES

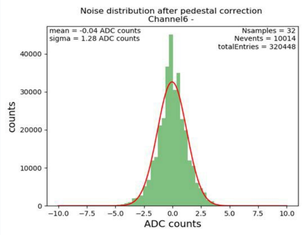
Measurement is done in absence of input signal, the named «pedestal»

For each sampling capacitor a distribution is made and the □ is extracted

The overall distribution shows a very small noise contribution of **σ = 1.3 ADC counts** only

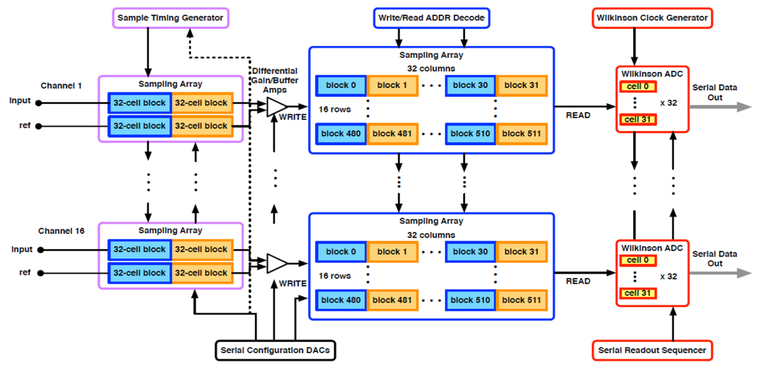
No dependence on the capacitor ID is evident





TARGET-C ASIC designed for CTA by G. Varner (univ. of Hawaii)
Input voltage range: 0.6 – 2.1 V
Noise: 0.6 – 1.0 mV
Dynamic range: 10.5 – 11.2 bits

TARGET-C



Conclusion

A new FEE module has been designed and is compliant with SCT camera. The first test phase will be executed in the laboratory, setting up the full chain composed by a photosensor matrix of 64 pixels and a FEE module. The FEE module will be interfaced via Gbit Ethernet on a special adapter board that replicates the backplane. The first prototypes have been tested in the middle of April 2019 and respect the SCT requirements. In the March 2022, a second set of prototypes will be tested, while the full production will be delivered within July 2022 and installed in the SCT camera within the end of 2022 and the beginning of 2023.