RATIONALE
Coordinating firmware development among many international collaborators is becoming a very widespread problem.

Guaranteeing firmware synthesis with Place and Route reproducibility and assuring traceability of binary files is paramount.

Hog tackles these issues by exploiting advanced git features and integrating itself with HDL IDEs: Xilinx Vivado, Xilinx ISE (planAhead) or Intel Quartus.

The integration with these tools intends to reduce as much as possible useless overhead work for the developers.

WHAT IS HOG?
Hog is a set of Tcl and Shell scripts plus a suitable methodology to handle HDL designs in a GitLab repository.

Hog is included as a submodule in the HDL repository and allows developers to create the Vivado/PlanAhead/Quartus project(s) locally and synthesise/implement it or start working.

HOG ON YOUR MACHINE
- a simple and effective way to maintain HDL code on git
- automatically integrated into Xilinx/Intel project without additional effort
- ensure the code was not modified before building binary files
- ensure traceability of binary files (even if produced locally)
- multi-platform compatibility, working both with Windows and Linux
- compatibility and support for IPBus
- automatic creation of Sigasi project

HOG CONTINUOUS INTEGRATION ON GITLAB
- YAML files to run continuous integration in your GitLab repository
- Automatic tag creation for versioning
- Automatic GitLab release creation with and binary files
  - including timing
  - utilisation reports
- Automatic changelog in the release note parsed from commit messages
- Possibility to store the output binary files on EOS

Are you an FPGA developer? Are you a Git fan?
Get in touch with Davide, Francesco, Nicolo!