Motivations

Simulation of a VBF H → ττ in 200 pile-up pp collisions

Conditions at HL-LHC very challenging
→ at the edge of tracker performances

Spread of ~180 ps in time collisions
→ slices of 35 ps will reject a factor of 5 more pile-up

= With 35 ps time resolution, instances of vertex merging are reduced from 15% in space to 1% in space-time, as in LHC operation

Starting from Run 4 (2029)[1][2] CMS will be equipped with a MIP Timing Detector[2]
The Endcap component will be equipped with ~ 14 m² of Low-Gain Avalanche Diodes[3]

Sensors

Low-Gain Avalanche Diodes (LGADs)
Impact ionisation occurs when E_{E_max} > E_{τ} > 25 kV/m
In LGADs the E_{E_max} is above E_{τ} for short distance well controlled by E\text{loss}
With an active thickness of ~ 50 μm, timing resolution is of ~ 30ps[4]

High collected charge with fluxence from FBK sensors

Uniform timing resolution of HPK sensors
→ ETL sensor market survey almost complete
→ ETL sensor design choice in September 2023
→ ETL sensor production completion expected by mid-2025

Electronics

Timeline

ETROC0 – Submission Dec. 2018
→ single analog channel

ETROC1 – Submission Aug. 2019
→ 4x4 pixel array with full front-end
→ TDC brand new design optimized for low power

ETROC2 – Submission Jul. 2022
→ 16x16 full size and functionality
→ H-tree clock distribution

ETROC3 – Submission Mar. 2024
→ pre-production chip

From beam tests at the FNAL facility

ETROC0: σ_t ~ 30 ps

ETROC1: σ_t ~ 42 – 46 ps

Integration

• ETL will be placed on the HGCAL nose
• Two disks for each endcap, on both sides
• Track resolution < 35 ps

Strong effort to combine inputs from studies into a complete detector design and layout
~ 8000 modules on 2 endcaps
~ 8M channels in total

⇒ The Endcap Timing Layer is expected to provide a timing resolution per track < 40 ps up to the end-of-lifetime in most of its volume

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References