Development of CoRDIA: an Imaging Detector for next-generation Photon Science X-ray Sources.

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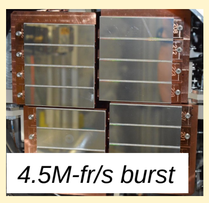
motivation



Photon Science Imagers available today

optimized for:
continuous readout
- up to a few k-frame/s
- typically used in: SRs, low-rep-rate FELs

SR becoming diffraction-limited

x100 brilliance
→ proportionally faster readout desirable

source upgrades

optimized for:
high-rep-rate FEL operation
- up to a few M-frame/s
- only for short imaging bursts

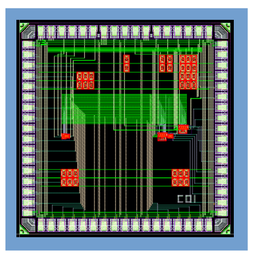
high-rep FELs considering CW operation mode

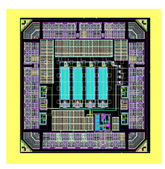
some reduction of burst rate, but no gap between trains
→ need continuous readout

common need for:
continuous readout
> 100kHz frame rate

prototypes

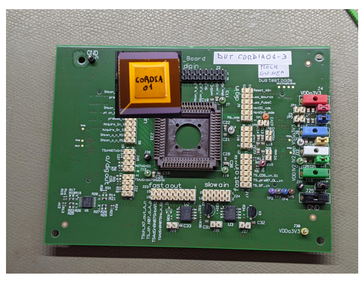
CoRDIA01 prototype: validation of Adaptive Gain circuit, CDS block, S/H to alternate the readout path between two readout sub-chains (to achieve continuous Write-Reading)

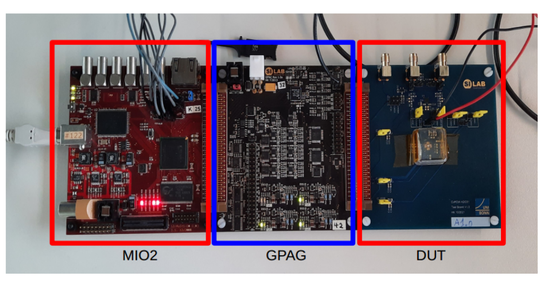


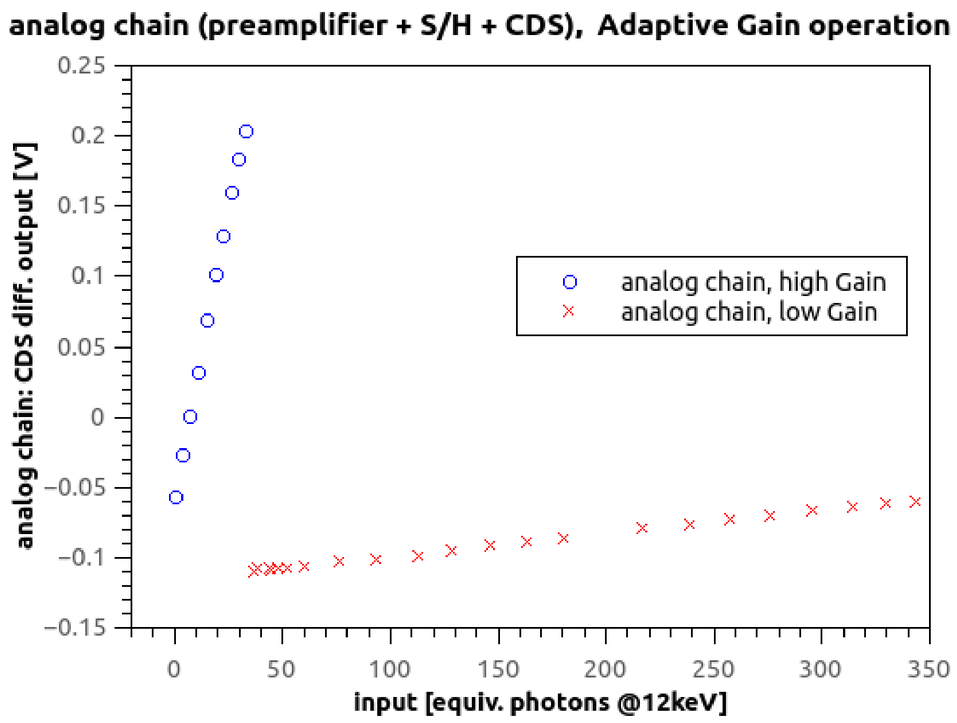


HSI_ADC01 prototype: evaluation of 4 ADC variants based on SAR architecture: exploring redundancy and switching options.

Multi-Project Wafer prototypes including basic circuital blocks have been manufactured in TSMC65nm technology for circuit validation and characterization. They are presently under test, so far confirming expectations.

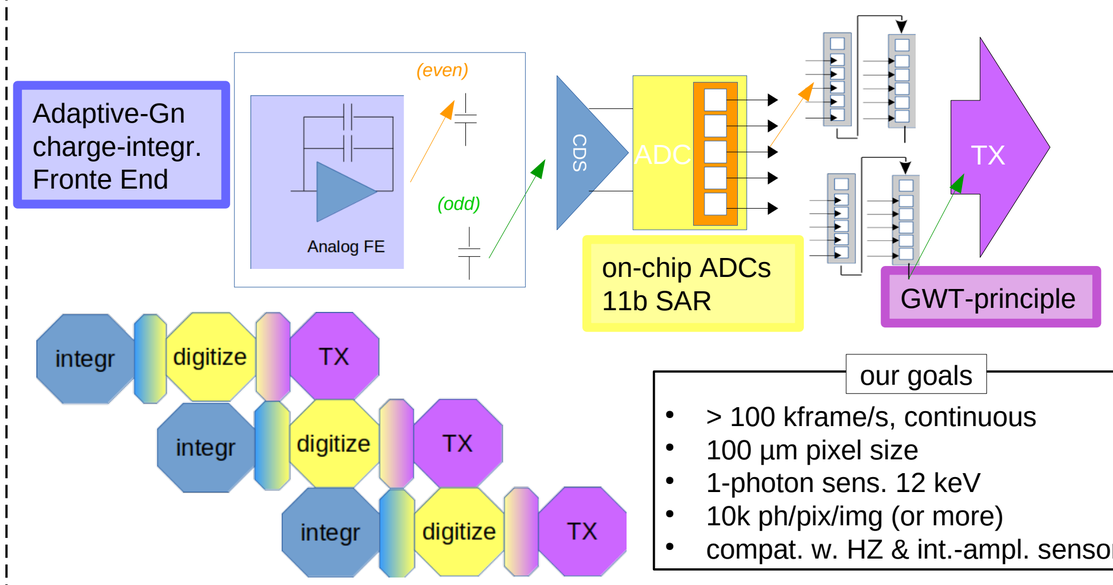






Analog Front-End: test of the Adaptive-Gain amplification circuit.
The system adaptively modulates the amplification of the preamplifier stage to the incoming photon flux. When exposed to a low flux, the system amplifies the input signal with a high Gain (steeper blue ramp) to minimize noise. When exposed to a high flux, the output drops, and the system amplification is reduced to a low Gain (shallower red ramp), thus avoiding saturation and extending the dynamic range.
In addition to the amplified analog value (shown above), the circuit provides a digital bit recording the high/low Gain modulation status, allowing correct evaluation of the input signal. The Gain modulation happens automatically and in real time, independently for each pixel and for each image.

COntinuous Readout Digitising Imager Array



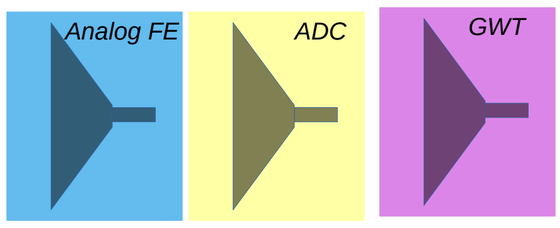
our goals
- > 100 kframe/s, continuous
- 100 µm pixel size
- 1-photon sens. 12 keV
- 10k ph/pix/img (or more)
- compat. w. HZ & int.-ampl. sensors

The detector adopts a 3-stage-pipeline structure, so that while incoming photons are integrated in a Adaptive Gain amplification stage (adapted from AGIPD detector), the former image is digitized on-chip (through 11bit Successive Approximation Register ADCs) and the image before that is read out (using the Gigabit Wireline Transmitter principle developed by Nikhef for Timepix4).
We plan to adopt a modular "superpixel" architecture, with one ADC digitizing 16 analog Front-Ends, and 128 ADCs (2k pixels) being streamed out by a GWT
The analog Front-End has been tested at a frame rate $>150\ kframe/s$

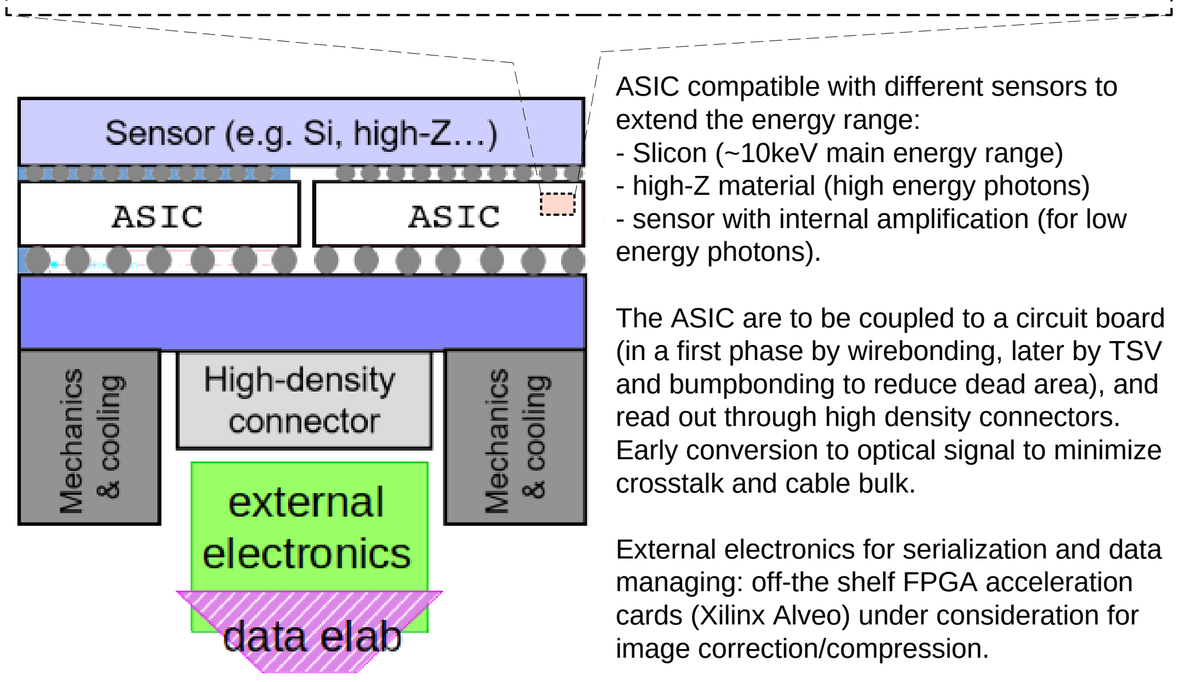
The ADC (serving 16 Front Ends) has been tested @2.5~3MS/s: $\frac{2.5\ MS/s}{16\ FE} > 150\ kframe/s$

The GWT functionality has been recently verified by Nikhef at 5.12MHz and above. We plan the use on a GWT for 128 ADC, each digitizing of a pixel value in less than 2 Bytes, and with a 66/64b encoding:

$$\frac{5.12\ GHz}{16\ bits * 128\ ADCs * 66/64} > 150\ kframe/s$$



Each of out pipeline stages has been verified to be able to operate above our frame-rate goal

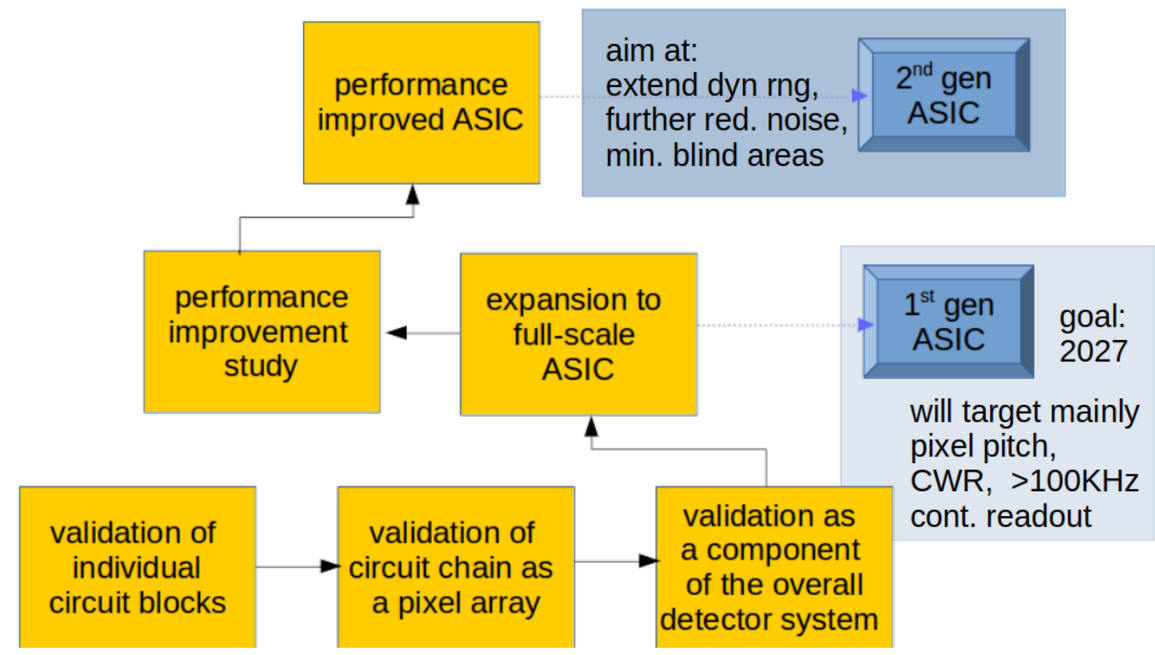


ASIC compatible with different sensors to extend the energy range:
- Silicon (~10keV main energy range)
- high-Z material (high energy photons)
- sensor with internal amplification (for low energy photons).

The ASIC are to be coupled to a circuit board (in a first phase by wirebonding, later by TSV and bumpbonding to reduce dead area), and read out through high density connectors. Early conversion to optical signal to minimize crosstalk and cable bulk.

External electronics for serialization and data managing: off-the shelf FPGA acceleration cards (Xilinx Alveo) under consideration for image correction/compression.

when can I have one?



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