

Contribution ID: 39 Type: Poster

## Demonstration System of the HGTD Peripheral Electronics Board (PEB) for ATLAS Phase II Upgrade

Friday, 27 May 2022 15:32 (1 minute)

The increase of the particle flux (pile-up) at the HL-LHC with instantaneous luminosities up to  $7.5\times10^34$  cm $^(-2)$  s $^(-1)$  will have a severe impact on the ATLAS detector reconstruction and trigger performance. The end-cap and forward region where the liquid Argon calorimeter has coarser granularity and the inner tracker has poorer momentum resolution will be particularly affected. A High Granularity Timing Detector (HGTD) will be installed in front of the LAr end-cap calorimeters for pile-up mitigation and luminosity measurement.

The HGTD is a novel detector introduced to augment the new all-silicon Inner Tracker, adding the capability to measure charged-particle trajectories in time as well as space. Two silicon-sensor double-sided layers will provide precision timing information for minimum-ionizing particles with a resolution as good as 30 ps per track. Readout cells with a size of 1.3 mm  $\times$  1.3 mm, lead to a highly granular detector with 3.7 million channels, which throw out a huge challenge to the readout electronics system taking the form of Peripheral Electronics Boards (PEB).

We developed a demonstration system of PEB to verify some uncertain aspects in advance. The demonstration system is designed as a flexible platform where we can perform many kinds of validations and tests, such as: exercise the data transmission of the critical versatile link (lpGBT + VTRx+), validate the feasibility of working with FELIX DAQ system, test the HGTD modules efficiently, etc. The demonstration system is actually a simplified version of PEB, small but complete. It has 2 uplinks both with the speed of 10.24Gbps, and 1 downlink with the speed of 2.56Gbps. Also, it adopts the modular design, which makes the ASICs replaceable.

We performed the test of the demonstration system, and it worked as expected. The Bit Error Rates (BER) for both uplinks and downlink are less than  $10^{-14}$ .

## Collaboration

ATLAS

Primary author: ATLAS COLLABORATIONN, To\_be\_selected

**Presenter:** HAN, Liangliang (Nanjing University)

Session Classification: Front End, Trigger, DAQ and Data Mangement - Poster session