Frontier Detectors for Frontier Physics
15th Pisa meeting on advanced detectors
La Biodola • Isola d'Elba • Italy
22 - 28 May, 2022

# Demonstration System of the HGTD Peripheral Electronics Board (PEB) for ATLAS Phase II Upgrade

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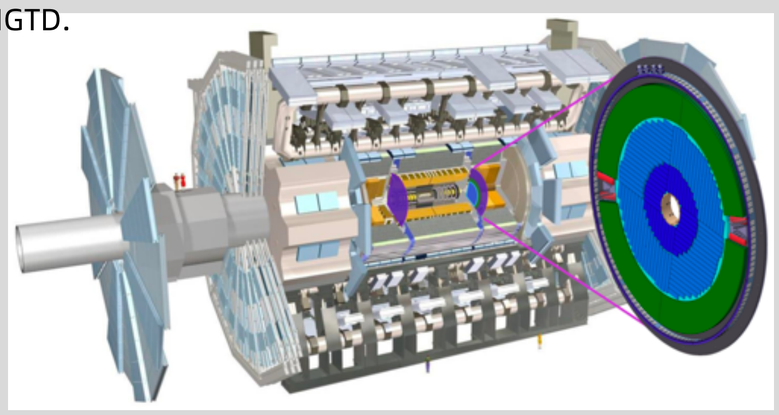
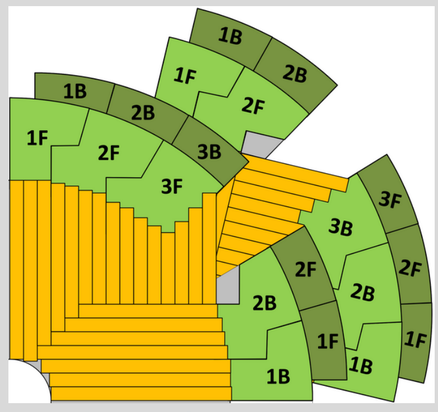
## Motivation

In order to mitigate the pileup effects caused by the increasing instantaneous luminosity of proton-proton collisions at the HL-LHC, a High-Granularity Timing Detector (HGTD) has been proposed for the ATLAS Phase-II upgrade. There will be several types of Peripheral Electronics Boards (PEB), which will be installed in the peripheral regions of the HGTD.



HGTD location in ATLAS detector



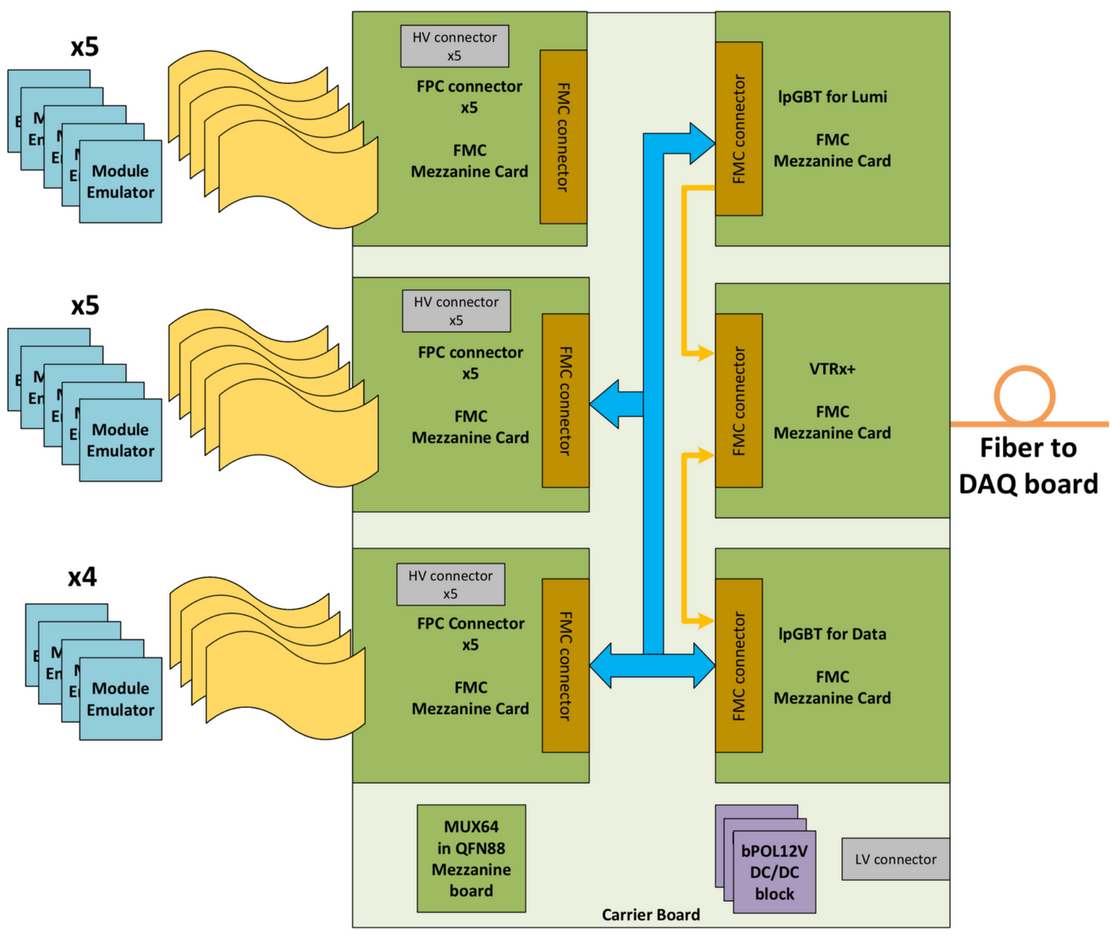

PEB layout in one quadrant

Prior to the PEB prototype, a PEB demonstration system has been developed to:

- Validate the versatile links (lpGBT + VTRx+)
- Validate PCB manufacturing techniques and some mechanical parameters
- Help to debug and develop the DAQ system
- Test many key chips/parts
- Exercise the assembly and integration procedure

## Demonstration system design

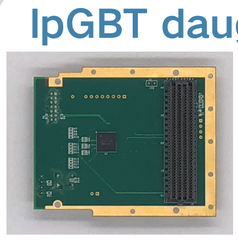
### Overview




The PEB demonstration system is actually a simplified version of PEB prototype, and it uses the key ASICs like lpGBT, VTRx+, bPOL12V, Mux64. Design highlights:

- **Modular design makes ASICs replaceable**: Those key ASICs are mounted on different kinds of daughter boards while the PEB demonstration itself serves as a carrier board.
- **Compatible with commercial ASICs**: In case those key ASICs are not available, we can still operate the demonstration system with some commercial ASICs.
- **Dedicated wire routing between modules and lpGBTs**: This kind of wire routing scheme can help us verify different lpGBT data rate settings.
- **Support up to 14 module emulators and 2 lpGBTs:** one lpGBT for time data (TX@10.24Gbps, RX@2.56Gbps), one lpGBT for Lumi data(TX@10.24Gbps)

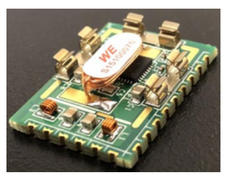
### lpGBT daughter board



Compatible with lpGBT v0 and v1.

Use POFV tech

### bPOL12V power block

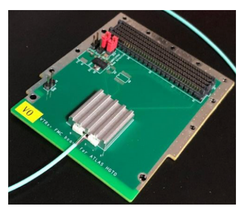


Shielding case

Customised inductor

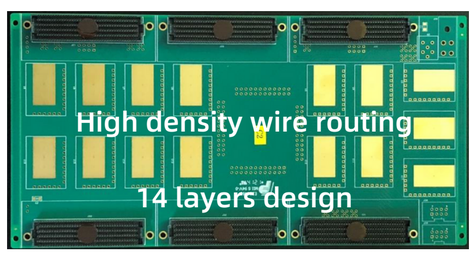
10 Ohm resistor between Cboot and BOOTS

### VTRx+ daughter board



Heat sink to help VTRx+ dissipate heat, and mitigate related side effect

### Carrier board

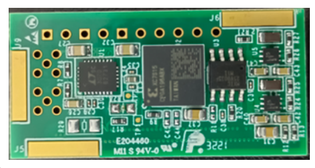



### MUX64 daughter board

QFN88 package

Pass aging test

Pass NIEL irradiation

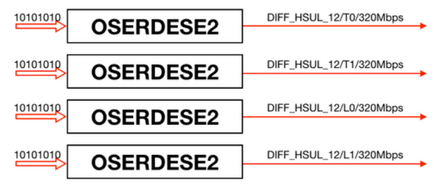


Module emulator

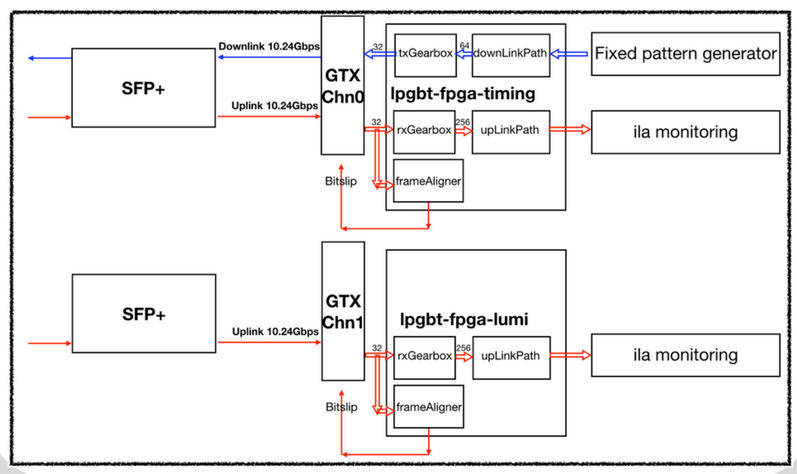
## Firmware development

Firmware is prepared for both the module emulator and the microTCA DAQ board attached right after the fiber.

- Firmware on module emulator can generate pseudo signals (fixed pattern) with a specific transmission speed.

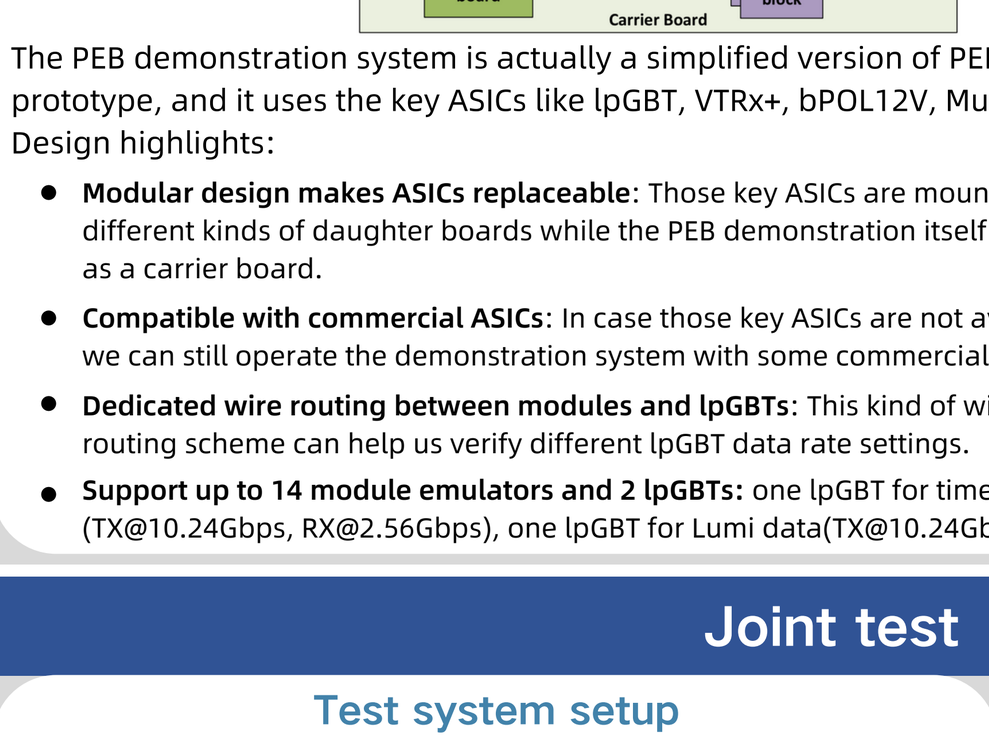



- Firmware on microTCA DAQ board is mainly used to decode and monitor the data from lpGBT.




## Joint test

### Test system setup




In the setup, all boards are integrated together into a functional system. 3 FH26 connector boards, 15 power blocks, 2 lpGBTs and 1 VTRx+ are mounted on the carrier board. uFC FPGA board used as DAQ board.

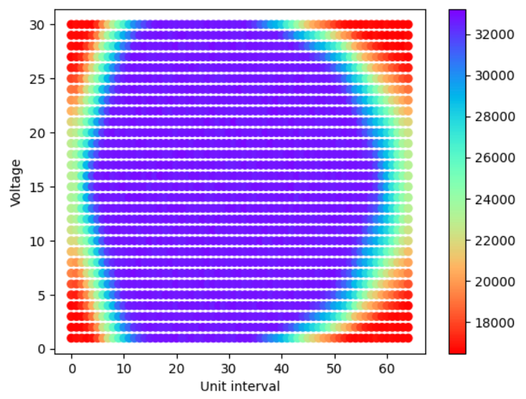
### Results

With the test system setup, the versatile link was successfully established. Meanwhile, many features of lpGBT are configured and tested.

- lpGBT clock test.
- Readout of lpGBT ADCs and GPIOs
- lpGBT I2C slave test
- Connectivity test (signal&power)

All above tests successful

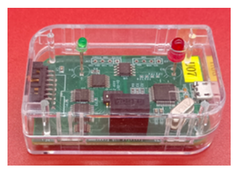
Eye diagram of VL+ downlink (2.56Gbps) measured by the EOM circuit of lpGBT

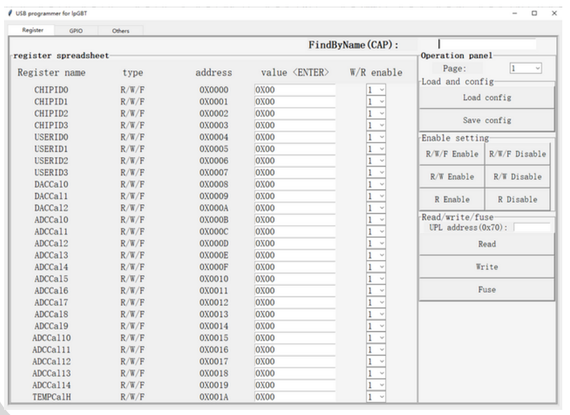



## lpGBT configuration toolkit

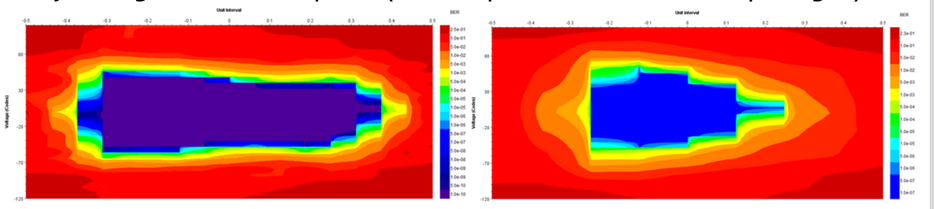
Dedicated configuration toolkit was developed to configure the lpGBT through its I2C slave interface. The toolkit includes:

- A programmer board UPL
- Graphic user interface(GUI)
- Configuration scripts






Eye diagram of VL+ uplink (5.12Gbps/left and 10.24Gbps/right)



BERT: better than 10^-14 for both uplink and downlink

## Conclusion and outlook

With the demonstration system, we have validated the feasibility of the versatile links (uplink && downlink), some PCB manufacturing techniques and mechanical parameters. In the meantime, many related tests are also carried out with the system, e.g. FE-module test, DAQ system development. So far, four sets of the system have been distributed to 4 institutions, where they are used to perform many related studies and tests.

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