Motivation

In order to mitigate the pileup effects caused by the increasing instantaneous luminosity of proton-proton collisions at the HL-LHC, a High-Granularity Timing Detector (HGTD) has been proposed for the ATLAS Phase-II upgrade. There will be several types of Peripheral Electronics Boards (PEB), which will be installed in the peripheral regions of the HGTD.

Demonstration system design

The PEB demonstration system is actually a simplified version of PEB prototype, and it uses the key ASICs like lpGBT, VTRx+, bPOL12V, Mux64. Design highlights:

- Modular design makes ASICs replaceable: Those key ASICs are mounted on different kinds of daughter boards while the PEB demonstration itself serves as a carrier board.
- Compatible with commercial ASICs: In case those key ASICs are not available, we can still operate the demonstration system with some commercial ASICs.
- Dedicated wire routing between modules and lpGBTs: This kind of wire routing scheme can help us verify different lpGBT data rate settings.
- Support up to 14 module emulators and 2 lpGBTs: one lpGBT for time data (TX@10.24Gbps, RX@2.56Gbps), one lpGBT for Lumi data (TX@10.24Gbps, RX@5.12Gbps), one UPL for Logi (TX@8.1Gbps, RX@16Gbps, RX@4.9Gbps).

lpGBT daughter board

- Compatible with lpGBT v0 and v1.
- Use POFV tech.

bPOL12V power block

- Shielding case
- Customized inductor 10 Ohm resistor between Cboot and BOOTS.

VTRx+ daughter board

- Heat sink to help VTRx+ dissipate heat, and mitigate related side effect.

MUX64 daughter board

- QFN88 package
- Pass aging test
- Pass NIEL irradiation.

Module emulator

Joint test

Test system setup

In the setup, all boards are integrated together into a functional system. 3 FH26 connector boards, 15 power blocks, 2 lpGBTs and 1 VTRx+ are mounted on the carrier board. uFC FPGA board used as DAQ board.

Results

With the test system setup, the versatile link was successfully established. Meanwhile, many features of lpGBT are configured and tested.

- lpGBT clock test.
- Readout of lpGBT ADCs and GPIOs
- lpGBT I2C slave test
- Connectivity test (signal&power)

All above tests successful

Eye diagram of VL+ downlink (2.56Gbps)

Eye diagram of VL+ uplink (5.12Gbps/left and 10.24Gbps/right)

BERT: better than $10^{-14}$ for both uplink and downlink.

Conclusion and outlook

With the demonstration system, we have validated the feasibility of the versatile links (uplink & downlink), some PCB manufacturing techniques and mechanical parameters. In the meantime, many related tests are also carried out with the system, e.g. FE-module test, DAQ system development. So far, four sets of the system have been distributed to 4 institutions, where they are used to perform many related studies and tests.

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