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Development of Readout Electronics for the CMS ME0 Muon Detector

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In the High Luminosity era, the Large Hadron Collider (LHC) will be upgraded to deliver instantaneous luminosities up to 5×10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$, five times more than the original design value. In order to maintain performance of the Compact Muon Solenoid (CMS) experiment under these conditions, ME0 is one of the three new muon sub-detectors being added, along with GE1/1 and GE2/1, which use the triple Gas Electron Multiplier (GEM) technology. ME0 is designed to cover the forward region of 2.0<$|\eta|$<2.8, thus improving muon reconstruction at high background rates by supplementing other overlapping muon subsystems up to $|\eta|$=2.4, while also extending the acceptance for the first time to $|\eta|$=2.8. The readout electronics for ME0 must be designed to deal with high data rates and be sufficiently radiation hard to operate so close to the beamline. The Optohybrid (OH) board for ME0, which reads out data from the front-end VFAT3b ASICs, has therefore been designed to operate without an FPGA (unlike GE1/1 and GE2/1) to ensure radiation hardness. It will use the radiation-hard CERN designed lpGBT ASIC and high bandwidth optical links at 10.24 Gb/s, thus also providing the benefit of high data rates. The backend system will be based on the ATCA standard. The design and development status of the readout electronics for ME0 will be presented, along with recent results from integration tests performed using the first prototypes.

Collaboration

Compact Muon Solenoid (CMS)

Primary author: DATTA, Abhisek (University of California, Los Angeles)

Presenter: DATTA, Abhisek (University of California, Los Angeles)

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