Development of Readout Electronics for the CMS ME0 Muon Detector

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PM 2021 - 15th Pisa Meeting on Advanced Detectors – Edition 2022

Introduction

ME0 Detector:

- In each endcap, arranged in a wide planar ring with inner radius ≈ 0.6 m and outer radius ≈ 1.5 m, centered on beamline
- 6-layer triple Gas Electron Multiplier (GEM) stacks
- Each chamber covering $\Delta\varphi = 20^o$ and $\Delta\eta = 0.8$ (divided into 8 partitions in η)
- 384 radial strips in each η partition
- ME0 electronics designed to deal with high data rates and be radiation hard

Motivation:

- Improve muon reconstruction at high luminosity (HL-LHC) by supplementing other muon subsystems till $|\eta| = 2.4$
- Extend muon acceptance to $|\eta| = 2.8$

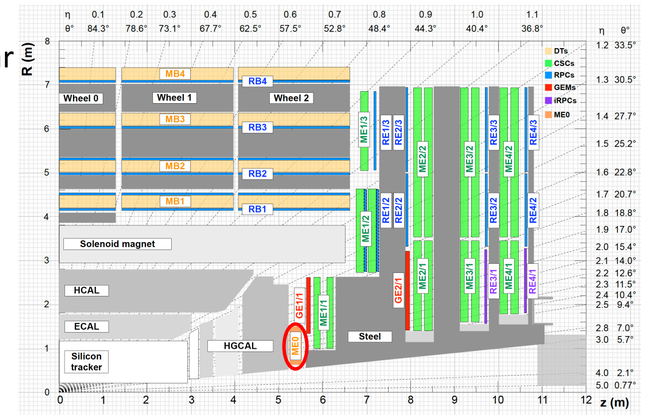

Figure 1: Quadrant of CMS experiment highlighting ME0 ($2.0 < |\eta| < 2.8$)

CMS Collaboration, The Phase-2 Upgrade of the CMS Muon Detectors, Technical Report CERN-LHCC-2017-012, CMS-TDR-016 (2017)

ME0 Electronics Overview

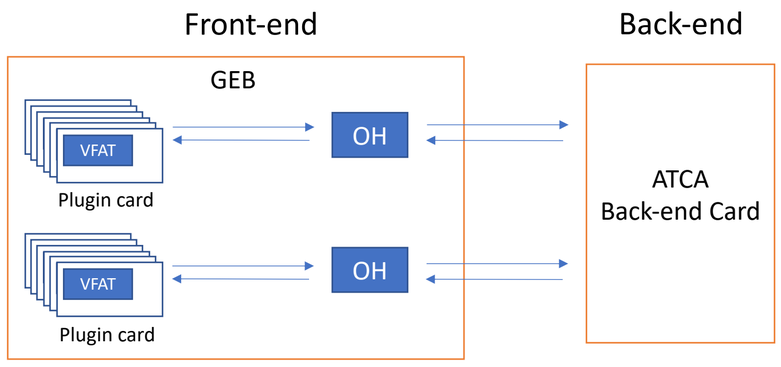

Figure 2: Block diagram for ME0 front-end and back-end electronics

- 128 strips per VFAT plugin card
- 6 Plugin cards per OH
- 2 OHs per GEB
- 2 GEBs per layer
- 6 layers per stack
- 18 stacks per endcap
- 2 endcaps in CMS

GEB: GEM Electronic Board
OH: Optohybrid

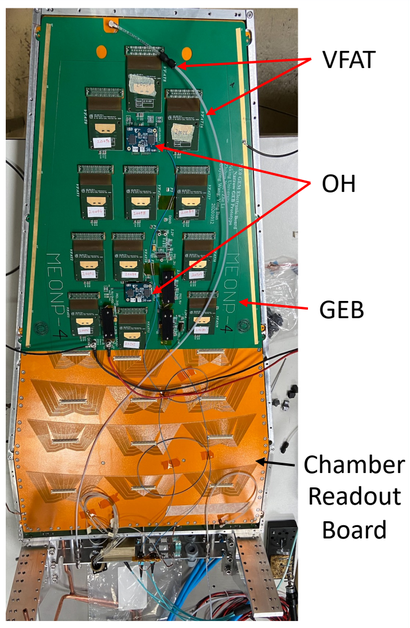

Figure 3: Picture of ME0 front-end electronics

Front-end Chips and GEM Electronic Board

VFAT3b (by INFN Bari, ULB) is the front-end chip to read out the strips on ME0 (also used in GE1/1, GE2/1):

- 128 channel chip, reads charges from the sensor
- Provide tracking and trigger data
- Time resolution of less than 7.5 ns (with detector)
- Radiation resistant

VFAT3b packaged in a plugin card with protection circuit

Current Status and Plans:

- VFAT3b plugin card prototype produced and successfully tested with ME0 GEB and OH
- All wafers for ME0 produced, packaging expected in 2022

GEB (by PKU) is fixed to the chamber readout board to which the VFATs are connected:

- Responsible for routing the signals from the VFATs to the OH
- Distributes power to the VFATs and OHs from DC-DC converters (bPOL12V, 3 per GEB)
- 1 Wide and 1 Narrow GEB per layer

Current Status and Plans:

- Pre-production boards produced and successfully tested
- Future iteration with halogen free PCB, optimized fiber routing and powering configuration

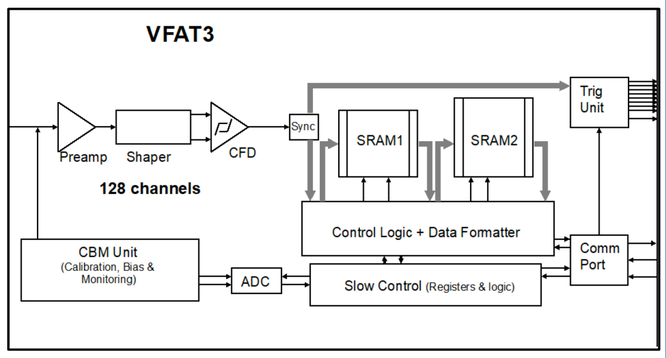

Figure 4: VFAT3b block diagram

Figure 5: Plugin card with VFAT3b chip

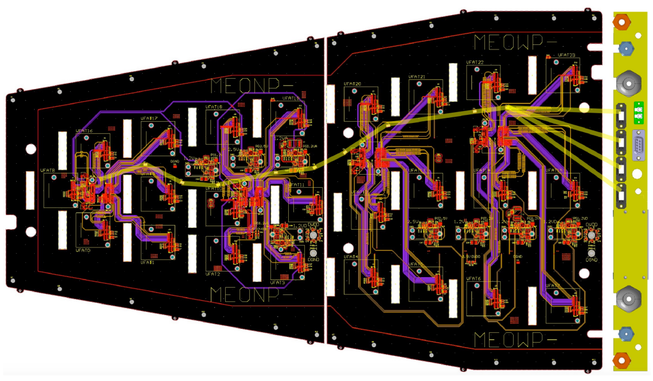

Figure 6: Design of the GEB

DC-DC converters (bPOL12V) will be used on the GEB for powering:

- Provide 1.2V and 2.5V to VFATs and OH
- 3 converters per GEB
- Carrier board for bPOL12V being designed for ME0 (by ULB)

Optohybrid and Back-end Electronics

Optohybrid (by UCLA) is the readout interface for 6 VFATs on the ME0 GEB:

- 2 lpGBT chips and 1 VTRx+ transceiver on each OH board
- No FPGA to ensure radiation hardness, data sent to back-end without compression
- Electrical links to VFATs at 320 Mb/s
- High speed optical links at 10.24 Gb/s for data transmission and at 2.56 Gb/s for trigger and control

Current Status and Plans:

- Pre-production boards (using halogen free PCB) produced and successfully tested (reliable optical and electrical links with bit error ratio $< 10^{-12}$)
- OH tester board being developed (will enable fast testing of all OH links)

ATCA based back-end system will be used for ME0 (also for GE2/1 and CSC):

- Has FPGA for online computation and transceivers to interface with VTRx+
- 2 ME0 stacks per card, 18 cards in total
- Supports high DAQ data rate of 700 Gb/s (all raw trigger hits from OH)
- Will perform 6 layer stub finding for trigger

Current Status and Plans:

- 2 pre-production boards available and tested with ME0 front-end electronics
- 2 more boards under production

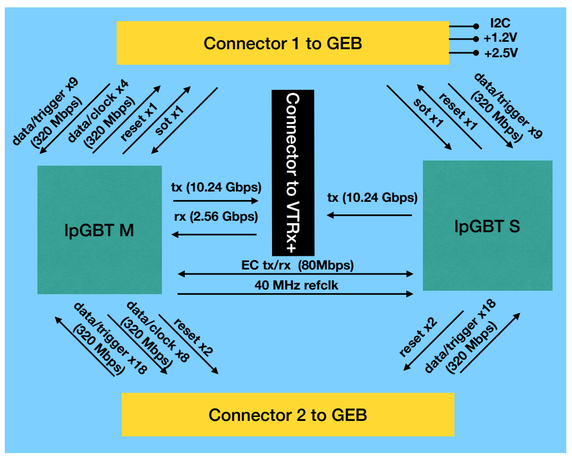

Figure 7: Block diagram for ME0 OH

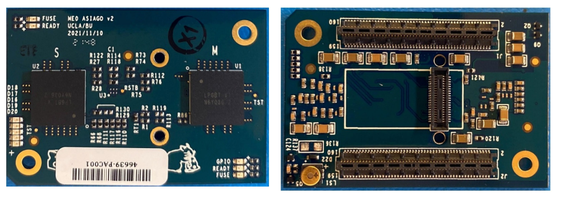

Figure 8: Pre-production ME0 OH board

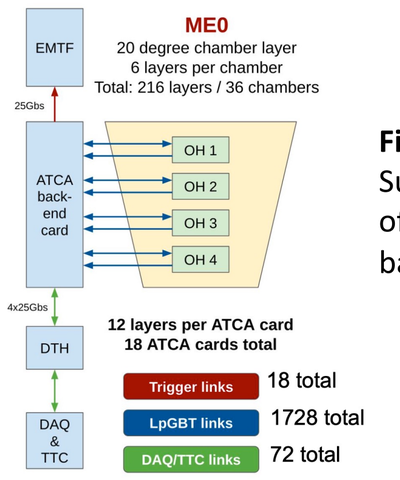

Figure 9: Summary of links to back-end

Latest Status and Results from ME0 Integration

Multi-layer ME0 stack test stand being integrated at CERN:

- Using all the latest ME0 electronics available
- First test of simultaneously operating multiple ME0 layers
- Will be important for firmware testing including stub finding

Figure 10: Picture of the ME0 stack at CERN

Current Status and Test Results:

- Currently has 2 layers (more layers to be added soon)
- Half of each layer assembled due to constraints in availability of electronics
- Successfully tested the operation of all VFATs and OH on 2 layers, mainly:
  - Equivalent noise charge (ENC) measurements for the data links using S-Curves with injected calibration signals – results look good

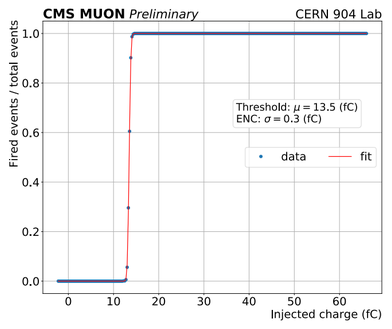

Figure 11: S-Curve for one channel with data and fit results on one VFAT plugin card on a ME0 detector

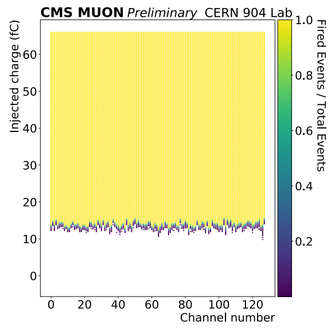

Figure 12: S-Curve for all 128 channels on one VFAT plugin card on a ME0 detector

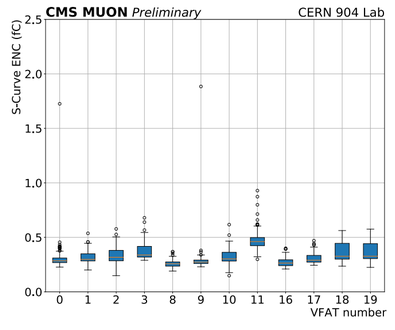

Figure 13: S-Curve ENC distributions for all 128 channels for 12 VFATs on a ME0 detector

- The noise rate measurement of the trigger links (S-bits) by scanning against the threshold setting in the VFAT – results look good

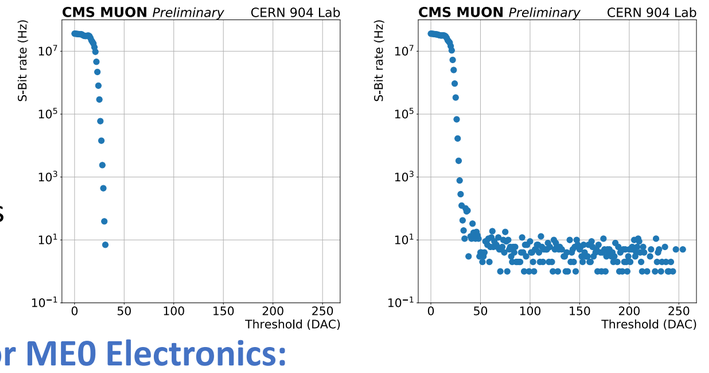

Figure 14: S-bit noise rate vs threshold from all 128 channels on one VFAT on a ME0 detector without (left) and with (right) application of high voltage across the GEM foils

Overall status and planning for ME0 Electronics:

- Complete the testing of all ME0 electronics after integrating with chamber
- Aim to undergo the ME0 electronics review in Summer 2022 before final production