

MALTA monolithic CMOS pixel sensors in Tower 180 nm technology

Heinz Pernegger / CERN EP Department
Heinz.pernegger@cern.ch

On behalf of H. Pernegger, P. Allport, I. Asensi Tortajada, D.V. Berlea, D. Bortoletto, C. Buttar, F. Dachs, V. Dao, H. Denizli, D. Dobrijevic, L. Flores Sanz de Acedo, A. Gabrielli, L. Gonella, V. Gonzalez, G. Gustavino, M. LeBlanc, K. Oyulmaz, F. Piro, P. Riedler, H. Sandaker, C. Solans, W. Snoeys, T. Suligoj, M. van Rijnbach, A. Sharma, M. Vazque Nunez, J. Weick, S. Worm, A. Zoubir



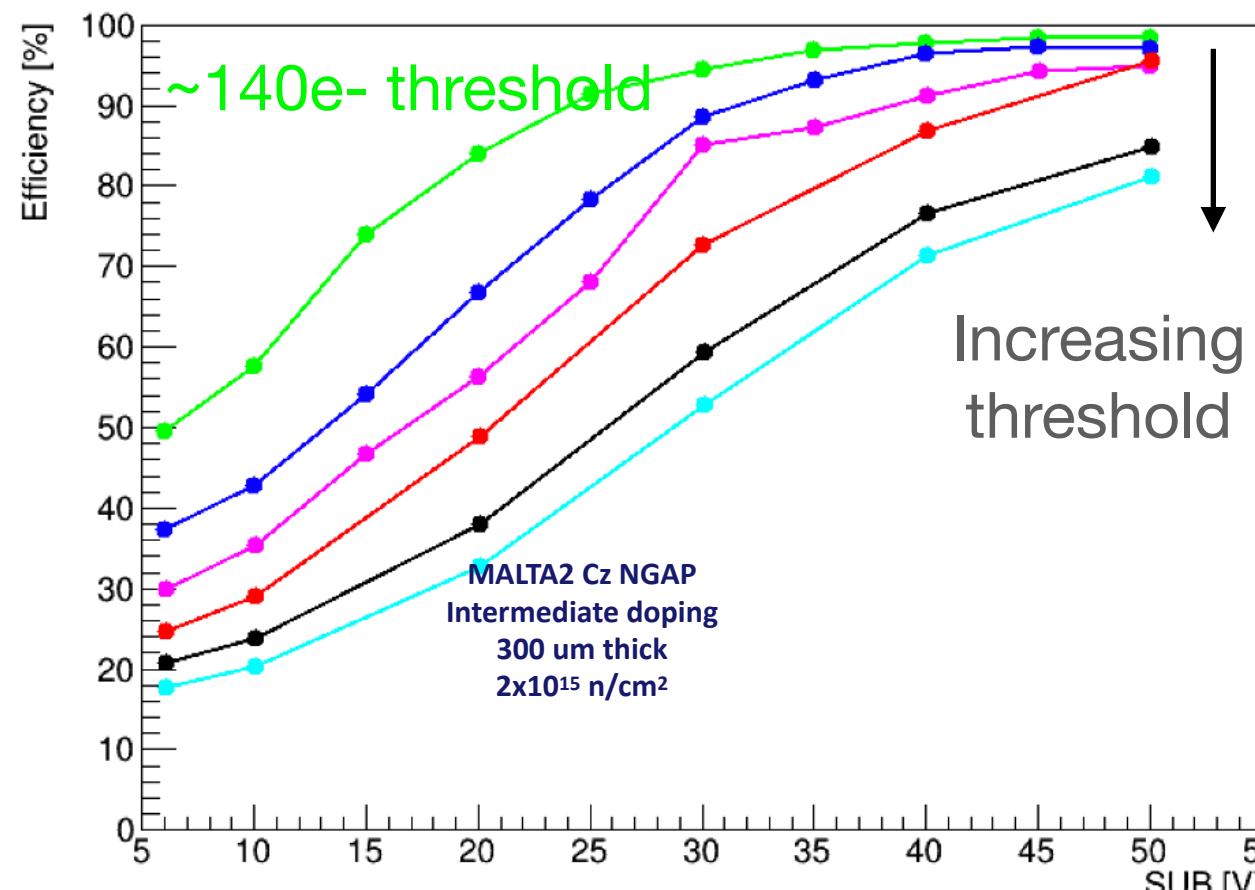
MALTA = Radiation hard small pixel CMOS sensor for tracking

MALTA sensor parameters and performance

- Pixel Pitch pixel size $36.4 \times 36.4 \mu\text{m}^2$
- Matrix size 512×512 pixel (MALTA1) and 512×224 pixel (MALTA2)
- Asynchronous readout architecture to stream all hit data to output (trigger-less operation)
- Sensors data daisy-chain for sensors-to-sensor data transmission
- sensor thickness optimised to application $50 \mu\text{m}$ to $300 \mu\text{m}$ on Cz-substrate
- full efficiency ($>98\%$) $2 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$
- TID radiation hardness tested OK to 100Mrad
- time-resolution $<2\text{ns}$
- threshold after irradiation 120 e^-



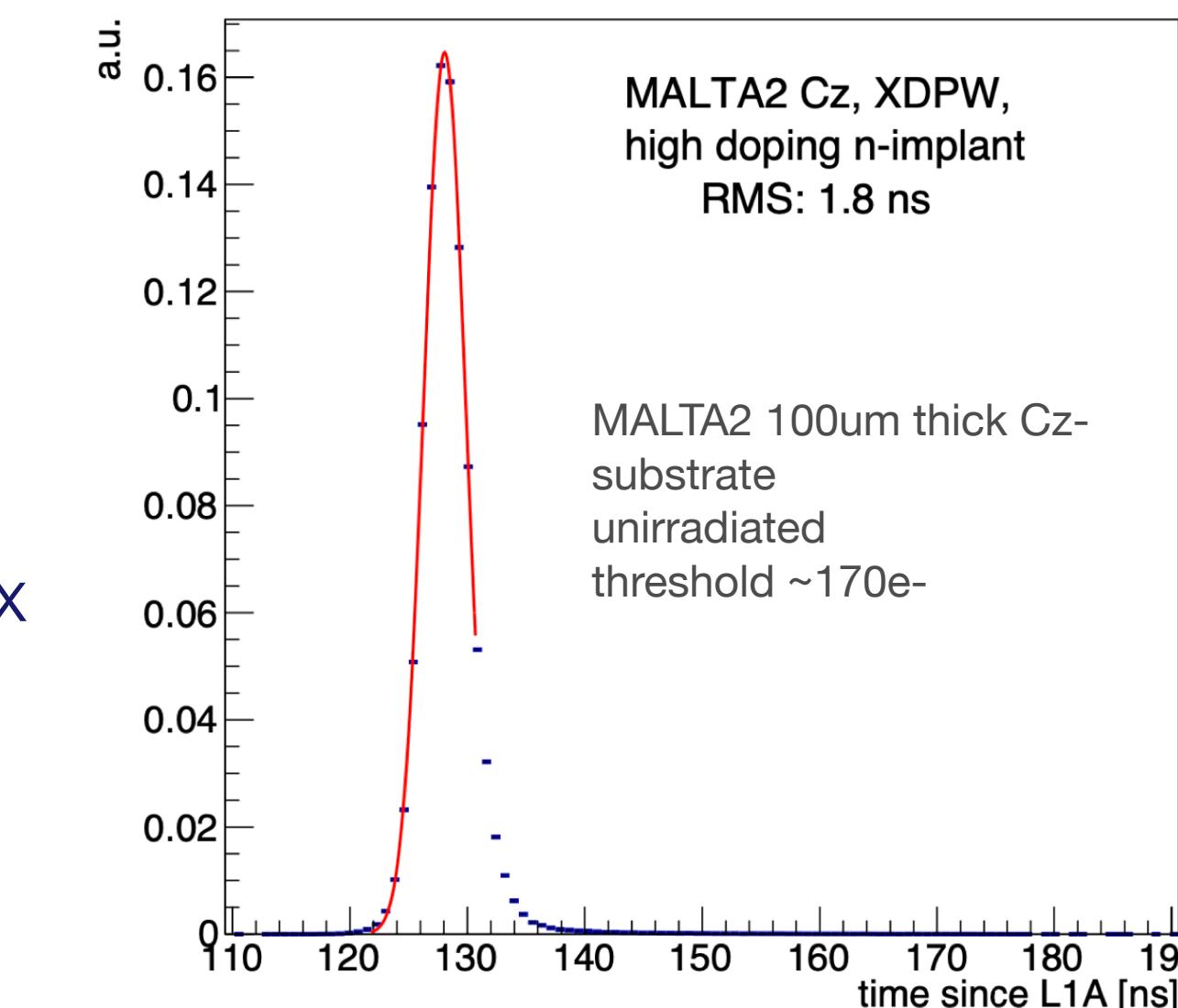
MALTA2 efficiency $>98\%$ after $2 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$ irradiation



- Good performance of Cz samples at $2 \times 10^{15} \text{n}/\text{cm}^2$
- Expected uniformity at lowest threshold setting
- Cluster size increases with substrate voltage
 - Maximum at ~ 1.9 at 50 V at 120 e^-
- Efficiency better than 98% at 50 V bias at 120 e^-

MALTA2 time resolution in beam tests $\sim 2\text{ns}$

- Time of arrival of leading hit in the cluster w.r.t. scintillator reference
 - Included scintillator jitter : 0.5 ns
 - Signal latching at FPGA: $3.125/\sqrt{12} = 0.9 \text{ ns}$
- Timing distribution integrated on full chip after correction in X and Y direction:
 - Y correction due to time propagation across the column (linear behaviour)
 - X correction compensates for non-uniformities in chip response



University of Oslo



University of Zagreb