
Monolithic Pixel Sensors in SOI technology – R&D activities at LBNL

SuperB Detector Workshop

SLAC, February 15, 2008

Devis Contarato

Lawrence Berkeley National Laboratory



M. Battaglia, L. Glesener (UC Berkeley & LBNL), D. Bisello, P. Giubilato (LBNL & INFN Padova), P. Denes, C. Q. Vu (LBNL)

Outline

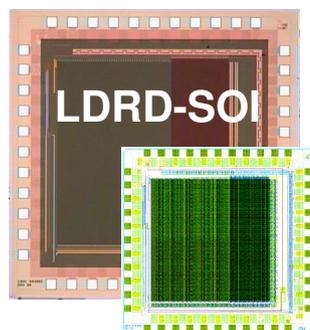
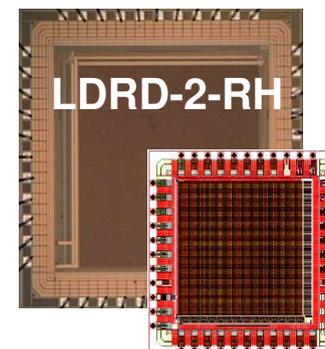
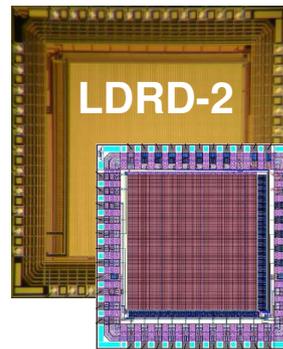
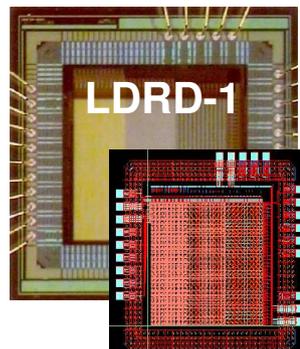
- **Introduction: Monolithic pixels @ LBNL**
- **SOI monolithic pixels: a brief history**
- **OKI 0.15 μm FD-SOI process**
- **The LDRD-SOI chip**
- **Beam test and radiation tests**
- **Conclusions & Outlook**



Monolithic pixels @ LBNL

• CMOS Monolithic Pixels

- AMS 0.35 μm CMOS tech.
- LDRD-1: first 3T prototype
- LDRD-2: in-pixel CDS
- LDRD-2-RH: rad. tol. layout
- LDRD-3: integrated ADC

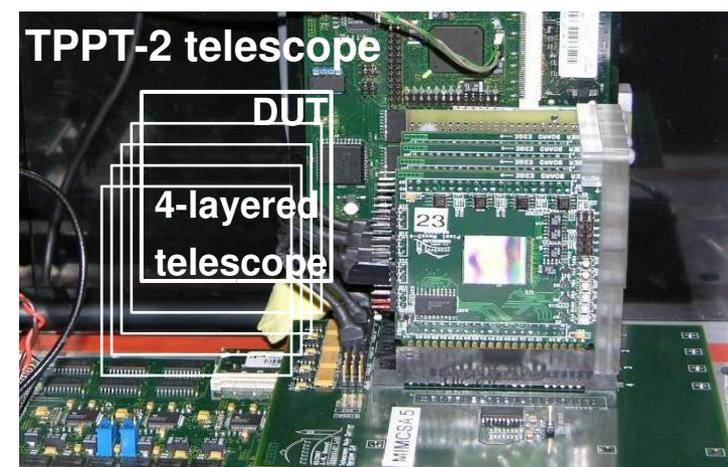


• SOI Pixels

- First prototype in OKI 0.15 μm FD-SOI technology
- Analog and Digital Pixels
- Second Prototype recently submitted

• Tracking with thin CMOS pixel telescope

- 4 layer, 50 μm thin MIMOSA-5 sensors
- Deployed at LBNL ALS and FNAL MTBF beam-tests



LBNL beam facilities

Advanced Light source (ALS)

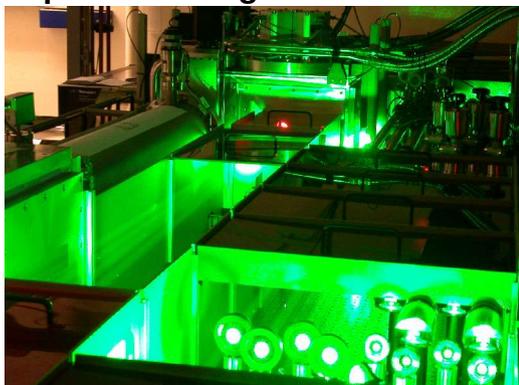
- X-ray light from 1.9 GeV electrons in 200 m storage ring
- 35+ beam lines for physics, material science and biology experiments
- 1.5 GeV e^- beam-test line extracted from injection booster



<http://www-als.lbl.gov>



<http://loasis.lbl.gov>



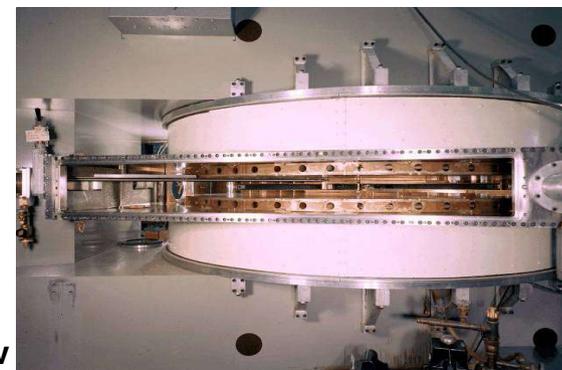
Laser Optics and Accelerator Systems Integrated Studies (LOASIS)

- Electron acceleration using TW laser wakefields in plasma: 1 GeV e^- achieved with 40 TW Ti:Sapphire laser in 3.3 cm
- Plans for upgrade up to 10 GeV

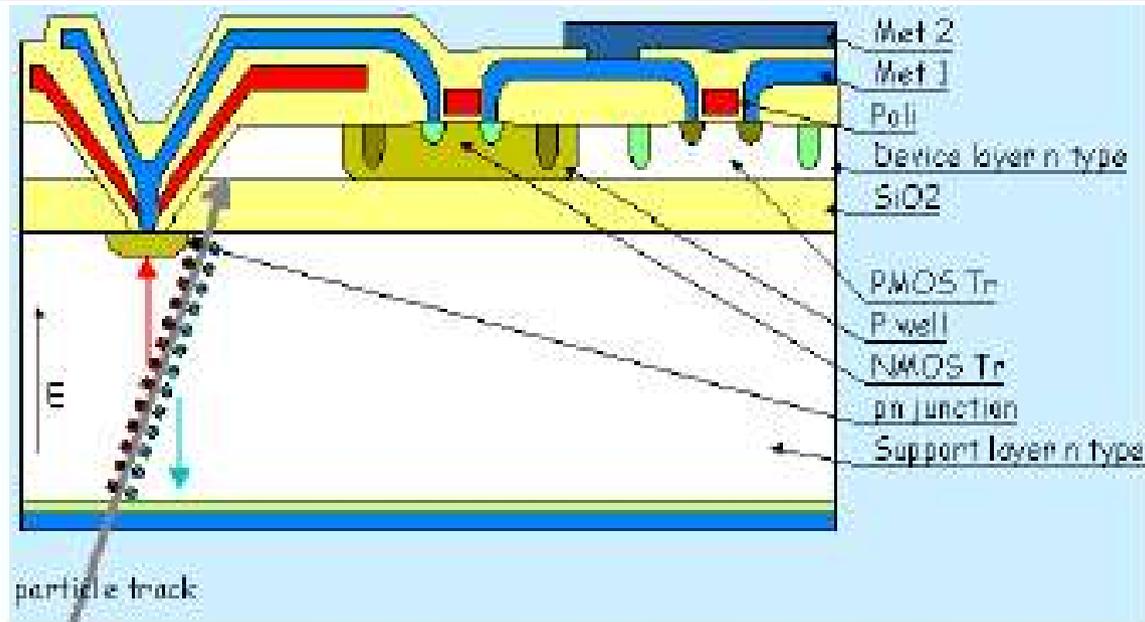
88-inch cyclotron

- Beam lines for proton, heavy ion and neutron irradiation
- Facilities for detector test with 30 MeV p and 1-20 MeV n

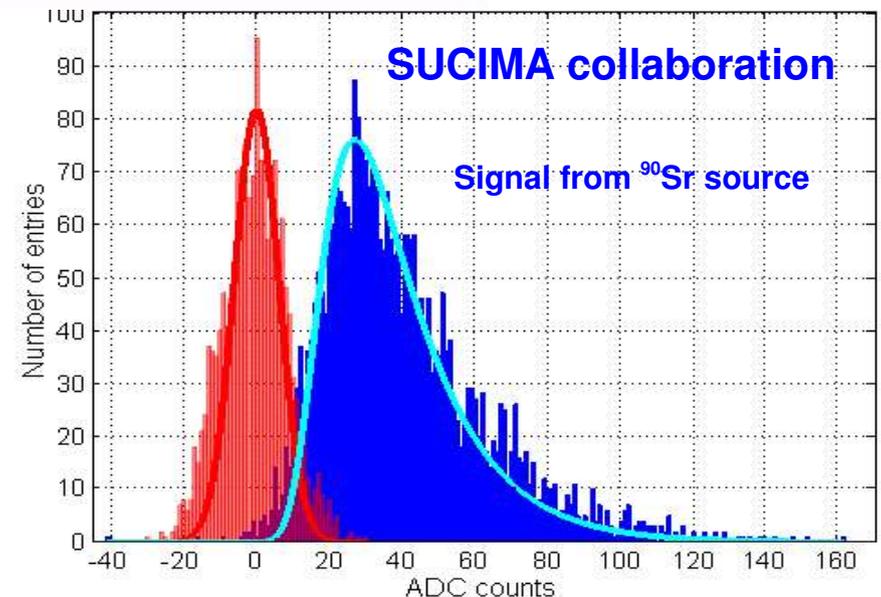
<http://cyclotron.lbl.gov>



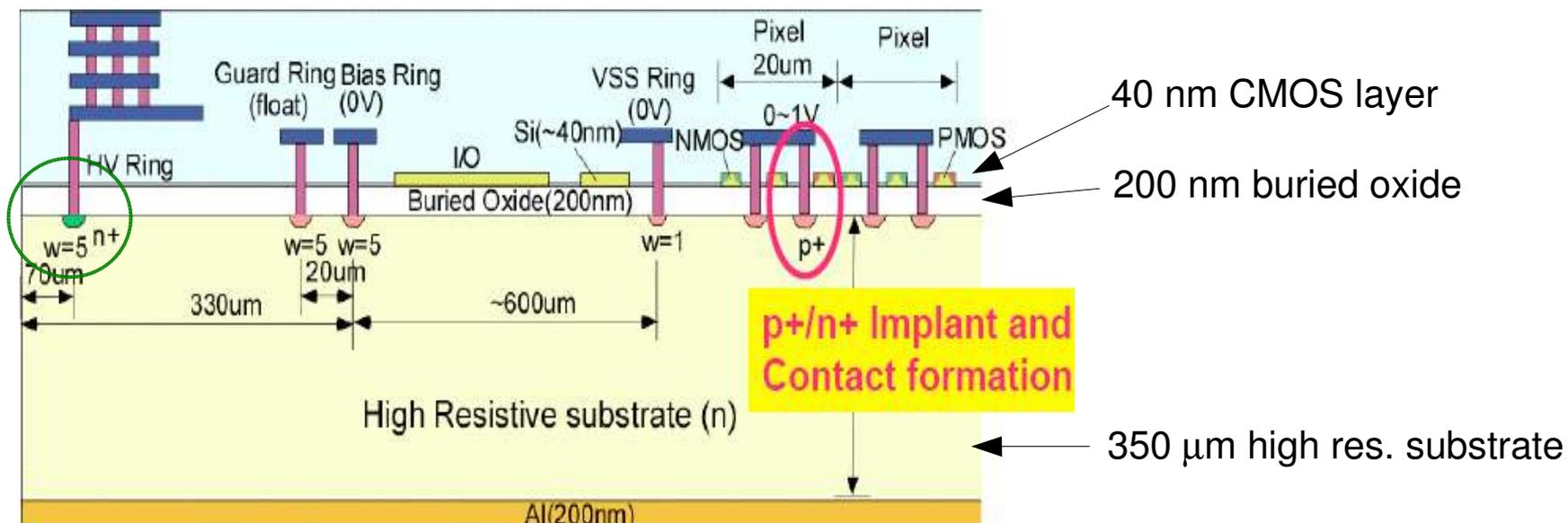
SOI monolithic pixels: a brief history



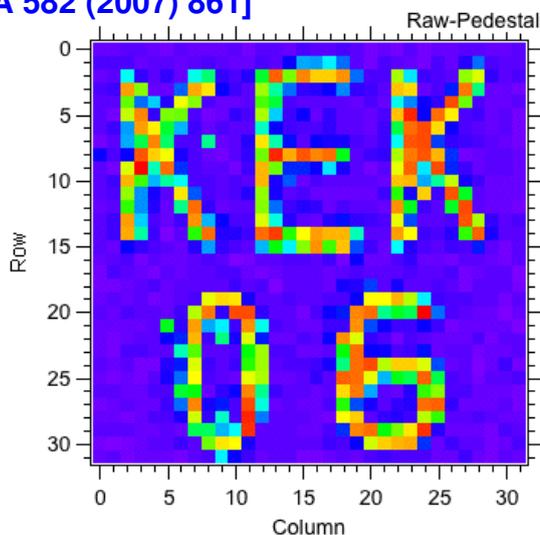
- **SOI: Silicon-On-Insulator** technology
- Electronics layer isolated from high-resistivity substrate by buried oxide; depletion of substrate via pn junction implanted through buried oxide and readout integrated on top of sensor
- Proof of principle from SUCIMA collaboration, prototype in 3 μm process (IET, Poland), though not compatible with standard CMOS



OKI FD-SOI process



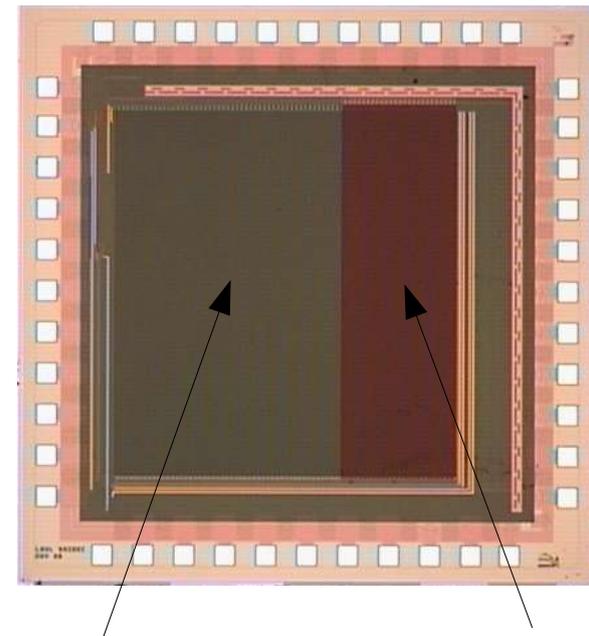
[NIM A 582 (2007) 861]



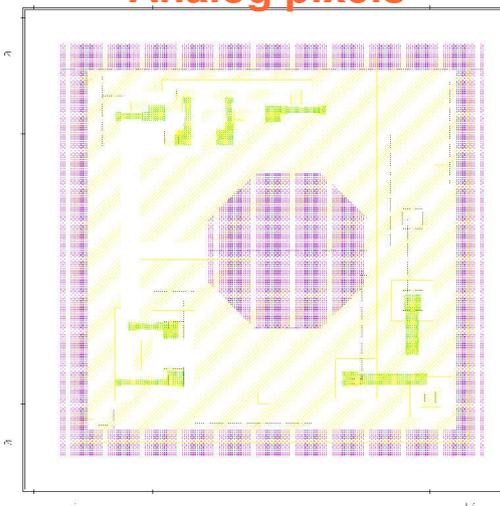
- Novel 0.15 μm fully-depleted SOI process from OKI; combines high-res substrate with full CMOS circuitry on top layer; high-speed, low power dissipation digital design possible, latch-up immunity
- 350 μm substrate; 200 nm buried oxide; 40 nm CMOS layer, fully depleted at operational voltages
- Functionality demonstrated by KEK chip in '06

LDRD-SOI pixel prototype

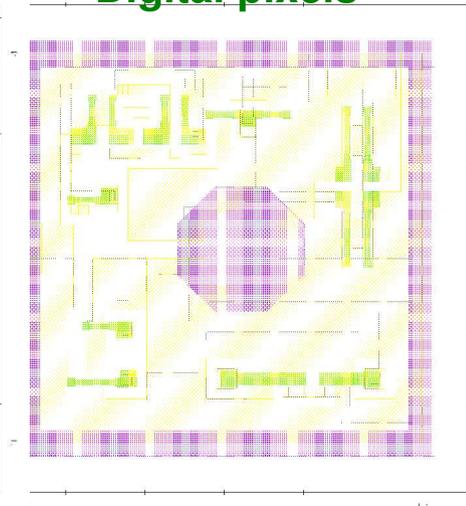
- 0.15 μm OKI fully depleted SOI
- December 2006 pilot run (through KEK), not optimized in terms of leakage current
- 160x150 pixels, **10x10 μm^2 pixels**
- 1x1 μm^2 and 4x4 μm^2 diodes
- floating p-type guard-ring around each pixel
- Choice of substrate contact and pixel layout justified by TCAD simulations
- **2 analog parts:**
 - 1.8 V and 1.0 V, “high” and “low” voltage resp.
 - simple 3T architecture
- **1 digital part:** in-pixel comparator and latch, no amplifier (no static power dissipation); adjustable threshold; 15 transistors/pixel
- Readout at 6.25 MHz, 1.3 ms int. time (analog pixels)



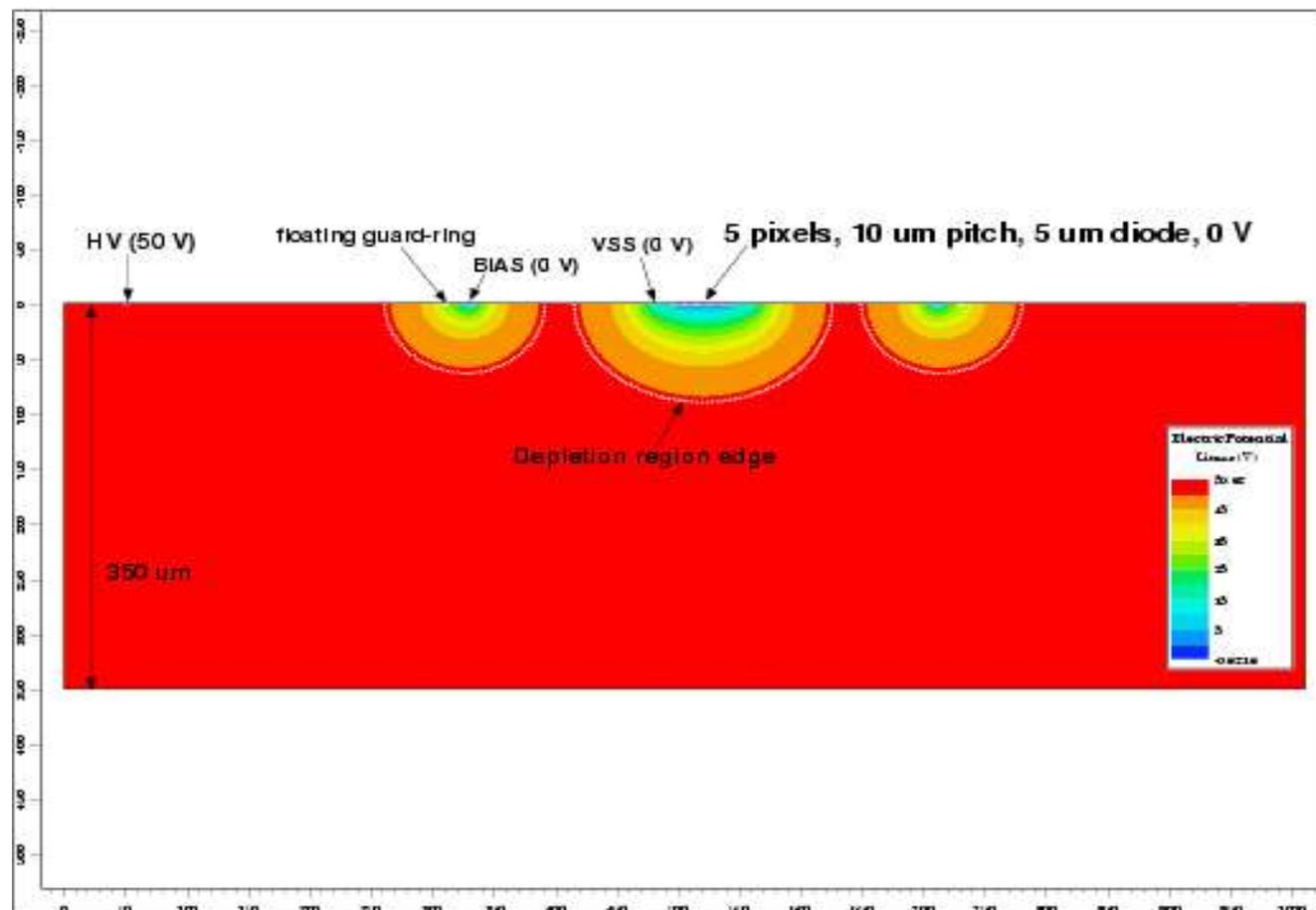
Analog pixels



Digital pixels



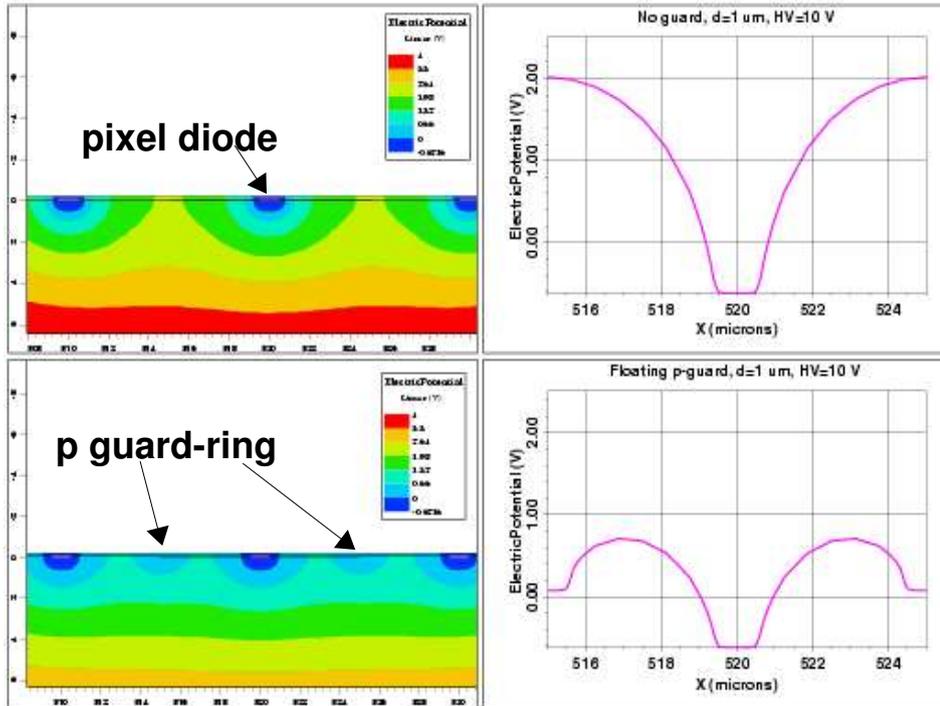
TCAD simulations



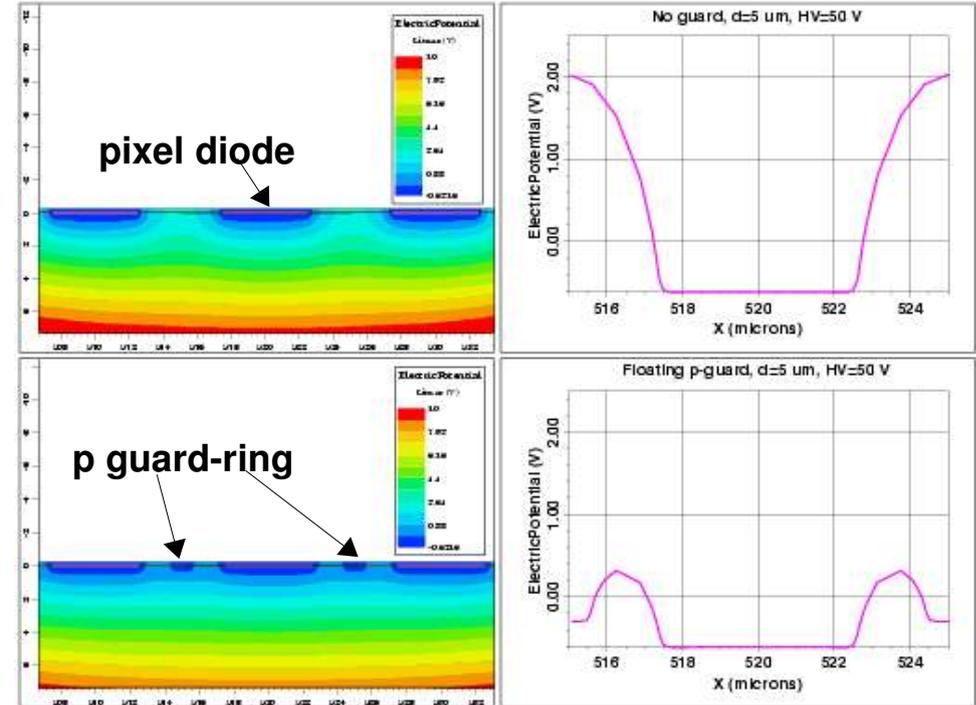
- Simulation performed with Synopsys TCAD (Taurus Device)
- 2D model of 5 pixel cluster (10 μm pixel pitch) and substrate contact regions
- 350 μm thick substrate, n-type silicon ($6 \times 10^{12} \text{ cm}^{-3}$); 200 nm buried oxide
- Different diode sizes ($1 \times 1 \text{ μm}^2$ and $5 \times 5 \text{ μm}^2$)

Surface potential, choice of pixel guard-ring

1x1 μm^2 diode, HV=10 V



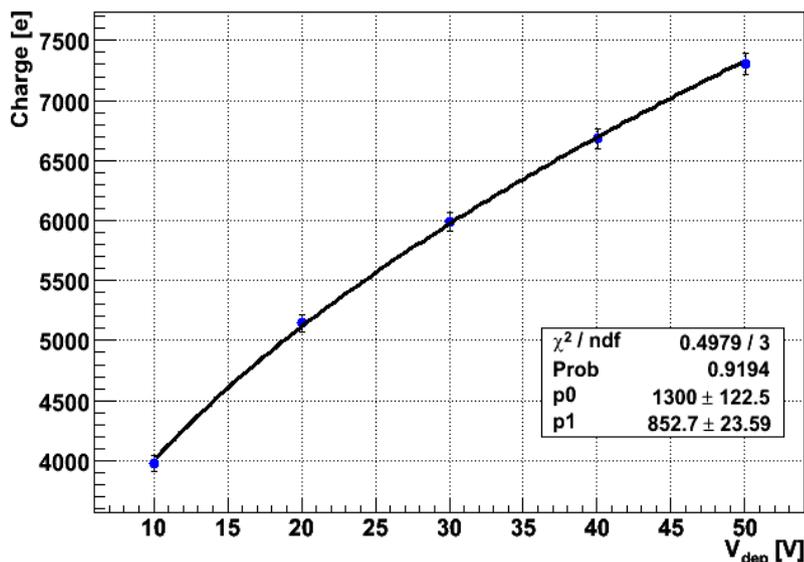
5x5 μm^2 diode, HV=50 V



- Pixel surface potential for different diode sizes and depletion voltages
- Potential in-between pixels too high, especially for smaller diode size
- Add floating p-guard structure (1 μm wide) to keep potential low and limit back-gate effects on MOS transistors on top of buried oxide

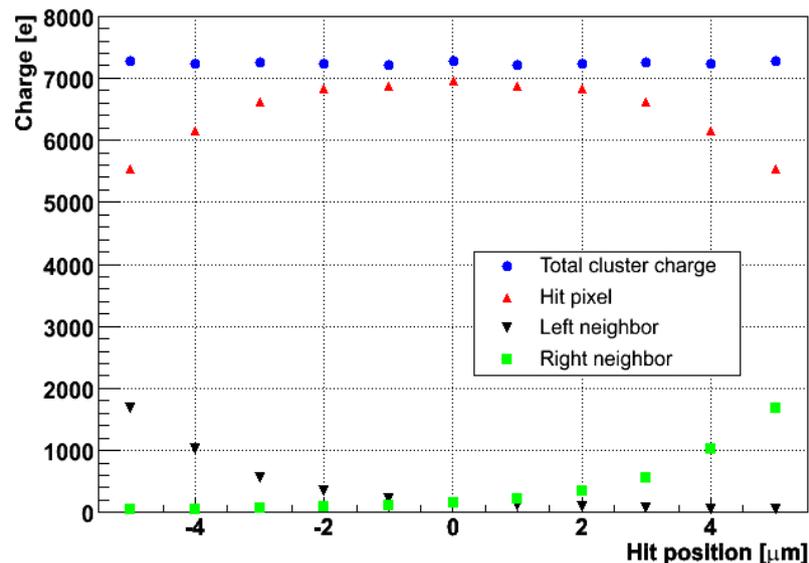
Charge collection simulation

Cluster charge vs depletion voltage, $5 \times 5 \mu\text{m}^2$ diode

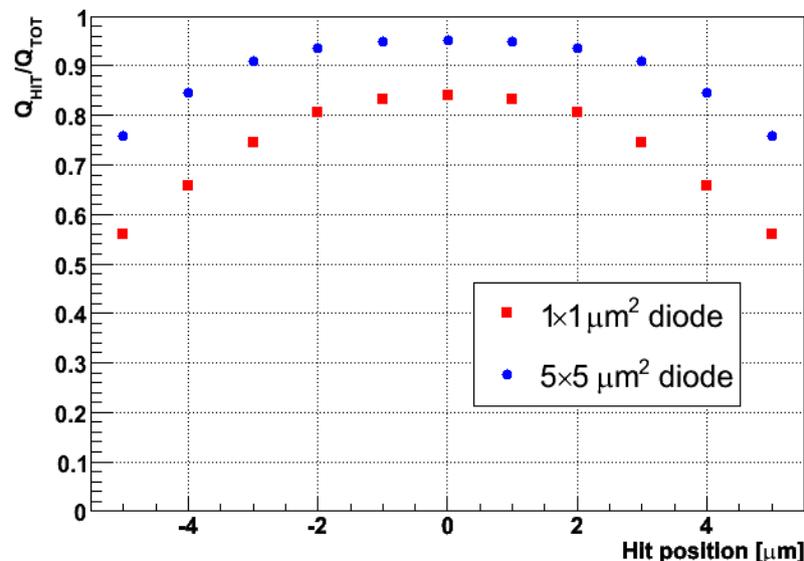


- Simulate passage of m.i.p. ($80 \text{ e-h}/\mu\text{m}$) and charge collection in 5 pixel cluster
- Study collected signal as a function of depletion voltage and of track position within hit pixel
- Total cluster signal \sim constant as a function of position within hit pixel
- Most of the charge is collected in hit pixel, expect larger cluster size for smaller diode pitch

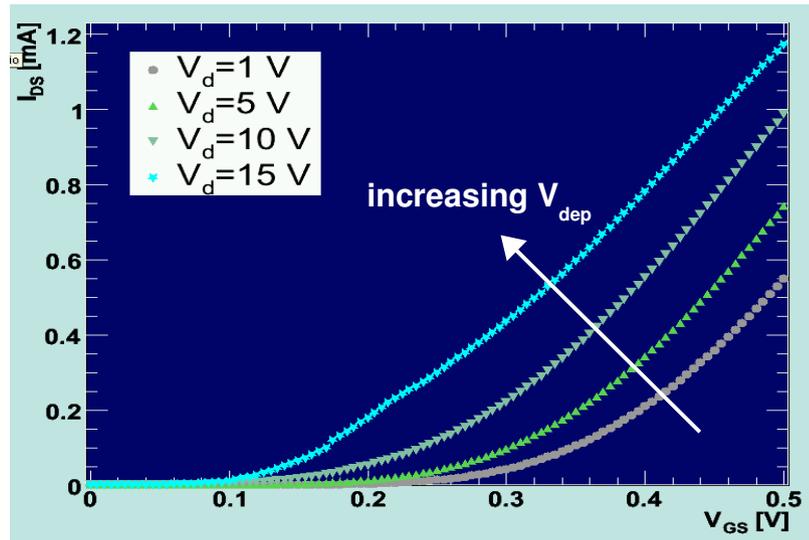
Charge vs hit position, $d=5 \times 5 \mu\text{m}^2$, HV=50 V



Charge fraction in hit pixel



Single transistor test: back-gating

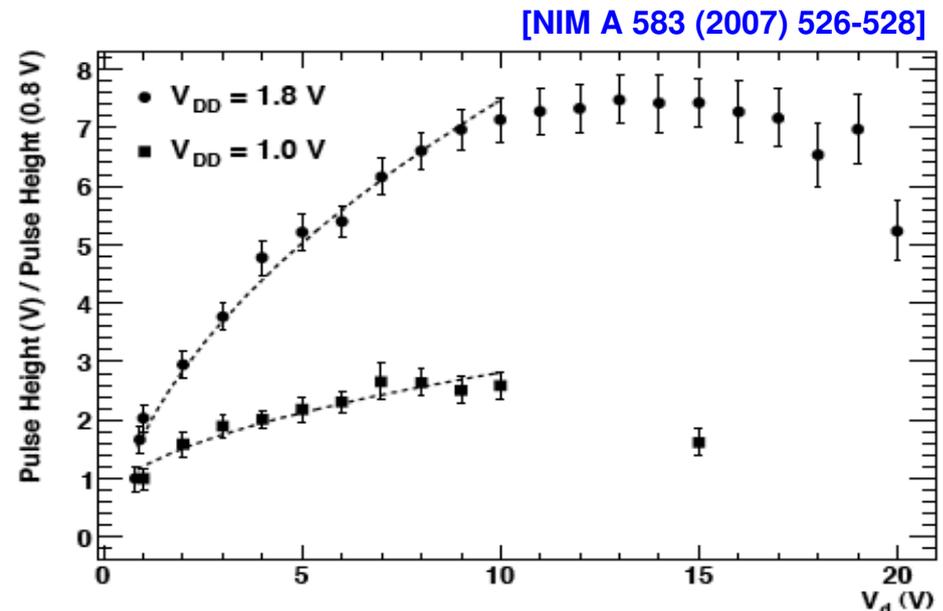


- Single test transistors: p- and n-MOSFETs, W/L=50/0.3, 1.0V and 1.8V bias. various body contacts (floating, source, gate)
- Input and output characteristics measured for different depletion voltages
- Back-gating causes a shift in threshold voltage as the substrate voltage increases
- Significant effect observed in single transistor tests: expect analog chip section functional for $V_{dep} < 20$ V

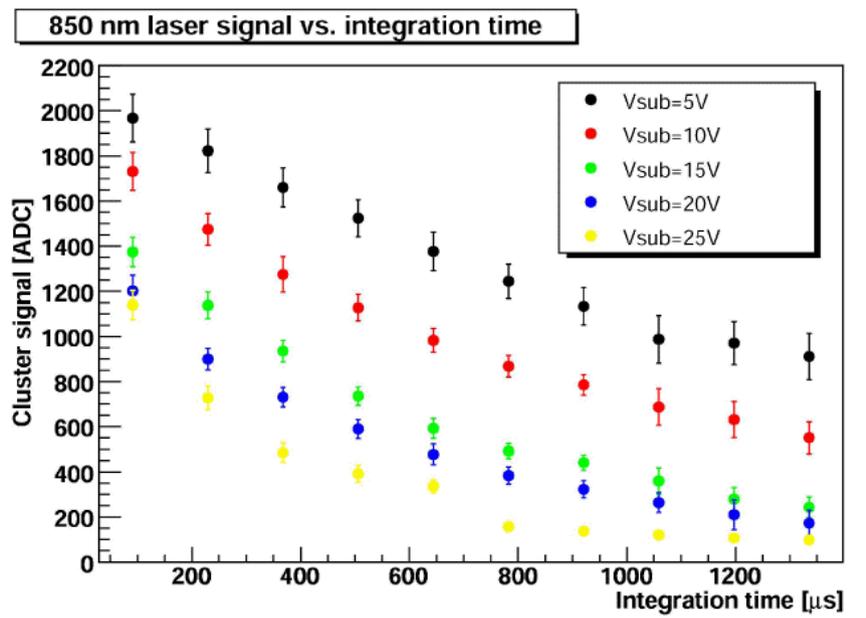
- Depletion region thickness vs substrate voltage measured with 1060 nm laser signal
- Expect depletion region thickness:

$$D \propto \sqrt{V_{dep}}$$

- Good agreement with expectation for depletion voltage up to $V_{dep} \sim 10$ V

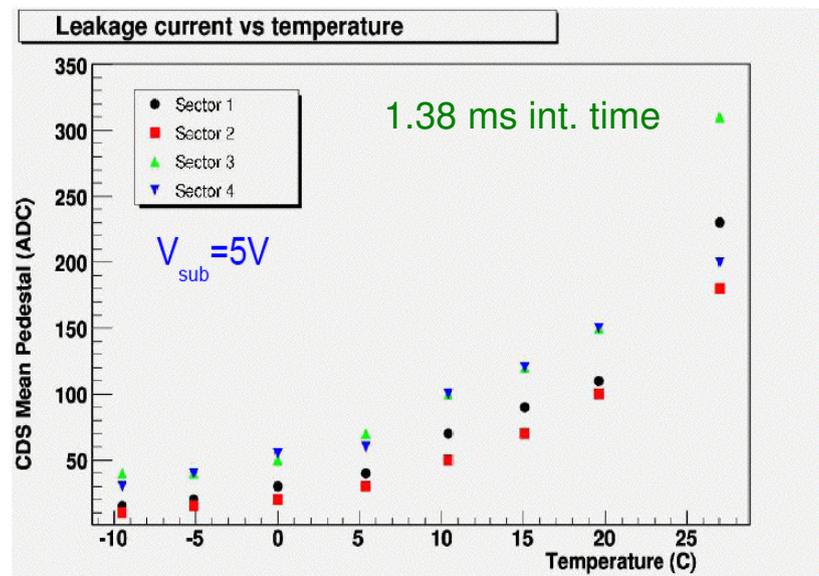


Leakage current studies

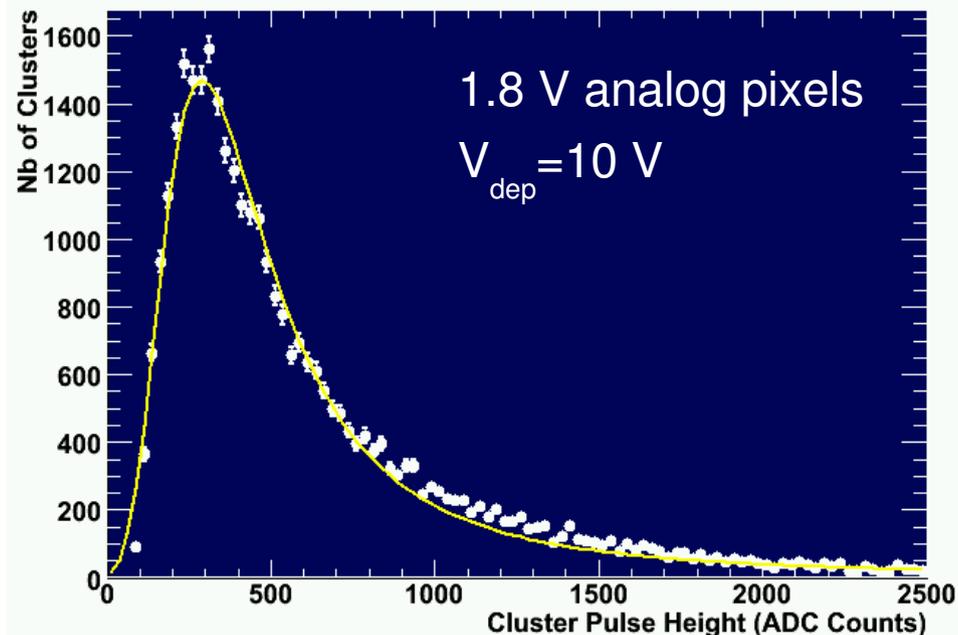
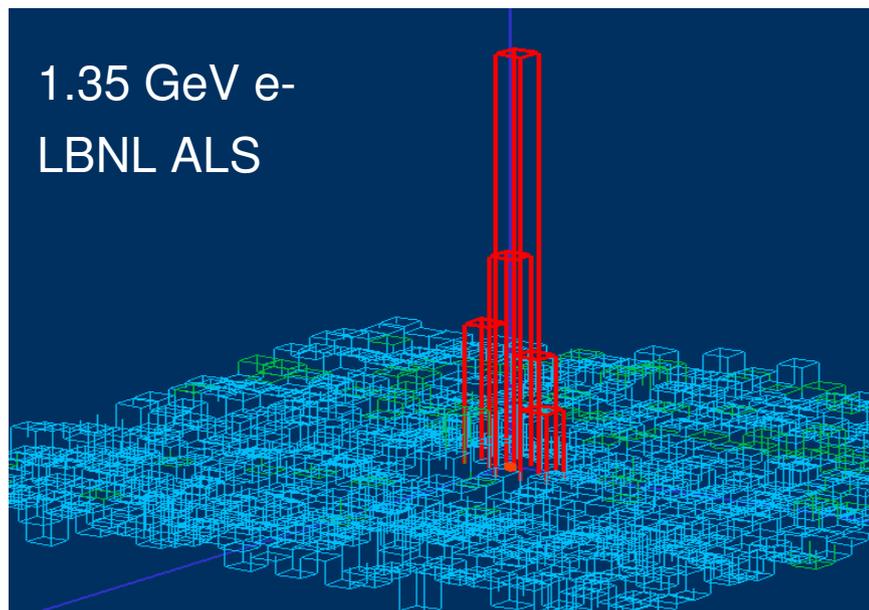


- Tests with 850 nm and 1060 nm lasers focused to a $\sim 20 \mu\text{m}$ spot
- **Signal loss for long integration times:**
 - More loss at large substrate voltages
 - combined effect of leakage current and back-gating
- To retain the entire signal, pixels must be read out immediately following charge collection.

- Noise and leakage current vs temperature down to -10°C
- Leakage current estimated from pixel dark level after correlated double sampling (CDS)
- **Decrease in leakage current at lower temperatures**



Electron beam-test: analog sectors



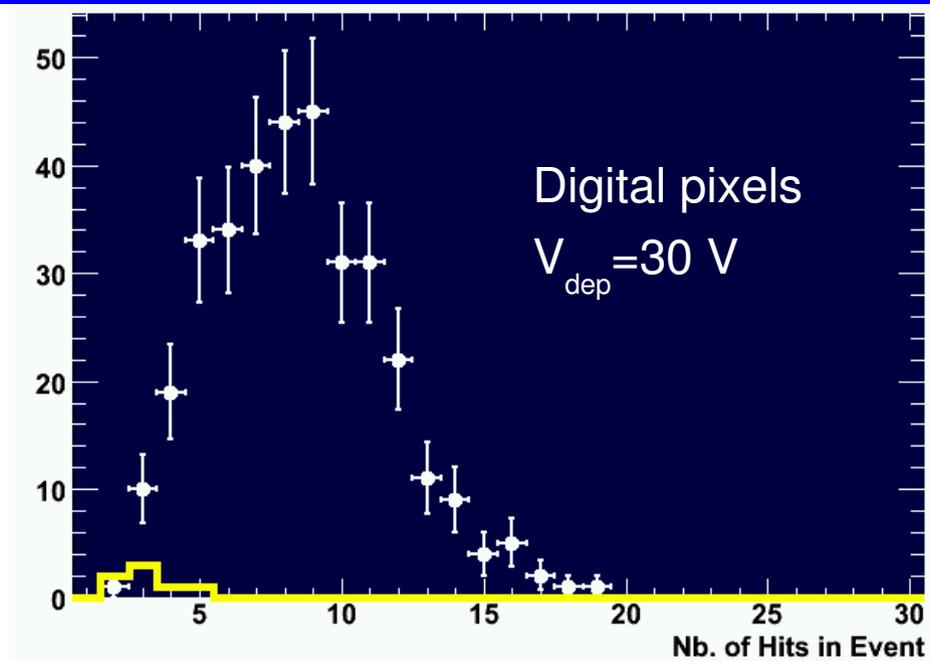
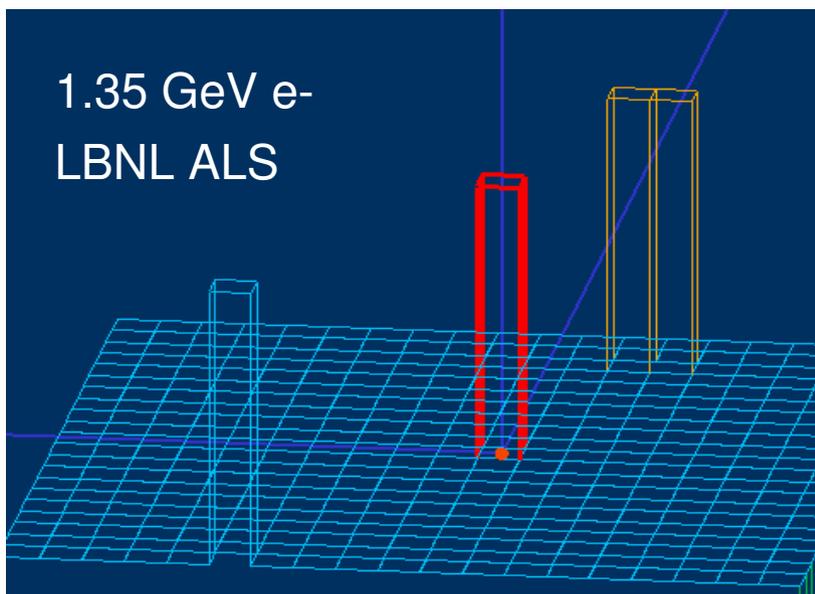
1.0 V Analog Pixels				
V_d (V)	Clusters / Spill (Beam on)	Clusters / Spill (Beam off)	Signal MPV (ADC Counts)	Average Signal/Noise
1	3.9	0.02	105	7.4
5	6.7	0.03	140	8.8
10	4.4	0.03	164	8.1
15	1.4	0.02	123	6.5

1.8 V Analog Pixels				
V_d (V)	Clusters / Spill (Beam on)	Clusters / Spill (Beam off)	Signal MPV (ADC Counts)	Average Signal/Noise
1	9.7	0.05	132	8.9
5	14.0	0.12	242	14.9
10	7.8	0.20	316	15.0
15	3.9	0.01	301	13.6

[NIM A 583 (2007) 526-528]



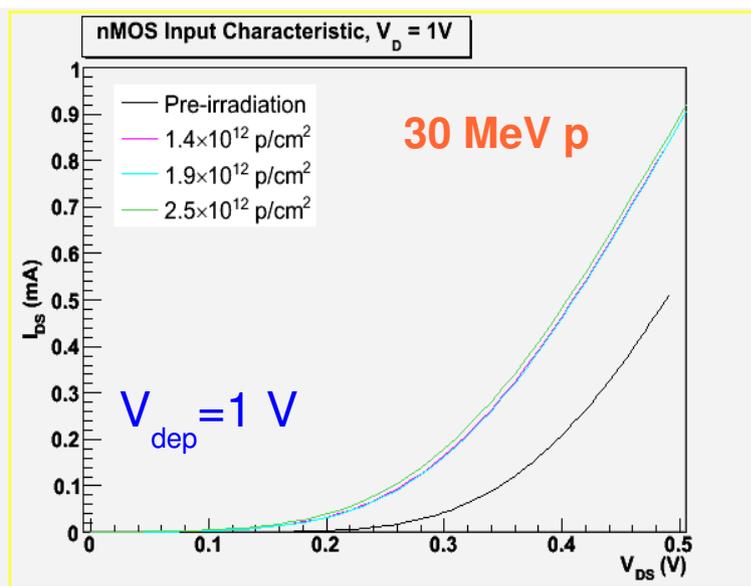
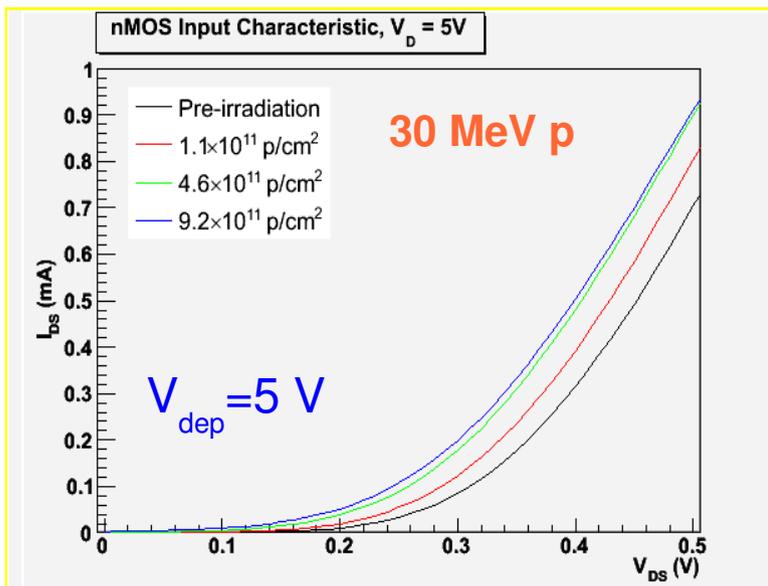
Digital pixels: beam-test results



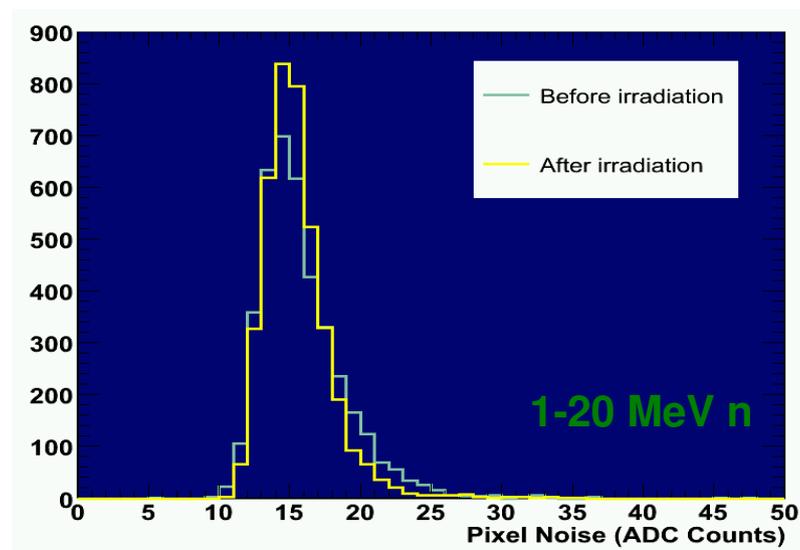
V_d (V)	Clusters/Evt w/ beam	Clusters/Evt w/o beam	<Nb Pixels>
20	3.62	0.04	1.78
25	5.81	0.04	1.32
30	8.31	0.04	1.26
35	1.60	0.01	1.14

- Adjustable integration time: reduced problem of charge loss due to leakage current
- Signal above threshold only at high substrate voltages:
 - analog threshold affected by back-gating
 - larger depletion \rightarrow increased charge signal
 - at 25-30 V, these effects seem to combine for best detection capabilities
- Cluster multiplicity decreases with increasing V_{dep}

Proton and neutron irradiation effects

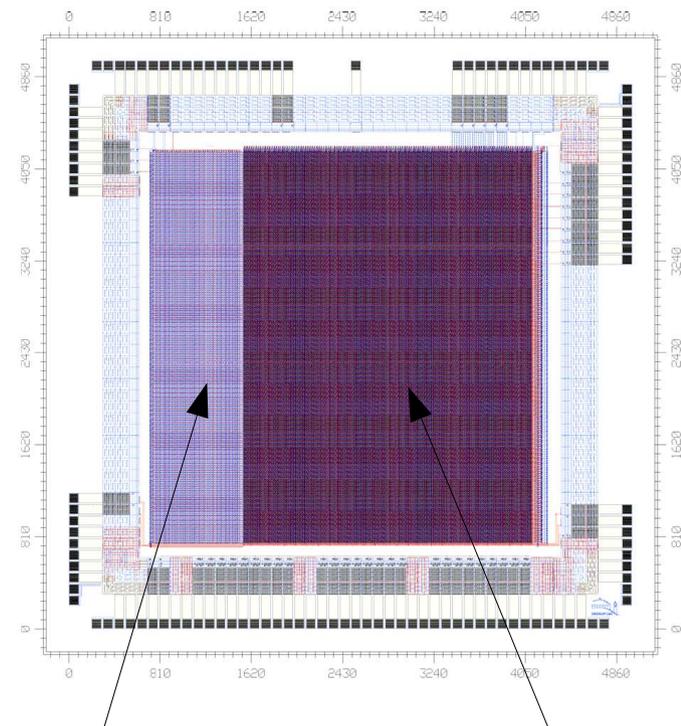


- Irradiations performed at LBNL 88" Cyclotron
- **30 MeV protons:** fluence up to 2.5×10^{12} p/cm²
 - Shift in transistor threshold voltages throughout irradiation
 - Charge trapping in BOX increases back-gating
- **1-20 MeV neutrons:** fluence up to 10^{11} n/cm²
 - No change in transistor characteristics
 - Test of analog pixels shows no significant noise degradation

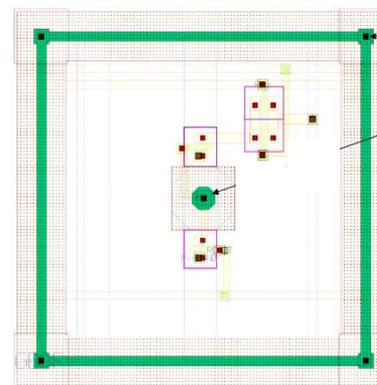


Outlook: the LDRD-SOI-2 chip

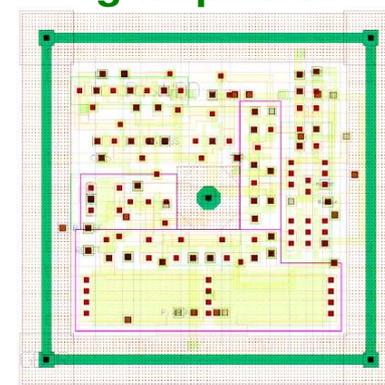
- OKI 0.20 μm FD-SOI process; production process, while 0.15 μm process is being upgraded from R&D to production
- 40x172 analog pixels: simple 3T structure for technology evaluation
- 128x172 digital pixels: evolution of chip-1 digital pixel: 2 capacitors for in-pixel CDS, clocked comparator with current threshold output; 40 transistors/pixel
- Submitted January 2008, expected in April 2008



Analog pixels



Digital pixels



Summary

- **First OKI 0.15 μ m FD-SOI pixel prototype designed and successfully tested at LBNL**
 - analog and digital pixel detection capabilities demonstrated with infrared lasers and 1.35 GeV electrons at LBNL ALS
 - analog pixels functional up to 10-15 V depletion voltage
 - digital pixels functional up to 30 V depletion voltage
 - back-gating effects significant at high substrate voltages and after irradiation with protons
- **Further tests under way:**
 - ALS beam-test: pairing with a 50 μ m thin MIMOSA-5 sensor to normalize flux and correlate hits
 - laser studies for consistency of threshold across digital pixels
 - uniformity scan of analog pixels
- **Second prototype submitted in optimized 0.20 μ m process**
- **Technology spin-offs:** detectors for synchrotron radiation (ALS), beam diagnostics (LOASIS), electron microscopy (NCEM)

