Trigger, DAQ, & Online: Perspectives on Electronics

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Outline

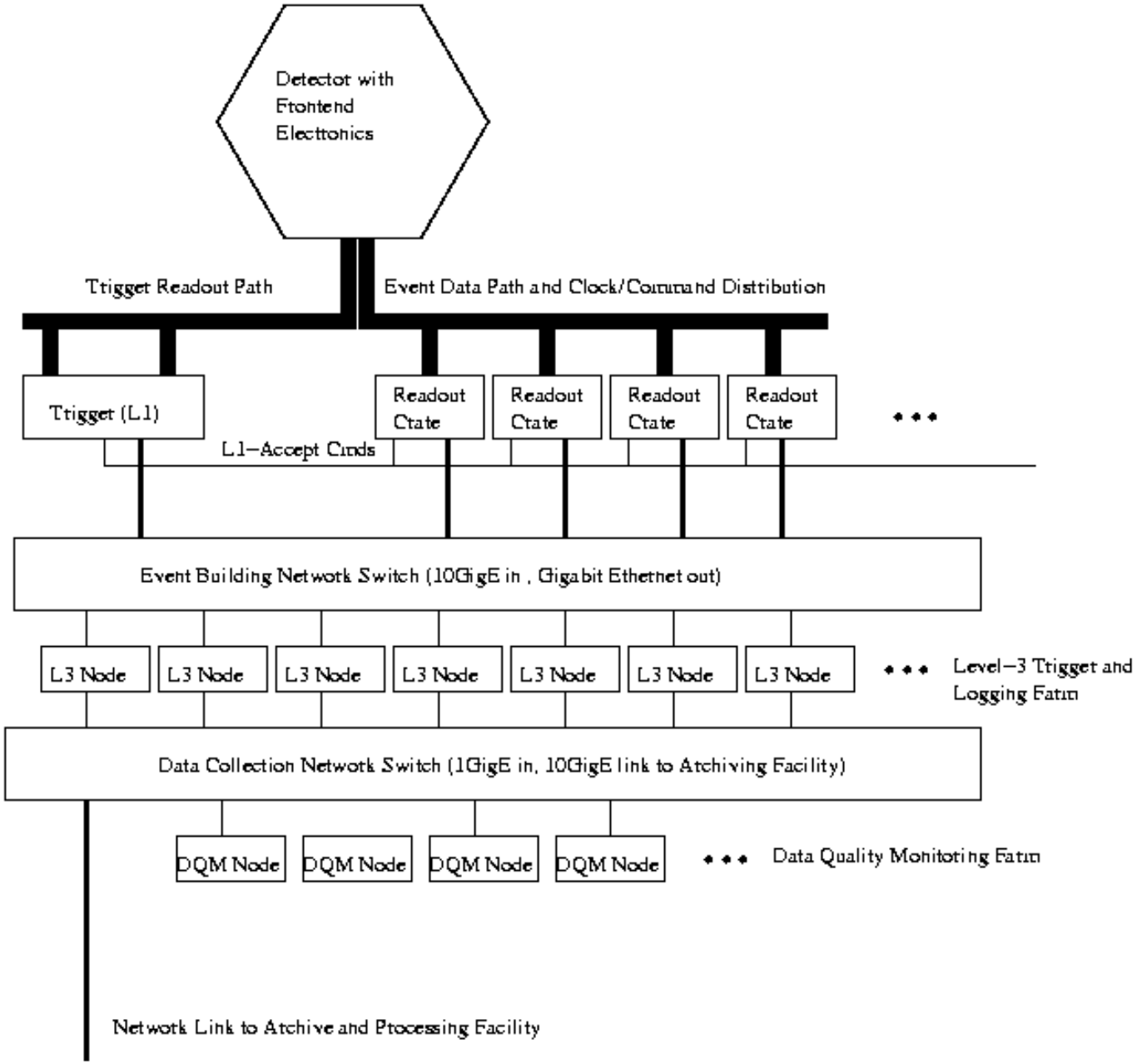
- Rate and Event Size Estimates
- Trigger
- FCTS and Data Flow
- Detector Control
- Configuration Management
- R&D Projects

Rate Estimates/Assumptions

- Trigger Rates –BaBar Open Trigger Philosophy
  - L1-Accept (dominated by e^+e^- interactions)
    - From BaBar:
      - ~20nb (BaBar physics filter output) → 20kHz @ 1e36
      - ~50nb Bhabhas (BaBar acceptance) → 50kHz @ 1e36
      - 10% scaled backgrounds of BaBar → ~25kHz
      - Operational BaBar experience: 50% headroom desirable
    - Would require L1 and Front End DAQ to handle 150kHz L1-Accept rate
    - Bhabha veto could bring down L1-A rate (with headroom) to ca. 100kHz
    - Assume Bhabha veto for now
  - L3-Accept
    - Assume ~20nb + ~5nb for monitoring triggers → 25kHz @ 1e36
    - Moderately optimistic extrapolation from BaBar
  - Rates are physics-driven and already fairly well-known

Event Size Estimates/Assumptions

- Event size
  - BaBar: ~35kByte average
  - SuperB: guess based on BaBar: 75kByte average
    - Some systems will be similar, but...
    - Possibly smaller cells in DCH
    - More samples needed to detect pile-up and overlapping events
    - Higher occupancy due to background events
    - Substantial uncertainty in SVT design and channel count!
  - So far this is really all just an uninformed guess
    - Further DAQ design work *requires* more clarity
    - Need to make progress at this workshop!



Looks like BaBar, doesn't it?

Trigger

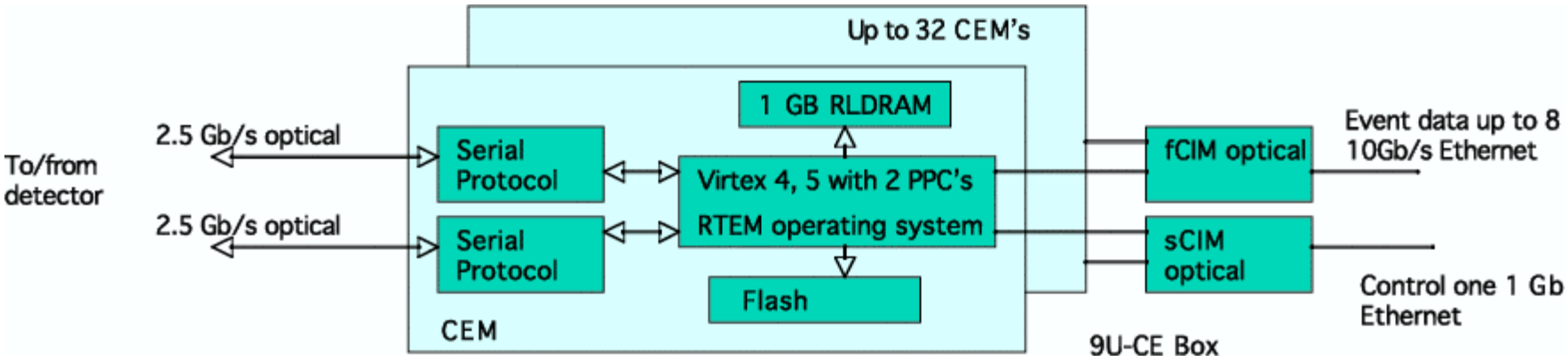
- BaBar-like trigger structure:
  - Level-1
    - Pre-event-readout **trigger based on drift chamber and calorimeter information**
    - Level-1-Accept initiates event readout
  - Level-2 (optional)
    - Trigger in data path acting on partial event information
    - Currently not foreseen (event sizes are small!)
  - Level-3
    - Software trigger running on server farm, acts on complete events.
    - Refines Level-1 calculations, allows more complex operations
  - Level-4
    - "Offline" filter - may need to place upstream of permanent storage!

CDR DAQ model

- Design based on a modular DAQ system currently developed at SLAC (for other programs!)
  - FPGA/System-On-A-Chip
    - PPC general-purpose CPUs
    - VHDL-style "DSPs"
    - Various link options, including 10GigE and 2.5GBit/s fiberoptic serial links
- Similar to BaBar, but faster fiber links to front-end electronics (2.5GBit/s)
- Feature extraction as close to front-ends as possible
  - Proof-of-concept in revised BaBar DCH electronics

DAQ Module

- Modular DAQ system design currently developed at SLAC for LSST, PetaCache, LCLS and other projects



Configuration Management

- FPGA configuration tracking
  - With more "traditional software functionality" implemented in FPGAs, FPGA firmware is considered "software" and must be included in the configuration and release management scheme

Fast Control and Timing system
(trigger distribution and flow control)

- "No" mandatory dead-time between triggers allowed
  - Frontend readouts that can "keep up" with a (very short) minimal allowed command spacing OR
  - Trigger queuing and fully addressable front end readout buffers

  Significant potential per-channel costs!
    - Channel requirements for raw data must be understood in detail

Control Systems

- Experiment ("Run") Control [...]
- Detector ("Slow") Control
  - Control detector and detector support systems
  - Monitor and record detector and environment conditions
  - Based on toolkit that provides interface to hardware
    - BaBar uses EPICS
    - Depending on hardware, a different system may be more appropriate
  - Should share a timebase with the FCTS (the event stream)
- Unified operator interface / GUI
- Electronic Logbook

R&D Projects – further study

- **Detailed evaluation of channel counts, and per-channel DAQ requirements**
  - Bit depth
  - Digitization rates and raw window sizes
  - Opportunities for zero-suppression and other compaction
  - Feature-extracted hit sizes
  - Implications of overlapping events
    - E.g., do they need to be kept together when read out?
- Study backgrounds and occupancies and their effect on event sizes

R&D Projects – further study II

- Level 1 Trigger
  - Define contributing subsystems and data paths
    - Need to understand what rates and precision of data are needed by Level 1
    - Possibility of tracking built in to SVT electronics?
  - Study attainable performance of a Level 1 Bhabha veto
- Assess cost of extending L1-Accept capacity to 150kHz
  - Headroom, no Bhabha veto, later lumi upgrades
- Investigate consequences of overlapping events, triggers and trigger queuing
- Queue modeling for data path to determine buffering requirements

R&D Projects – further study III

- Study adaptation of the current "Level-4" BaBar physics filter to Level-3 quantities
- Review LHC technologies for applicability:
  - Look at control system alternatives to EPICS
  - Concrete experience with ~100kHz DAQ (though expensive) - channel costs may be instructive