

Towards a beam test

Beam telescope and striplets with FSSR2 chips

M. Bomben on behalf of SLIM5 project

Università & INFN - Trieste

Outline

- General idea
 - the "Demonstrator"
- The FSSR2 Readout Chip
 - features
 - test
 - first results
- Conclusions



General idea

the "Demonstrator"

- The SLIM5 project aims to build a "demonstrator" and test the trigger rate, resolution & efficiency for
 - low material budget Silicon trackers
 - double sided triplets (200 μm)
 - Monolithic Active Pixel Sensors (MAPS) thinned down to $\sim 100 \mu\text{m}$
 - a DAQ connected to an Associative Memory (AM) system; AM will give the "demonstrator" the trigger => data driven architecture

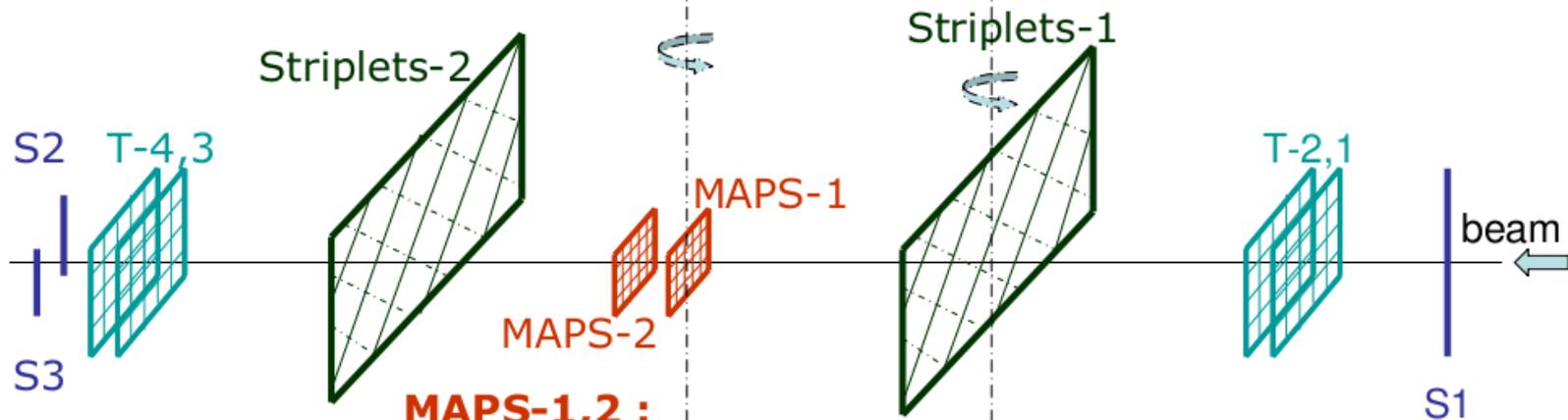
Proposed design

The Demonstrator

The "DEMONSTRATOR"

(conceptual)

S-1,2,3
scintillator
(coinc. NIM/TTL output to the DAQ)



MAPS-1,2 :
active area $\sim 10 \text{ mm}^2$
Cell: $50 \times 50 \mu\text{m}^2$ (300 \rightarrow 100 μm -thick)

Reference telescope T-1,2,3,4:
area $\sim 2 \times 2 \text{ cm}^2$
DSSD 300mm thick
25 p-side, 50 n-side mm pitch
50 mm r.o. pitch (3 chips
FSSR2/side)

Striplets-1,2:
area $1.29 \times 6.0 \text{ cm}^2$
DSSD 200 μm thick ($\angle 45^\circ$)
25 p-side, 50 n-side μm pitch
50 μm r.o. pitch (3 chips FSSR2)

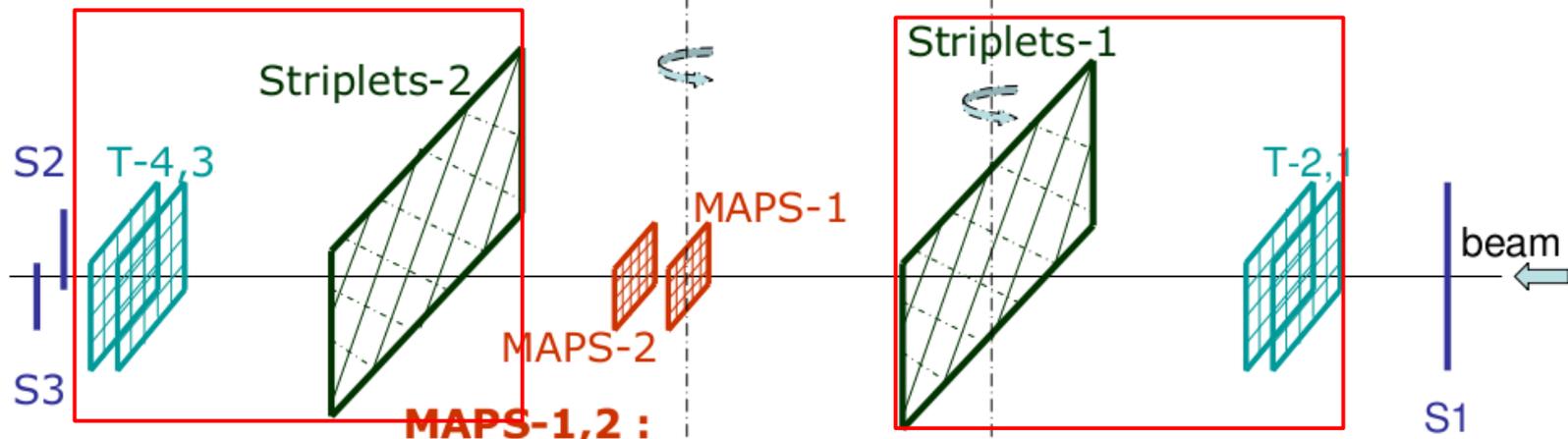
The Demonstrator

The "DEMONSTRATOR"

S-1,2,3
scintillator
(coinc. NIM/TTL output to the DAQ)

(conceptual)

Read by
FSSR2



MAPS-1,2 :
active area $\sim 10 \text{ mm}^2$
Cell: $50 \times 50 \mu\text{m}^2$ (300 \rightarrow 100 μm -thick)

Reference telescope T-1,2,3,4:
area $\sim 2 \times 2 \text{ cm}^2$
DSSD 300mm thick
25 p-side, 50 n-side mm pitch
50 mm r.o. pitch (3 chips
FSSR2/side)

Striplets-1,2:
area $1.29 \times 6.0 \text{ cm}^2$
DSSD 200 μm thick ($\angle 45^\circ$)
25 p-side, 50 n-side μm pitch
50 μm r.o. pitch (3 chips FSSR2)

Striplets

- Active area = $27 \times 12.9 \text{ mm}^2$
- $200 \text{ }\mu\text{m}$ thick double sided
- AC-coupled to metal electrode
- $\pm 45^\circ$ oriented strips
- $50 \text{ }\mu\text{m}$ pitch on p-side
- $50 \text{ }\mu\text{m}$ pitch on n-side

Telescope detectors

- Active area $\sim 17 \times 17 \text{ mm}^2$
- $300 \mu\text{m}$ thick double sided
- AC-coupled
- $25 \mu\text{m}$ pitch on p-side
 - read-out strip pitch: $50 \mu\text{m}$
- $50 \mu\text{m}$ pitch on n-side

Detector capacitance @ Bias = 40 V
strip P-side

4.83 pF @ 10kHz

4.34 pF @ 100kHz

4.20 pF @ 1 Mhz

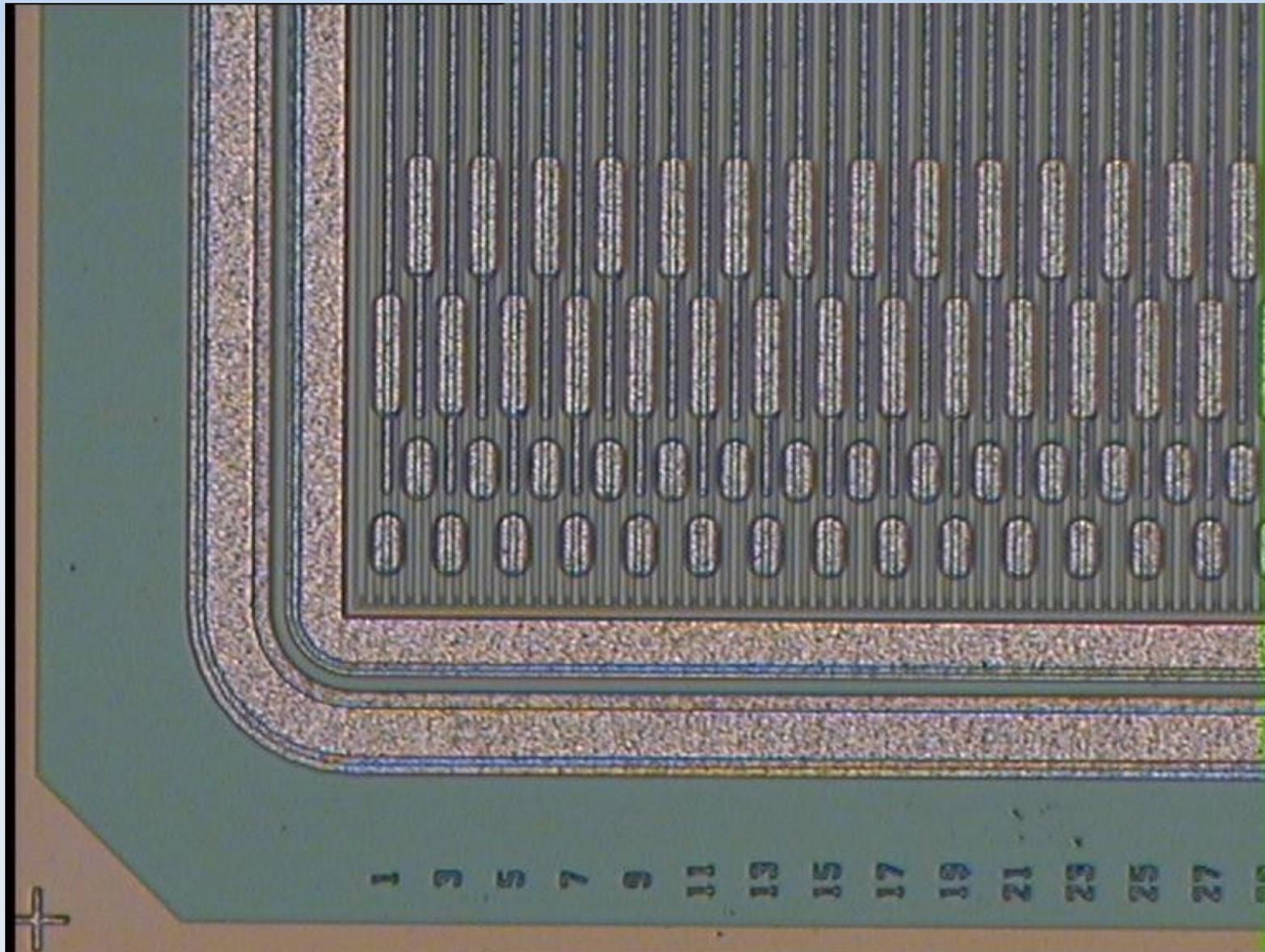
strip N-side

5.67 pF @ 10kHz

5.37 pF @ 100kHz

5.17 pF @ 1 Mhz

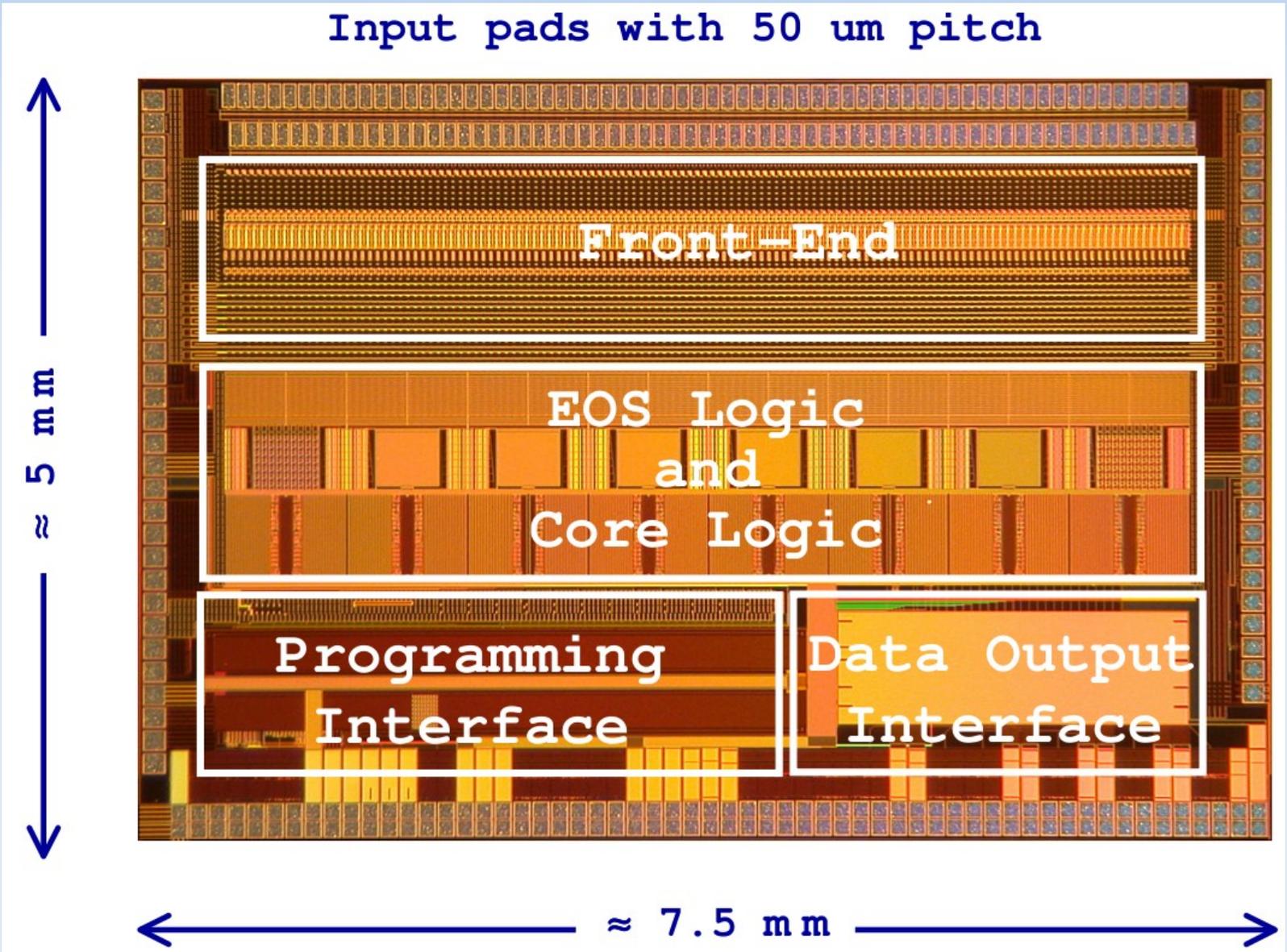
Tele-detector, p-Side





The FSSR2 chip

FSSR2 chip



FSSR2 chip characteristics

- Fermilab Silicon Strip Readout Chip V2
- 128 analog channels, address, time, and magnitude information for all hits
- Self-triggered readout architecture with no analog storage,
- It can be read up to 60 MHz
- It was designed for the BTeV Forward Silicon Tracker; the FSSR2 is suitable for a wide range of applications with microstrip detectors

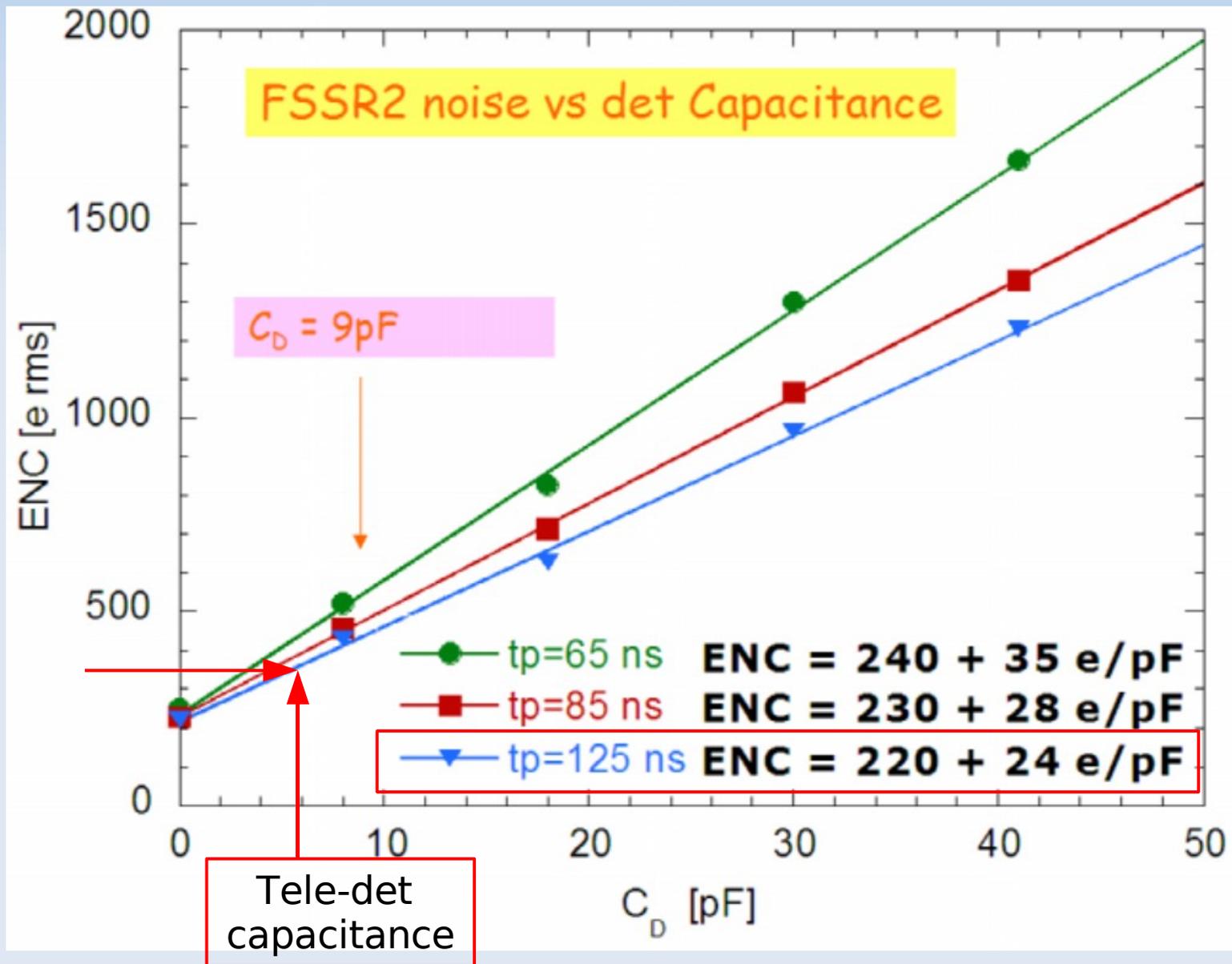
More info on FSSR2

- **Data driven architecture – no trigger**
- Operation at 132 ns (2% strip occupancy), 264 ns, or 396 ns (6 % strip occupancy) beam crossing
- Tolerance to total ionizing dose (5 Mrad) and single event effects (SEU)
- Power < 4 mW/channel
- Design spec's:
 - ENC < 1000 e rms @ CD=20 pF
 - Threshold dispersion < 500 e rms

... and more!

- 3bit flash ADC
- Programmable Gain and Shaper
- Internal pulser
- data to be read can be splitted in 2, 4 or 6 lines; this is perfect for high rate!
- internal Baseline restorer
- With a total load of ~ 9 pF \Rightarrow ENC ~ 500 e⁻rms
- For a **200 μ m** silicon thickness, the **S/N** ratio for **MIPs** will be about **26**.

Noise & Det. Capacitance

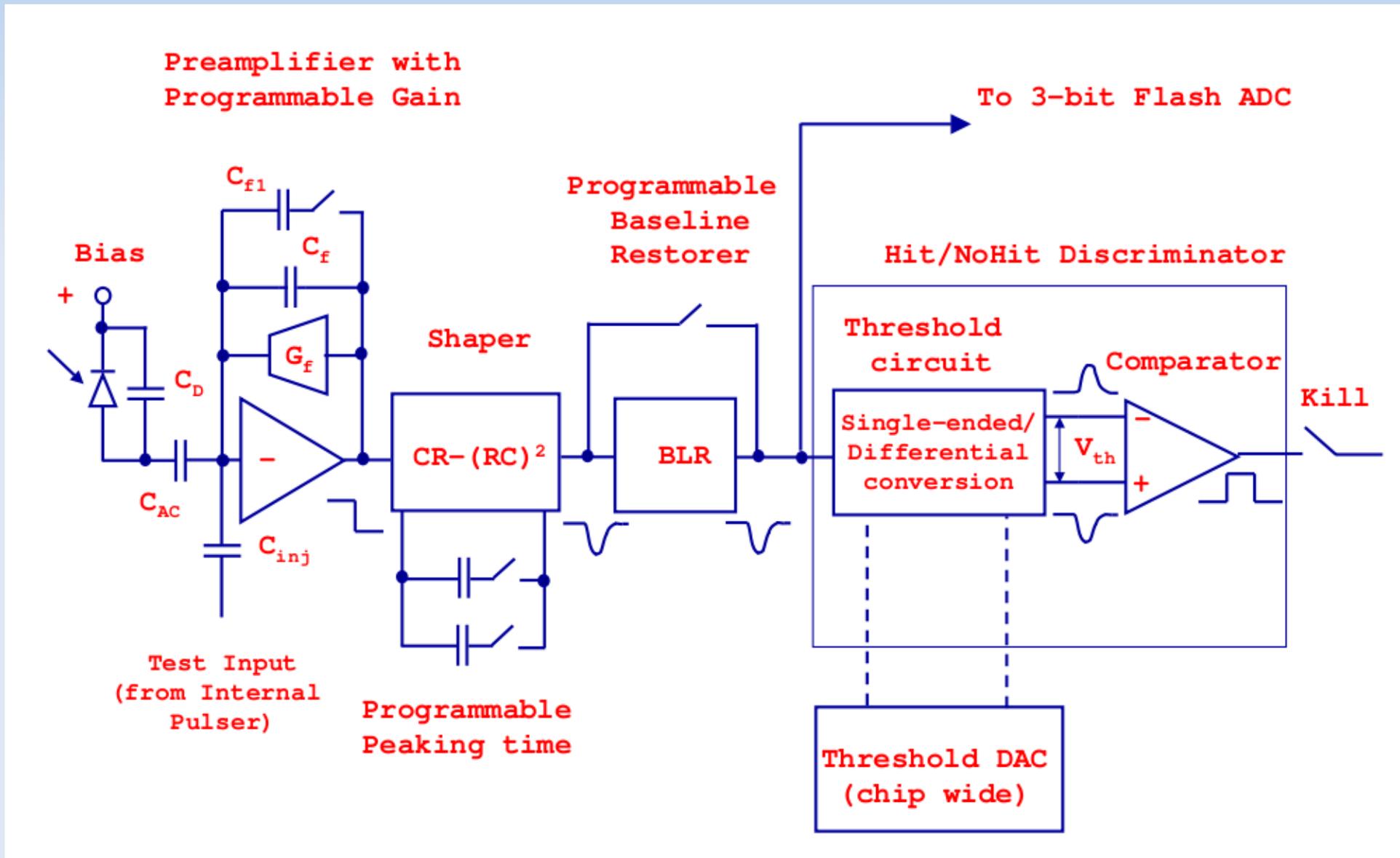


Nominal gains

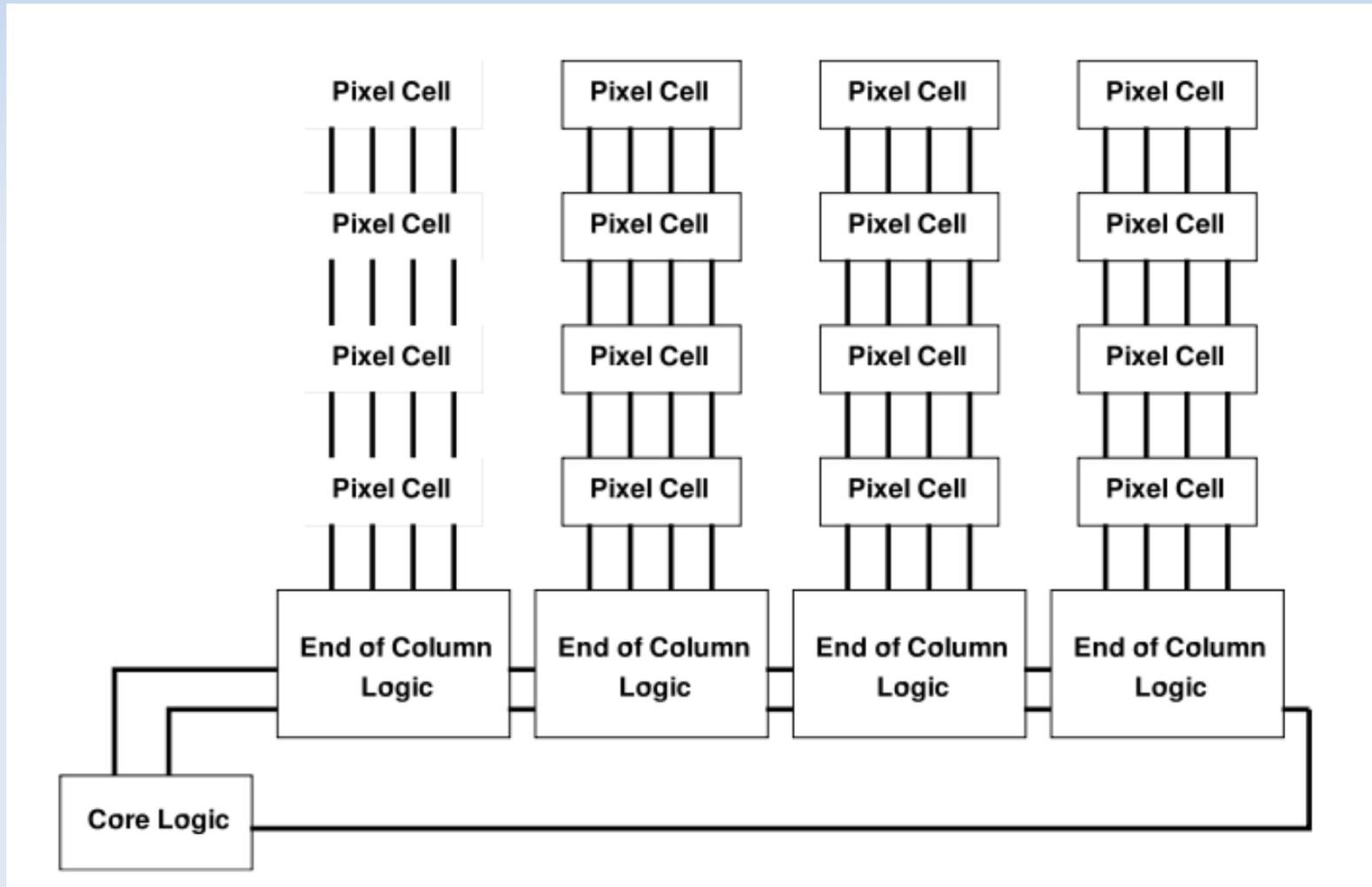
Shaping time [ns]	Feedback capacitance [fF]	Gain [mV fC ⁻¹]
125	150	93
85	150	96
65	150	101
125	100	137
85	100	142
65	100	149

Table 4.1: *FSSR nominal gains expected from simulations.*

Analog section



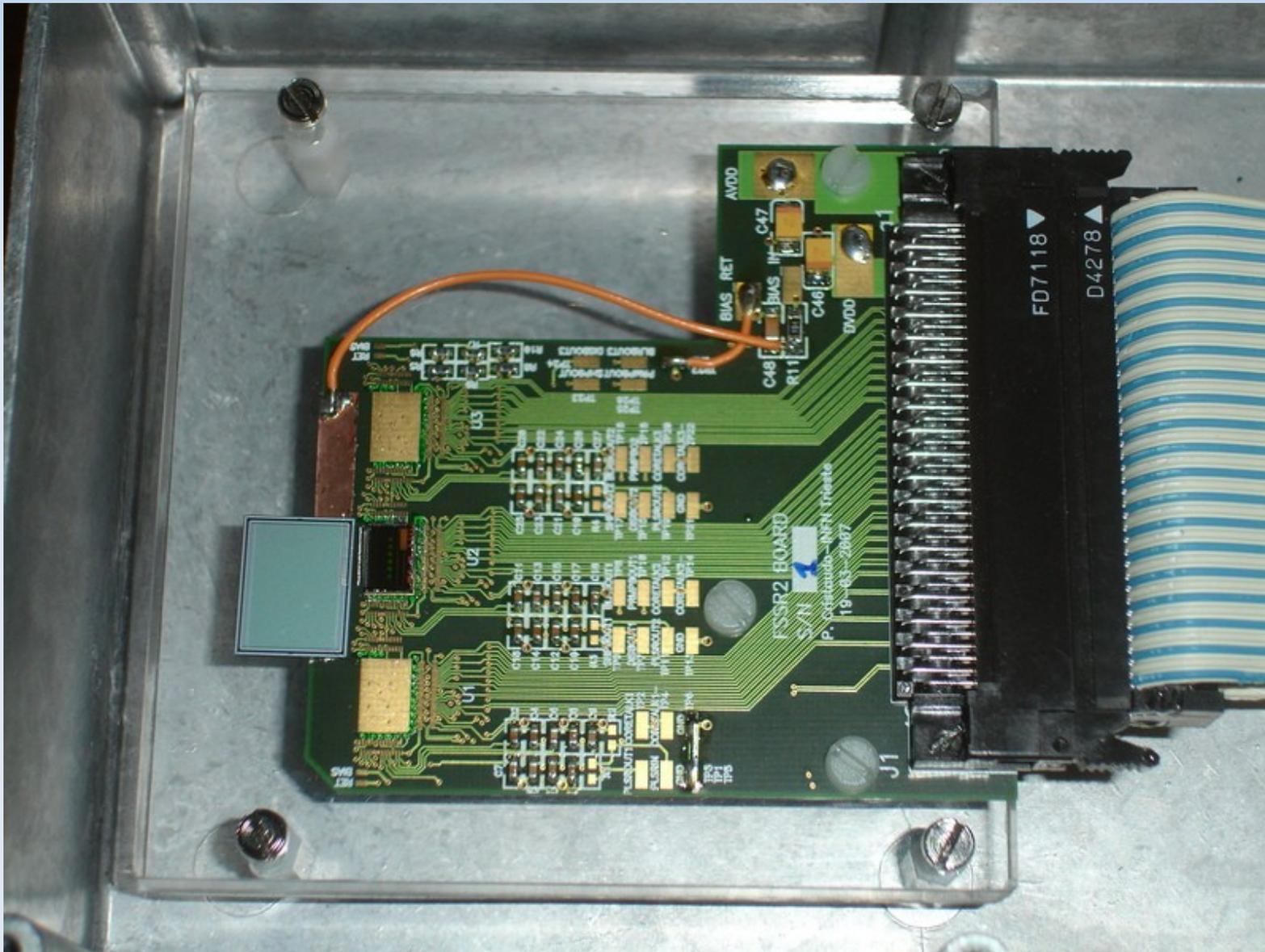
Logical structure



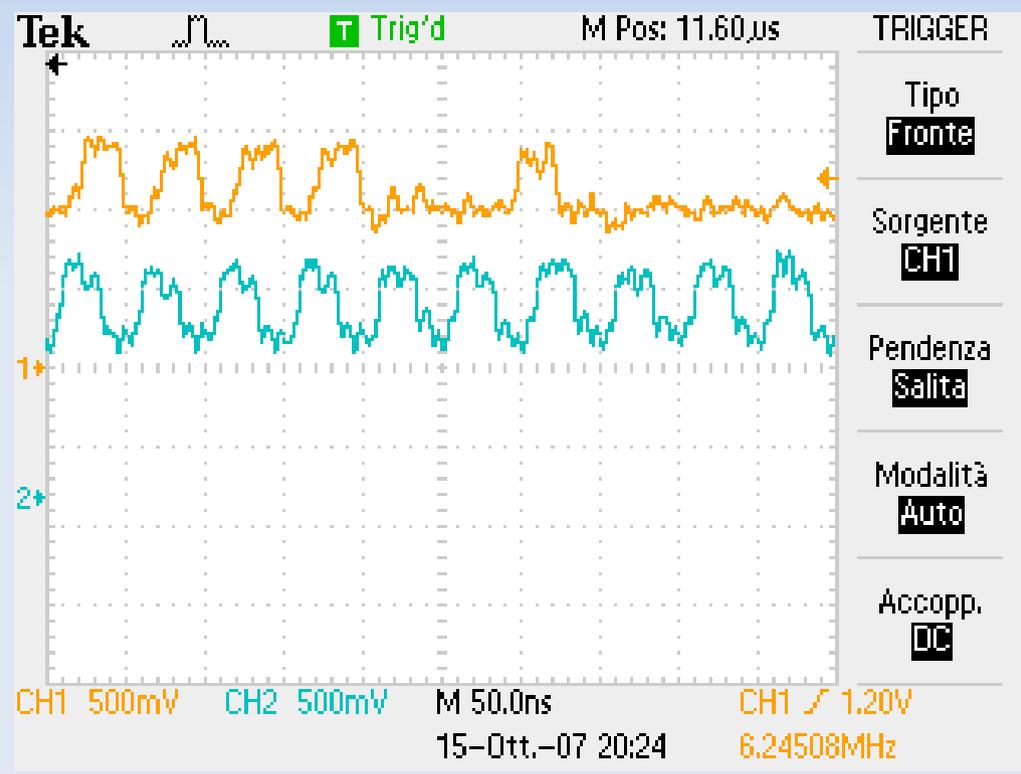
Trieste setup



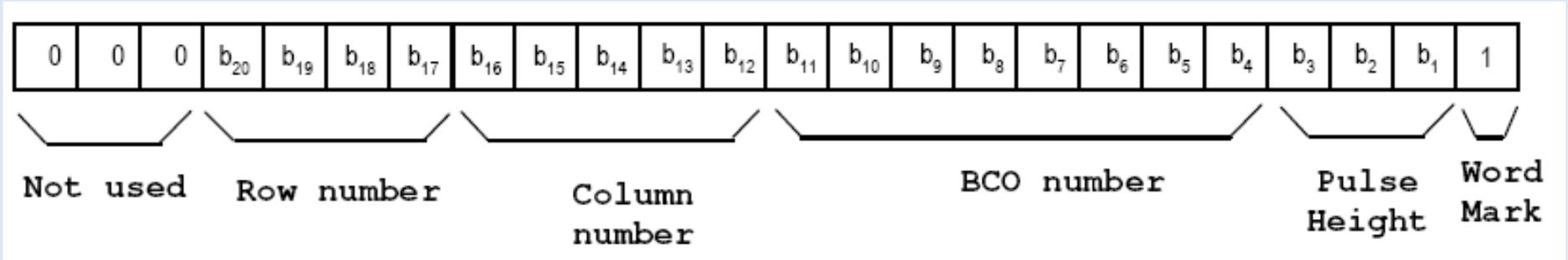
FSSR2 hybrid



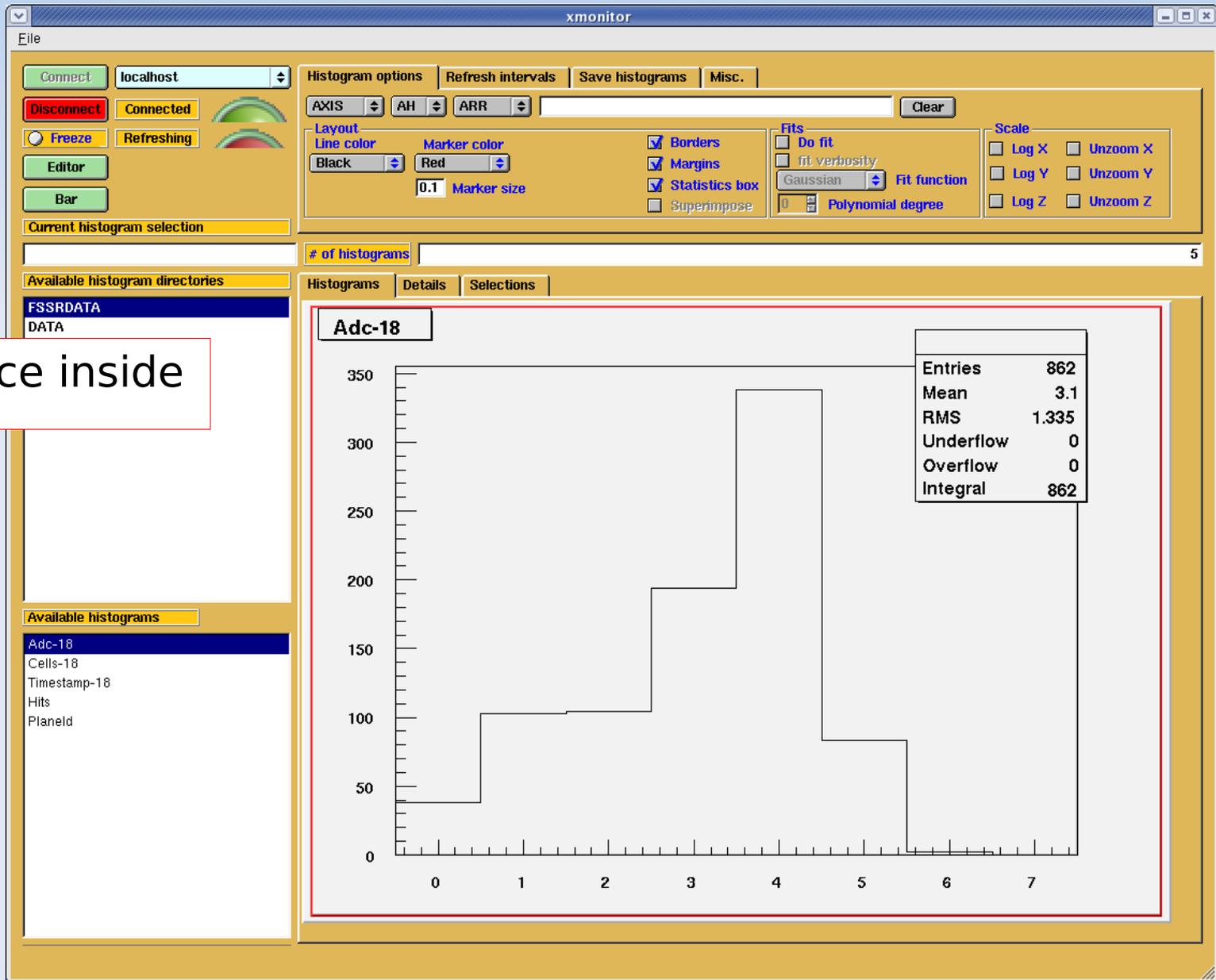
Some signals



- **Yellow** line is the data word
- **Cyan** is Out Clock



A run with FSSR2 chips

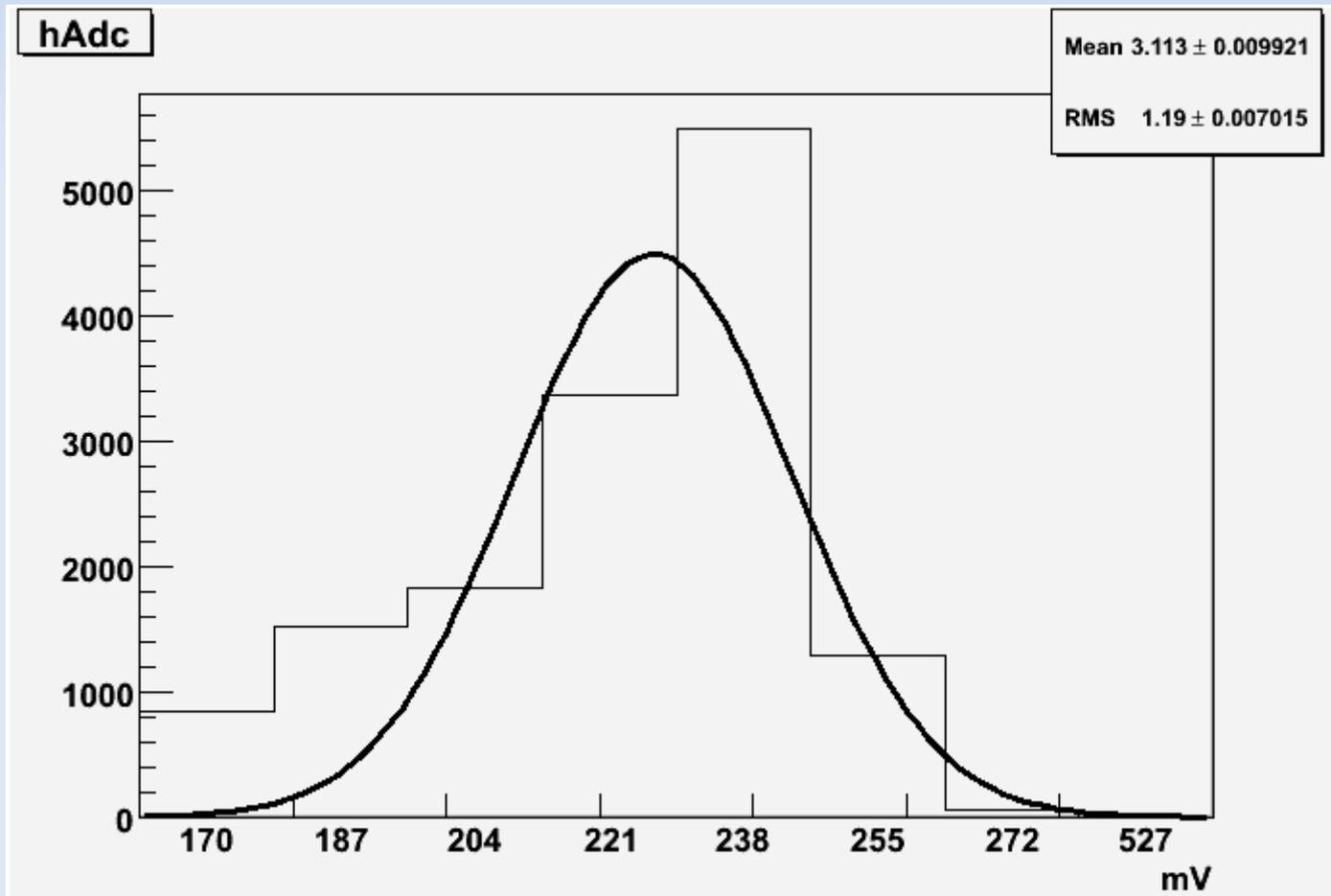


^{241}Am source inside

S/N for 2/3 of a MIP

S = DAC value for peak-bin
 N = DAC value for noise-suppressed threshold

Peaking Time = 125 ns
 low gain
 Estimated gain = 95 mV / fC



S/N ~ 18 for ²⁴¹Am 60 keV gamma line

Conclusions

- We want to test the possibility for low material budget silicon detectors with Level 1 trigger capabilities
- Trigger will be given by Associative Memory algorithms
- A fast, data driven architecture is mandatory
- FSSR2 ROC is a perfect candidate
- We are working to fully characterize FSSR2
- Moving towards a beam test in 2008!

That's it!

Backup slides

Data driven architecture

- The idea is to use silicon detectors as part of the Level 1 (L1) trigger
- So far silicon detectors were used only for L2 triggers
 - BTeV was going to use this feature, but...
- A L1 silicon-based trigger is essential in a Flavor factory
 - to complement the calorimetry information

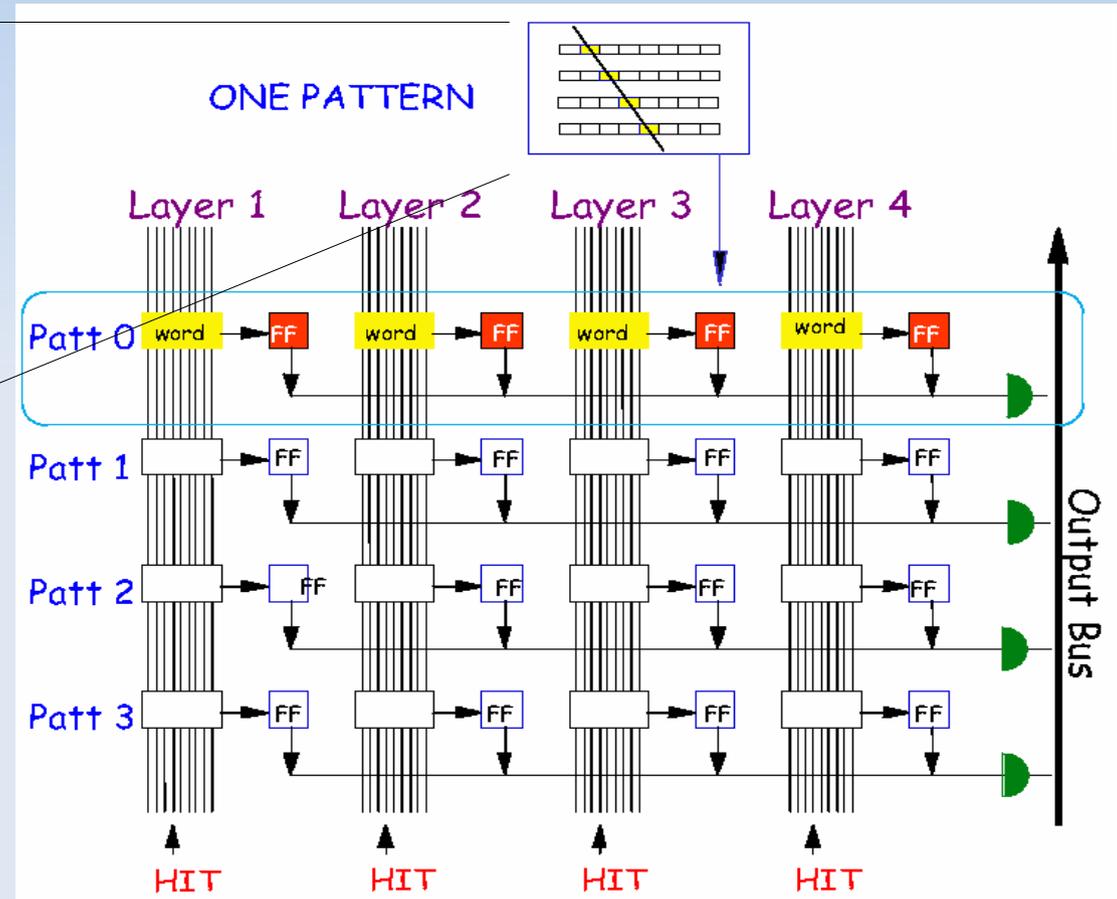
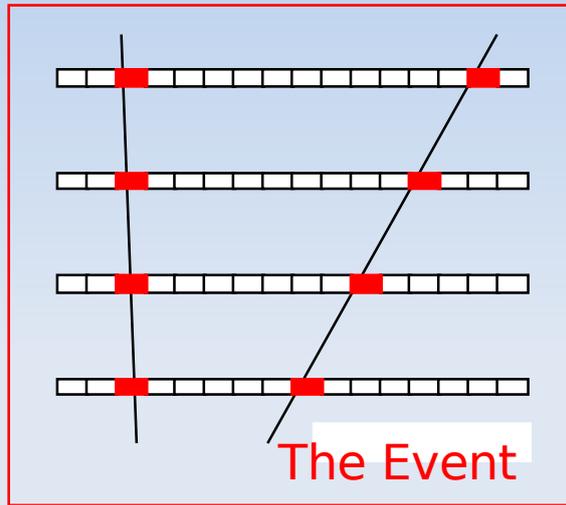
Timestamps

- The chip itself should carry information on the Pulse Height and
- **on the timestamp too!**
- In this way the information from the chip is complete and you can build triggers directly from silicon detectors too.
- Data from the chips can be fed directly in Associative Memory

Track reconstruction

- Trigger will be provided by associative memories (AM)
- The AM will be loaded with all possible patterns
- During the run a pattern will be chosen and the corresponding track parameters will feed the trigger logic

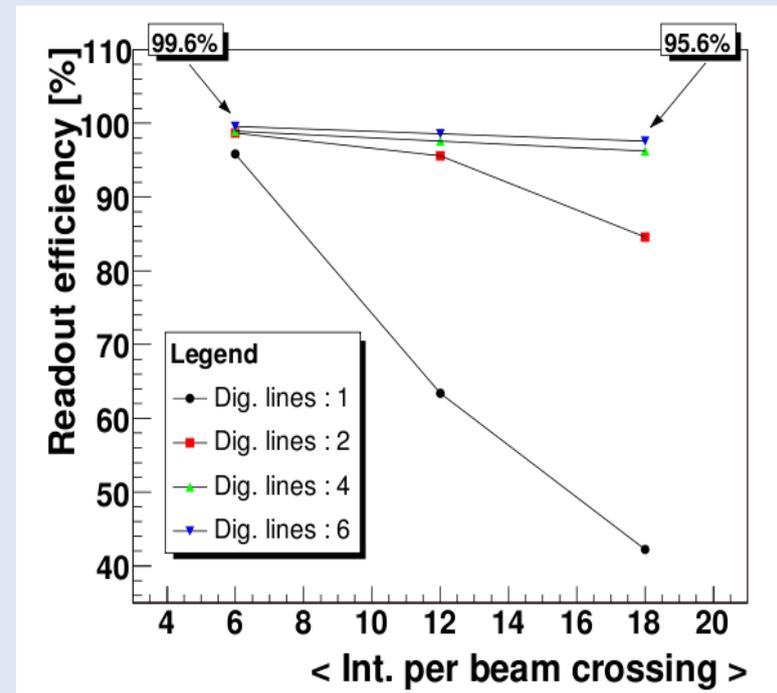
AM for pattern matching



- Dedicated device: **Maximum** parallelism !
- Each pattern with **private comparator**
- Tracks found during **detector readout** !

FSSR2 hybrid

- New design in Trieste
- 3 chip pads
- splitted lines readout fully implemented
 - 1, 2, 4 or 6 readout lines per chip



The DAQ chain

- A **EDRO** board matched on
- the **Associative Memories**
- through the **VME bus**

Slightly different setup

- @TS We are using a PCI-card based setup
 - It is inspired to BTeV test-stand

