

Update on Cluster Counting Technique

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Super-B workshop 14 Feb 2008

Summary

- ❑ Cluster Counting
 - ✓ Simulations
 - ✓ Measurements Setup
 - ✓ SI-telescope

- ❑ DAQ development
 - ✓ FE-ADC ASIC in Lecce
 - ✓ DAQ block diagram
 - ✓ FPGA based DAQ

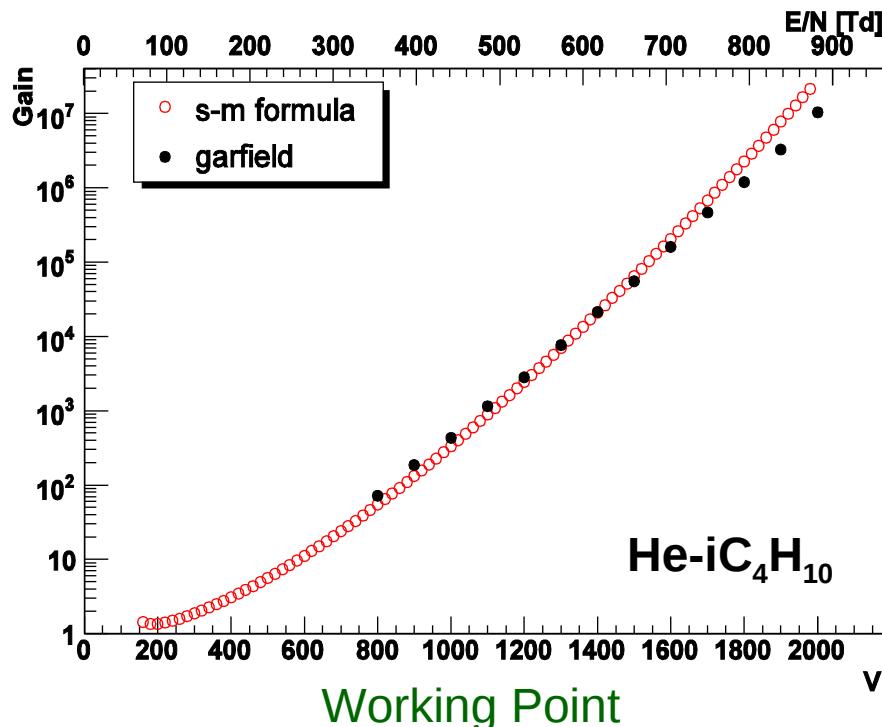
- ❑ Conclusions

CLUCOU Simulation: Gas parameters

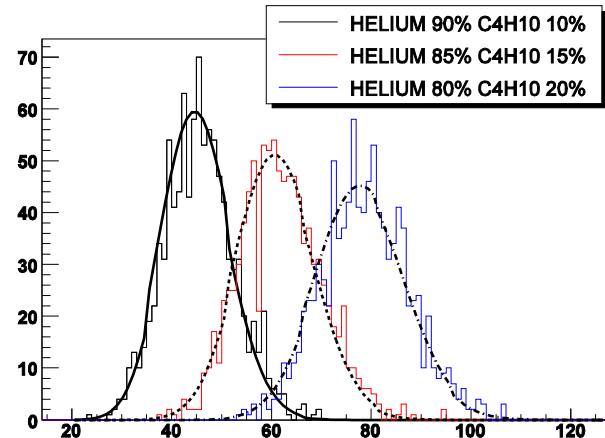
Based on packages: HEED, MAGBOLTZ, GARFIELD9 and ROOT

Number of clusters/cm and e-/cluster

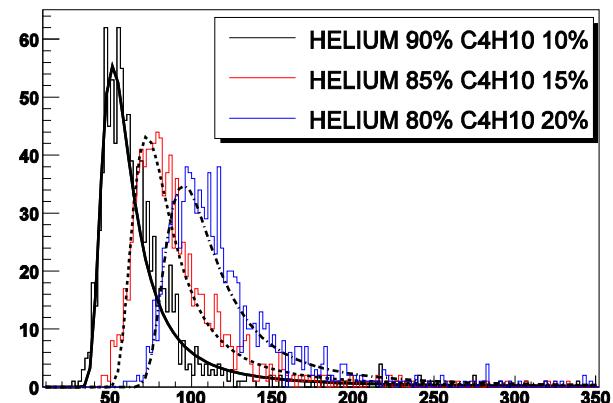
He-iC ₄ H ₁₀	90%-10%	85%-15%	80%-20%
n _{cl} /cm	11.3	15.3	19.6
n _{el} /n _{cl}	1.60	1.62	1.62



Clusters Poisson ionization statistics

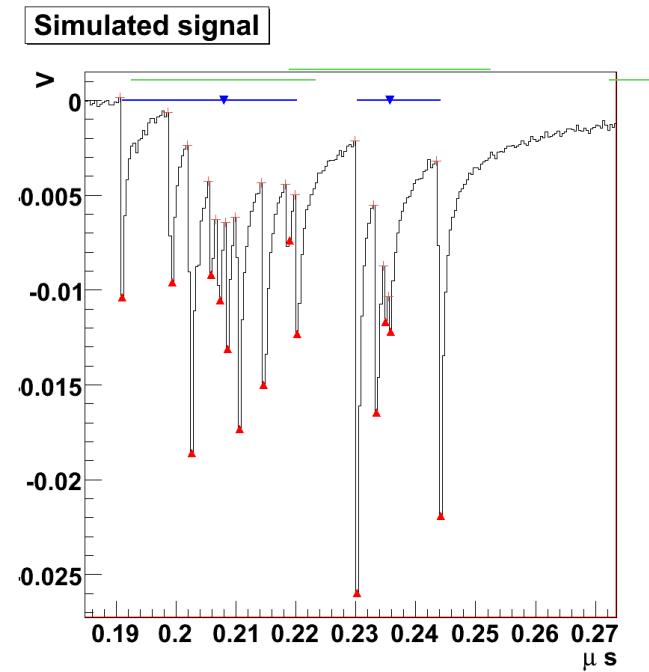
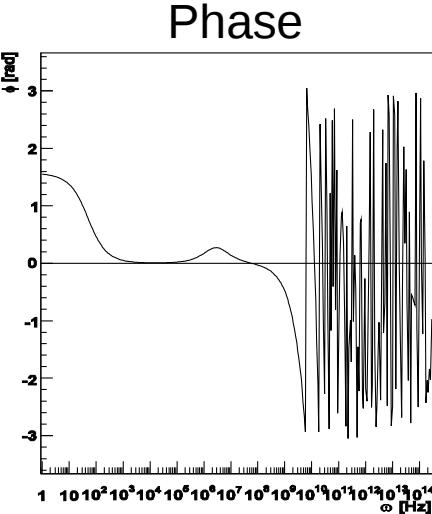
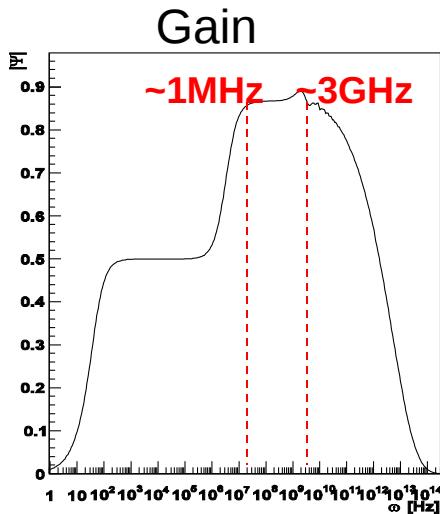
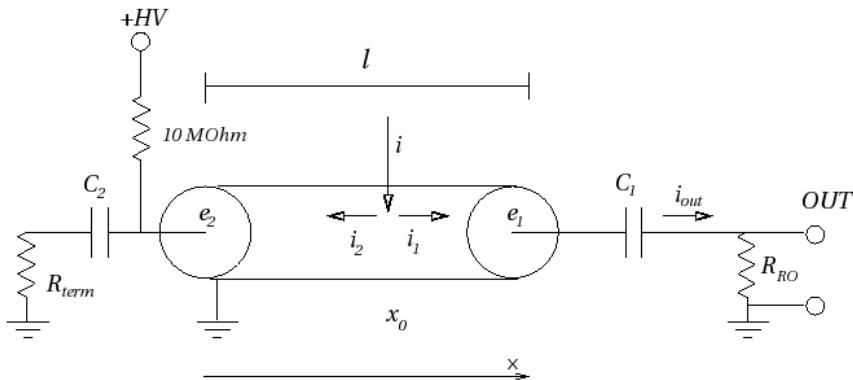


Electron Landau ionization statistics



CLUCOU simulations:

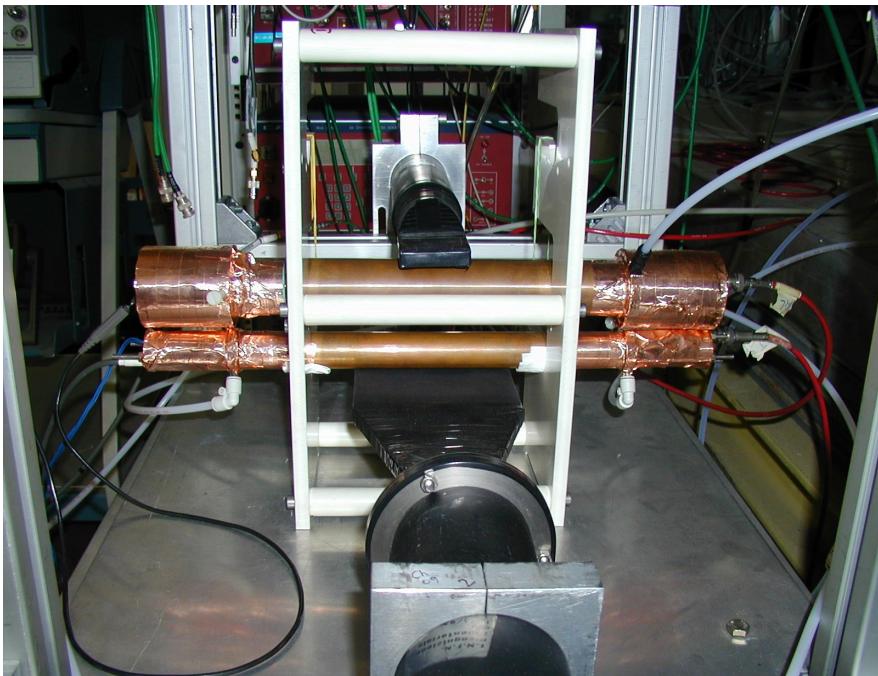
FE Response



Peak Finder after Front-End

Atlas internal note MUON-NO-105 (1995) and PS-SPICE

CLUCOU measurements: Setup



Gas Mixture = 90 % He 10 % iso-C₄H₁₀

Drift tube ray = 1.4 cm

Wire diameter = 25 micron

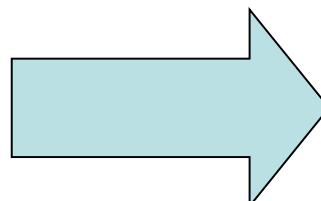
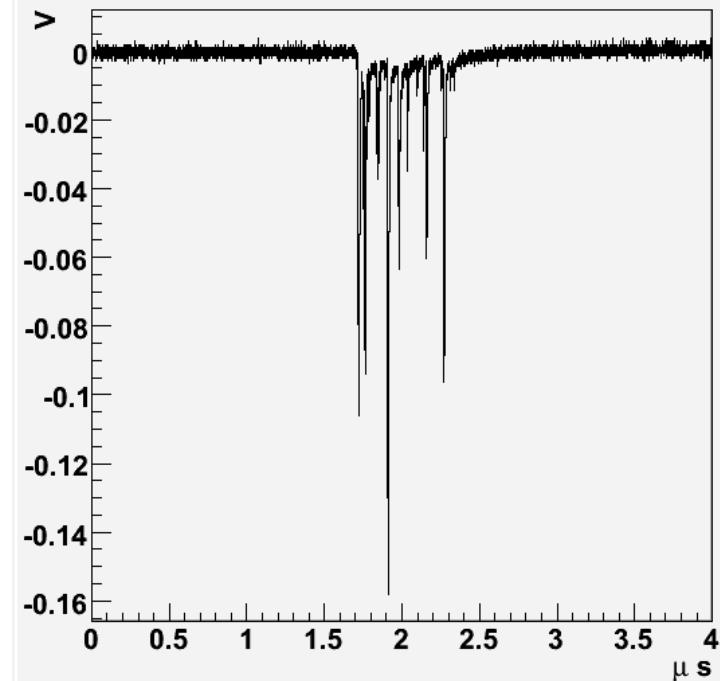
Tube length = 30 cm

High Voltage = 1750 V

Amplifier Gain = 10

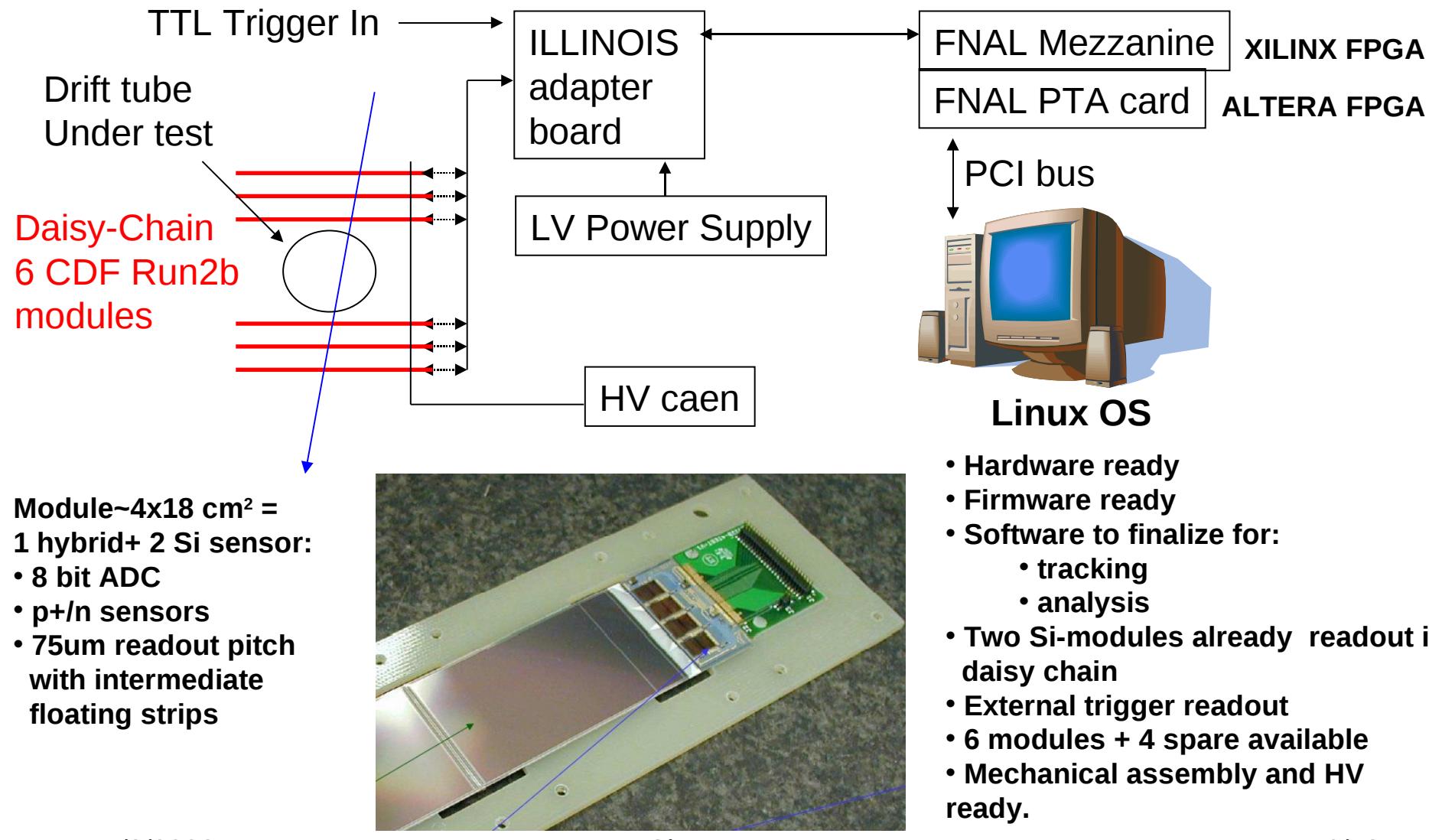
Amplifier BW = 500 MHz

Signal on First Channel



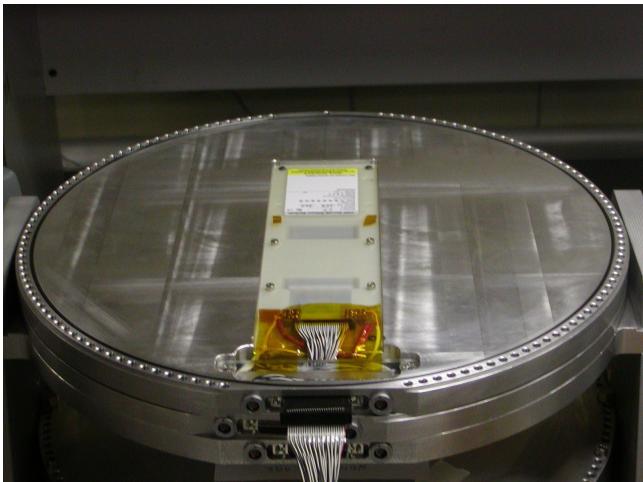
- Peak Finder
- Ionization statistics
- RT relation vs n-th cluster
- track Impact parameter
- Si-Telescope

CLUCOU measurements: Si-Telescope (I)

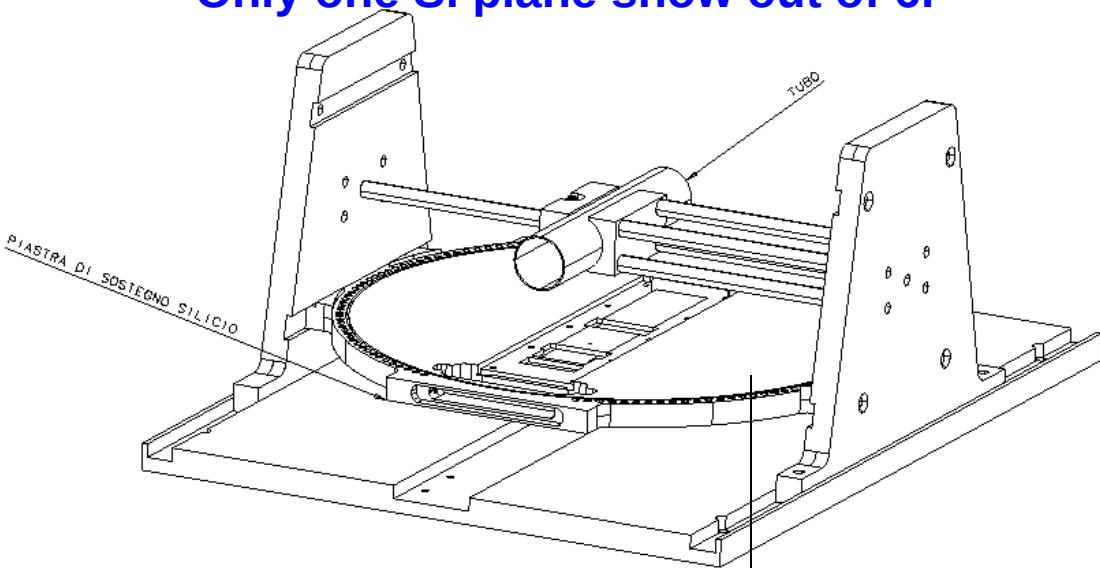


CLUCOU measurements: Si-Telescope (II)

6 plane microStrip-Si telescope



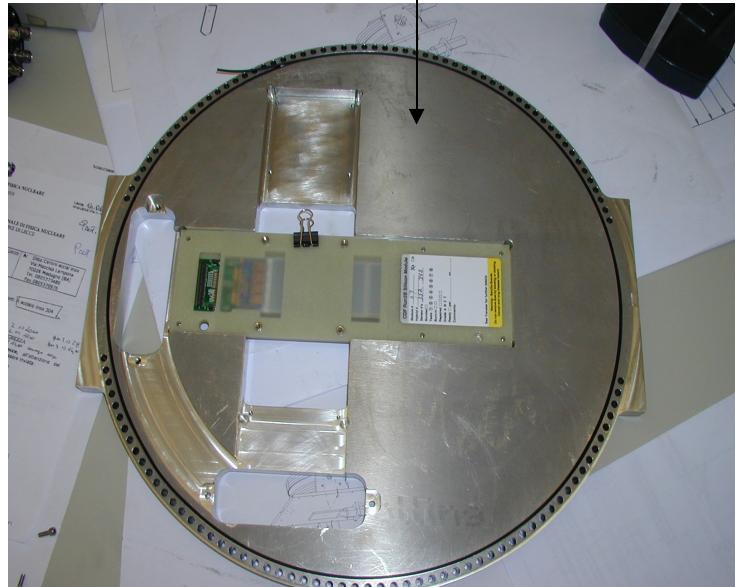
Si - telescope and Device Under Test.
Only one Si plane show out of 6.



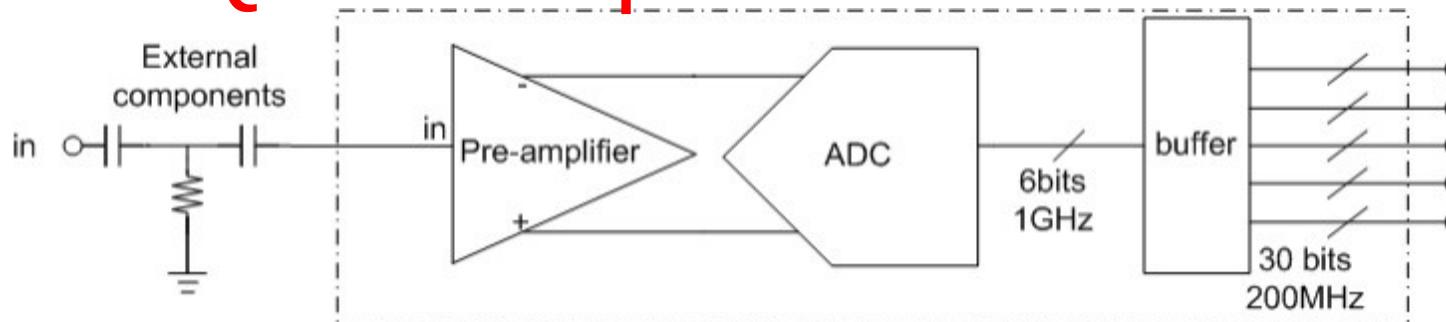
- Full adjustable angles 1.2° step
- Easy to upgrade to more planes

Next: Tracking on cosmics
- X_0 Material not optimized yet
14/2/2008

Clucou status



DAQ development: FE-ADC ASIC in Lecce



- Test board delivery in few weeks
- 72 Chips from foundry today

i.Preamplifier features

Parameter	Value
DC-gain	21dB
-3dB Bandwidth	500MHz
Current Consumption	12mA
Noise	$291\mu\text{V}_{\text{rms}}$

*A CMOS high-speed front-end for cluster counting techniques in ionization detectors
Proceeding a 2-nd IEEE International Workshop on Advances in Sensors and Interfaces, Bari, 26-27 Giugno 2007*

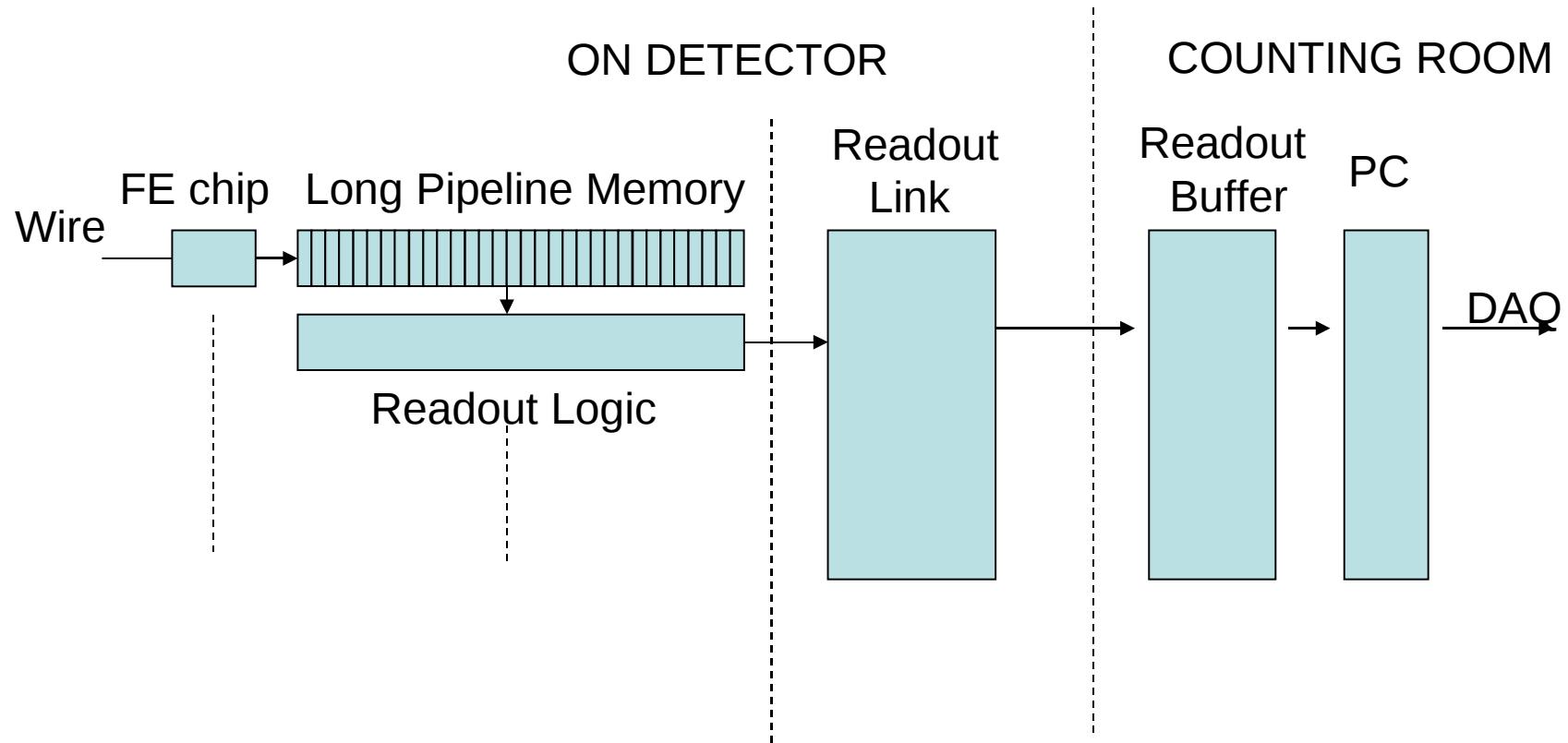
ADC features

Parameters	Values
Technology	0.13μm CMOS
Supply Voltage	1.2V
Resolution	6 bits
Sample rate	1Gsa/s
Clock Frequency	1GHz
Full Scale input range	160mV
SNR(@10MHz, FS)	34.5dB
SNDR(@10MHz, FS)	34.1dB
ENOB	5.4bits

S. D'Amico and A. Baschirotto Engineering designers (Lecce University - Engineering department)

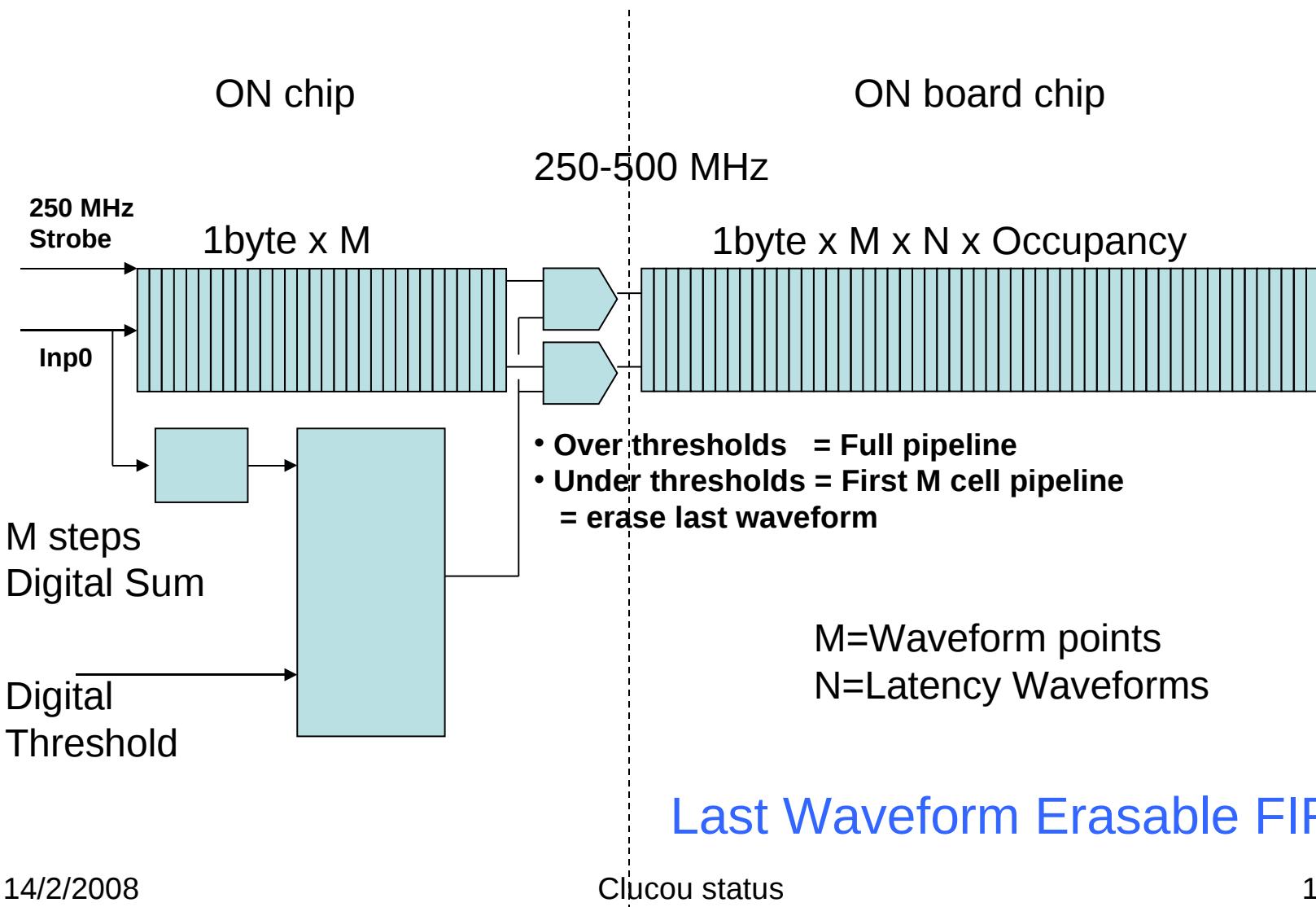
DAQ development: Conceptual design (1)

1. Pipeline the data in Local Memory Buffer
2. Move data out by Readout Link
3. CLUCOU algorithm implemented in FPGA



DAQ development: Conceptual design (2):

Zero Suppression Algorithm



DAQ development: Fermilab PCI board



Short term plans:

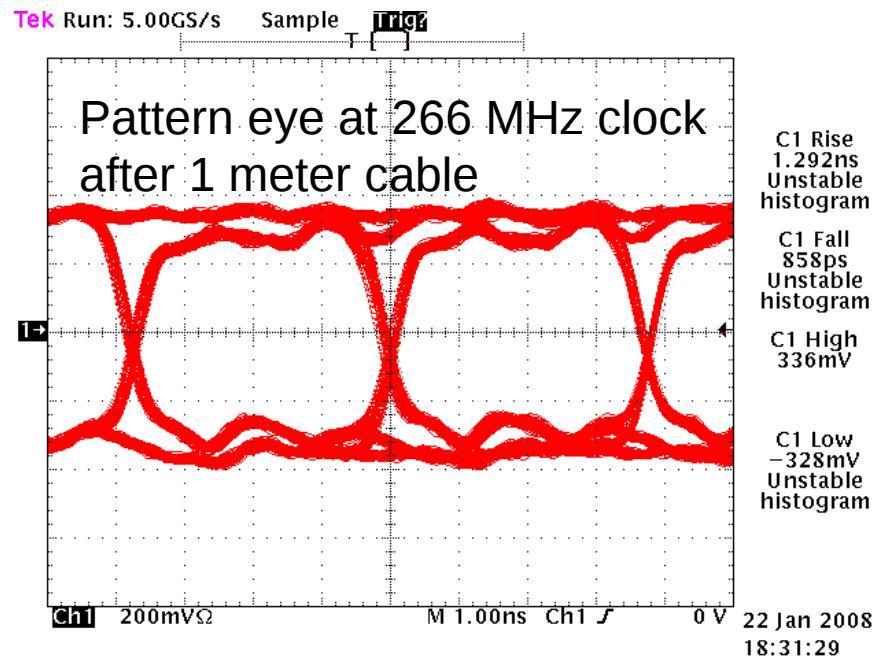
- Readout 1 to 5 CLUCOU_V1 chips
- Implement Last WF Erasable FIFO
- Implement Peak Finder
- Implement Data-Serializer
- ...

New PTA Fermilab
from ESE department

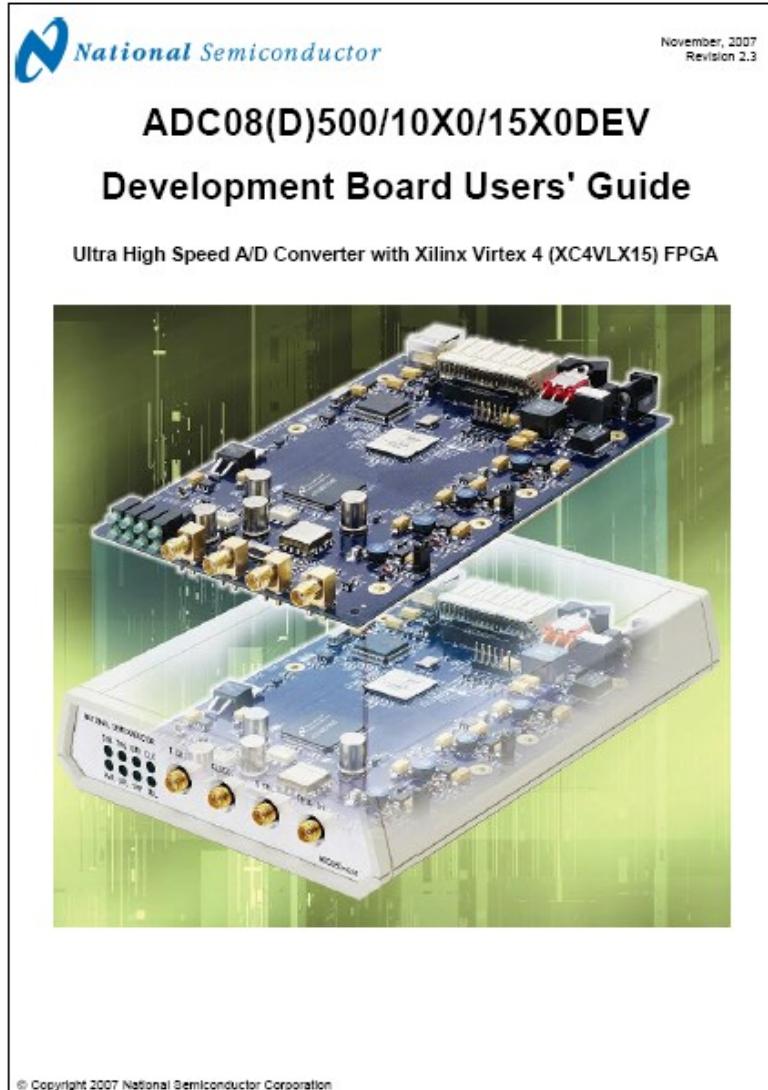
- PCI bus
- 80 LVDS I/O
- VirtexIV FPGA
- We have one in

Many thanks to Fermilab
ESE department
(M. Turquetti, L. Uplegger
and S.Kwan)

Lecce



DAQ development: NS Development Board

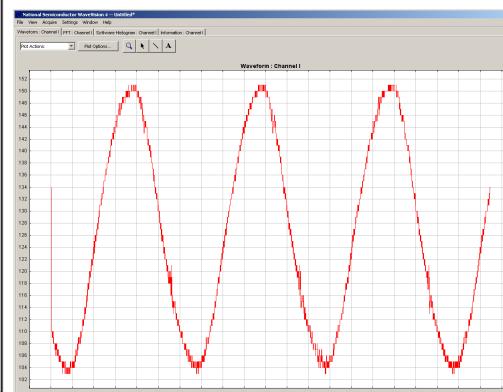


ADC08D500DEV:

- 2 Channels
- 8 bit @ 1.5Gs/sec
- dynamic range +/-280 mV
- VIRTEX-IV FPGA
- In/Ext clock
- Vision Software

GOALS

- Both end drift-tube readout
- FPGA firmware development
- Benchmark for real DAQ based on:
 - FE-ADC Lecce-ASIC
 - GHz Multi clock distribution
 - CLUCOU Data Combiner Board



Example of 1.5 GHz sampling waveform data capture in Lecce.

Conclusions

- We have in place all we need to prove the CLUCOU basic idea and real implementation:
 - ✓ Efficient peak finder on real data
 - ✓ Measurements of ionization statistics
 - ✓ Measurements of n-th cluster r-t relation
 - ✓ Impact parameter measurements
 - ✓ VLSI Chip testing
 - ✓ Proof of principle CLUCOU DAQ
 - ✓ Cost estimate of a final system
- This year progress are crucial
- Work strongly interfere with ATLAS RPC commissioning where we are heavily involved