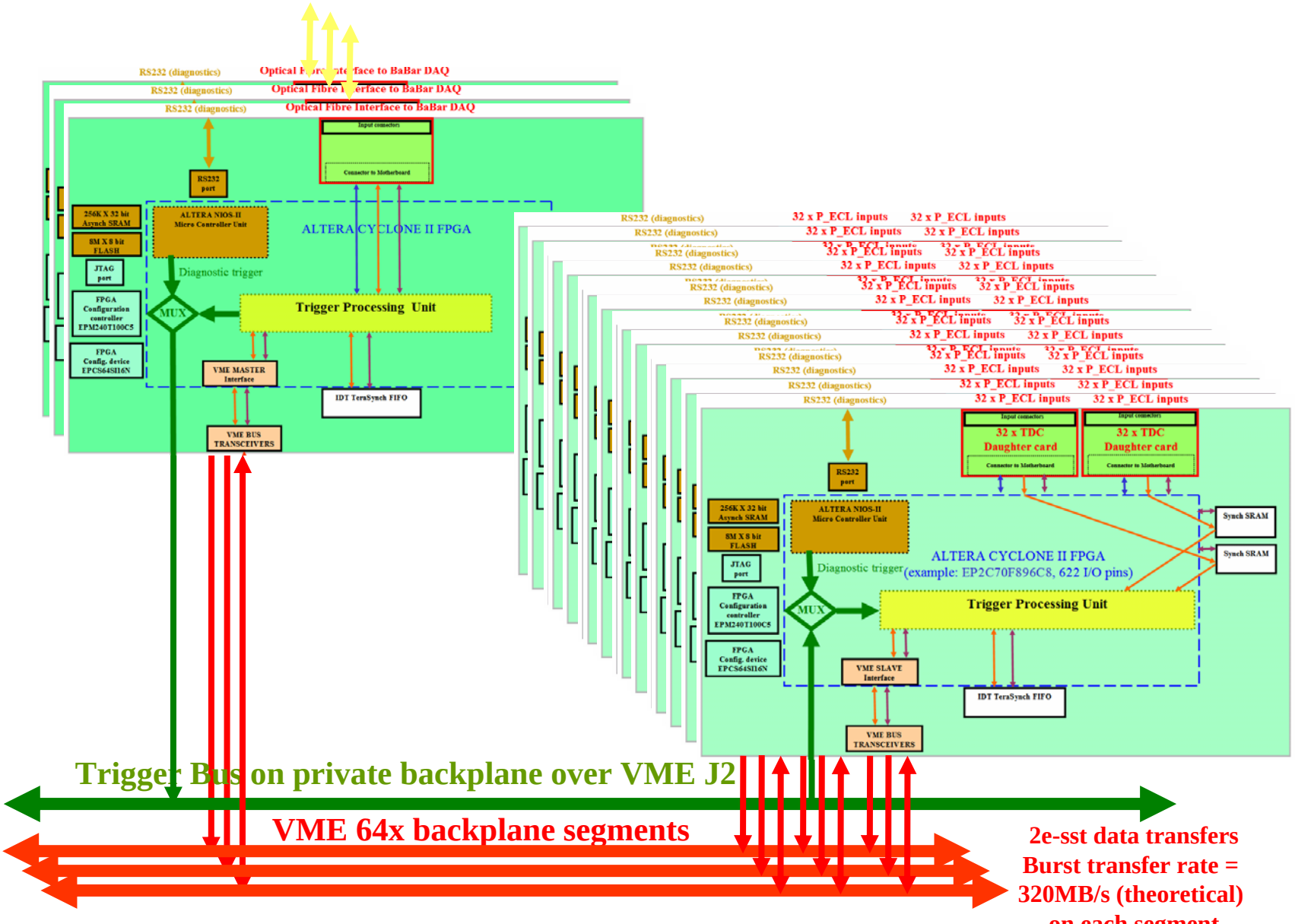
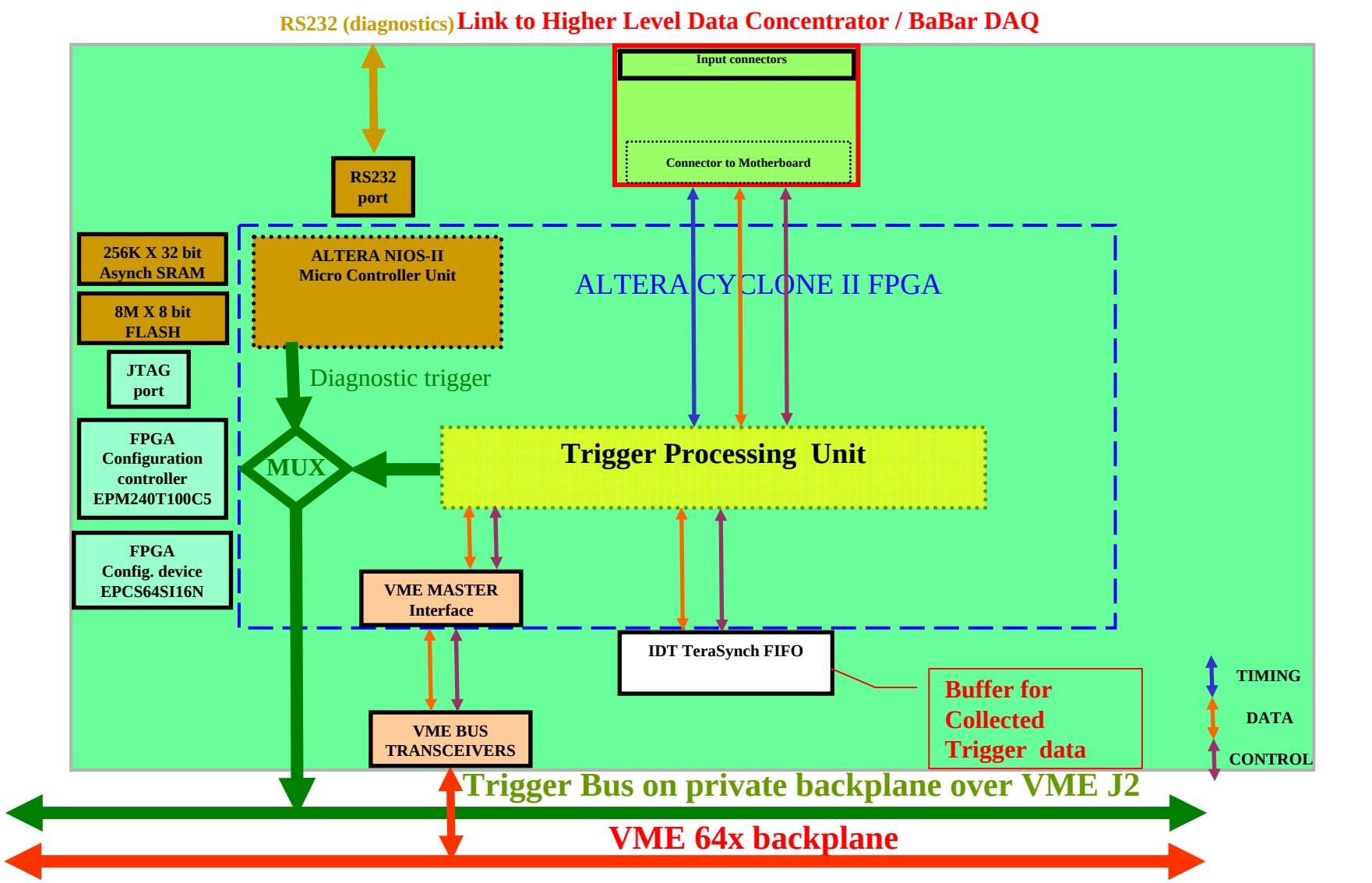
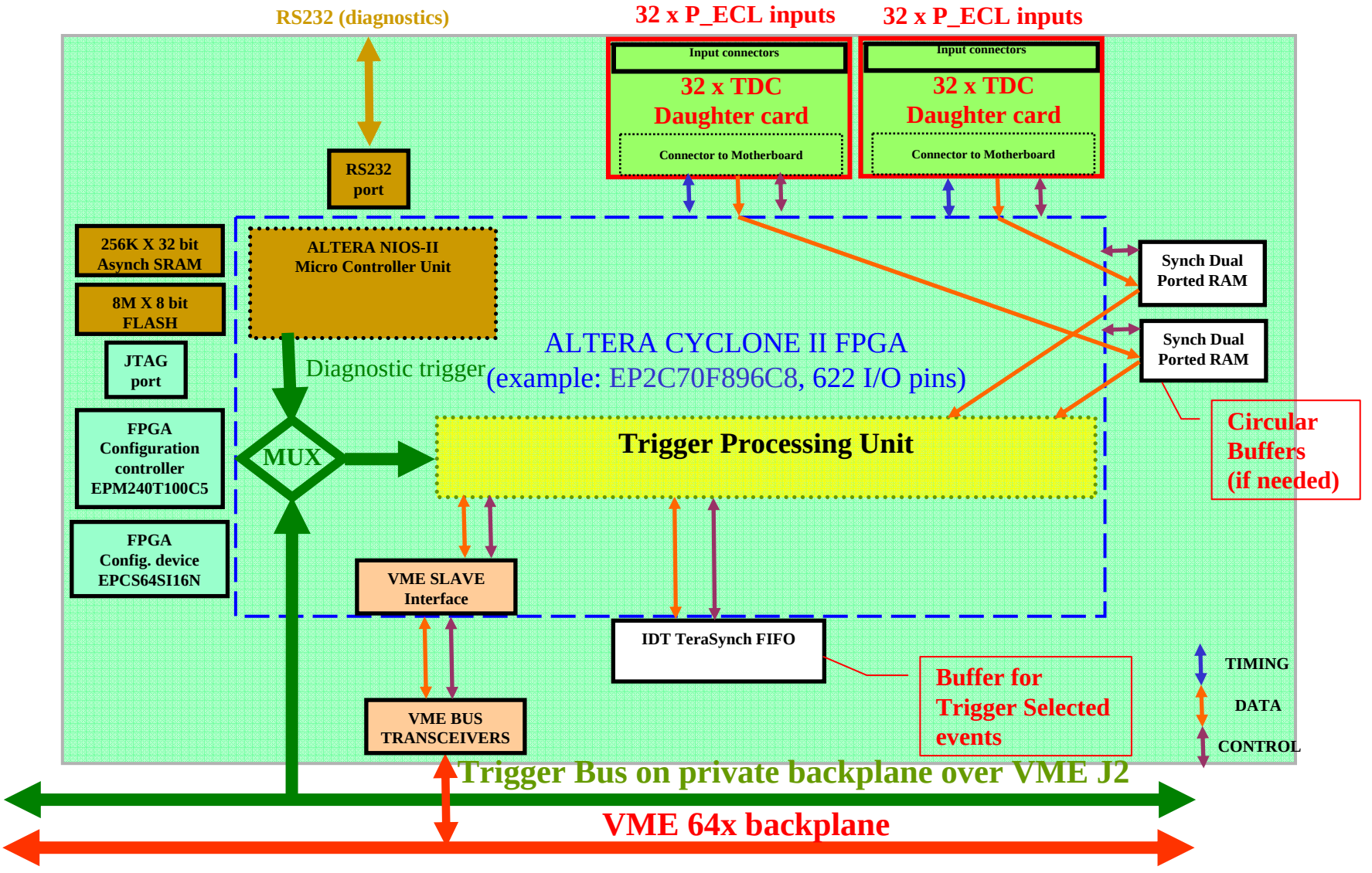


Very Preliminary layout of a modular crate of TDC Front End for the SUperB IFR

INFN Istituto Nazionale di Fisica Nucleare



Very Preliminary layout of a BABAR DAQ Interface card for the SUperB IFR Front End:
It controls TDC cards and collects data acting like a VME Master with 2e-sst capacity


RS232 (diagnostics)
32 x P_ECL inputs
32 x P_ECL inputs
Input connectors
32 x TDC
Daughter card
Connector to Motherboard
Input connectors
32 x TDC
Daughter card
Connector to Motherboard
RS232
port
256K X 32 bit
Asynch SRAM
8M X 8 bit
FLASH
JTAG
port
FPGA
Configuration
controller
EPM240T100C5
FPGA
Config. device
EPCS64SI16N
ALTERA NIOS-II
Micro Controller Unit
Diagnostic trigger
MUX
ALTERA CYCLONE II FPGA
(example: EP2C70F896C8, 622 I/O pins)
Trigger Processing Unit
Synch Dual
Ported RAM
Synch Dual
Ported RAM
Circular
Buffers
(if needed)
VME SLAVE
Interface
IDT TeraSynch FIFO
Buffer for
Trigger Selected
events
TIMING
DATA
CONTROL
VME BUS
TRANSCEIVERS
Trigger Bus on private backplane over VME J2
VME 64x backplane
Very Preliminary layout of a 64 input TDC card for the SUperB IFR Front End

SuperB IFR TDC Front End: numerology

·Assuming SiPM transducers applied to Minos-like radiation detectors

·ASSUMING THAT NO PULSE HEIGHT INFORMATION IS NEEDED FOR TIME-WALK CORRECTION (OR THAT THE CORRECTION IS PERFORMED WITH A CONSTANT FRACTION DISCRIMINATION CIRCUIT)

Estimated rate at the inputs of the SuperB IFR TDC cards: 500KHz / channel

Estimated SuperB Level_1 accept rate : 150KHz

⇩

Let's assume that each channel is selected by a trigger about 1/3 of the times

⇩

Let's assume that the address+timing information for each hit is coded into 32 bits.Timing may be referred to the trigger timestamp, included in the event header with the board_ID, to compact the size of the timing information

⇩

Each board produces a data flow of: 64/3 channels * 4 Bytes * 150KHz = 13 MB/s

⇩

Data from 8 TDC boards could be sinked by one SuperB-DAQ interface board -> the Data Transfer Backplane in the crate would be split into 2 segments each with 8 TDC boards and one DAQ_Interface

⇩

Assuming a channel count of 9000 then 9 IFR-TDC crates would be needed -> some "data concentrator" could be used to reduce the number of links to the SuperB DAQ

Very Preliminary layout of a 64 input TDC card for the SuperB IFR Front End : rate estimates

Available online at www.sciencedirect.com
SCIENCE DIRECT®
ELSEVIER
Nuclear Instruments and Methods in Physics Research A 518 (2004) 493–494
NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A
www.elsevier.com/locate/nima

A new drift chamber TDC readout for the high intensity program of the NA48 experiment

R. Arcidiacono[a,1], N. Cartiglia[a,b], S. Chiozzi[c], M. Clemencic[a,b], A. Cotta Ramusino[c], C. Damiani[c,d,*], A. Gianoli[c], L. Milano[c,d], R. Malaguti[c], F. Petrucci[c,d], M. Scarpa[c,d]

[a] *INFN Torino, via P.Giuria 1, 10125 Torino, Italy*
[b] *Department of Physics, University of Torino, via P.Giuria 1, 10125 Torino, Italy*
[c] *INFN Ferrara, via Paradiso 12, 44100 Ferrara, Italy*
[d] *Department of Physics, University of Ferrara, via Paradiso 12, 44100 Ferrara, Italy*

Abstract

A new read-out for the drift chambers (DCH) (8192 channels) of the NA48 experiment at CERN has been developed and realized by the Ferrara and Torino INFN sites and has taken data during the 2002 run. The core of the system is a set of 32 VME-9U Time-to-Digital-Converter boards (NA48-TDC). The NA48-TDCs record the time of arrival of signals from the DCH and store them in 40 MHz pipelined ring memories pending the trigger supervisor's decision. Dual memories and data extraction resources allow independent and simultaneous processing of level-1 and level-2 trigger requests. Time measurements are performed by the TDC-F1 commercial ASICs, having an intrinsic time resolution of 120 ps and multi-hit capabilities. The NA48-TDC board features a maximum sustained rate of 500 kHz per channel.

Candidate TDC ASICs for the SUperB IFR Front End: experience with TDC-F1 by ACAM

Unfortunately TDC-F1 is being discontinued (the last order for TDC-F1 would have to be placed by Feb. 28 2008).

Possibile alternative candidates (preferred the ones with on-chip trigger matching):

- **CERN – HPTDC**
- **ATLAS – AMT-3**

Non trigger-matching TDC ASICs:

- **ACAM TDC-GPX**
- **..?..**

Using a (cheaper and simpler) non trigger-matching TDC ASIC will make the design of the TDC card much more complex due to the need of implementing circular buffers, based on (costly) dual-port RAM devices, in which timing measurements must be kept pending the Level_1 accept.

Dual ported RAM is needed to allow simultaneous storage of new hits and extraction of trigger-matched hits.

Accurate estimates of hit rates is needed to foresee the necessary depth and segmentation of Dual Ported RAM

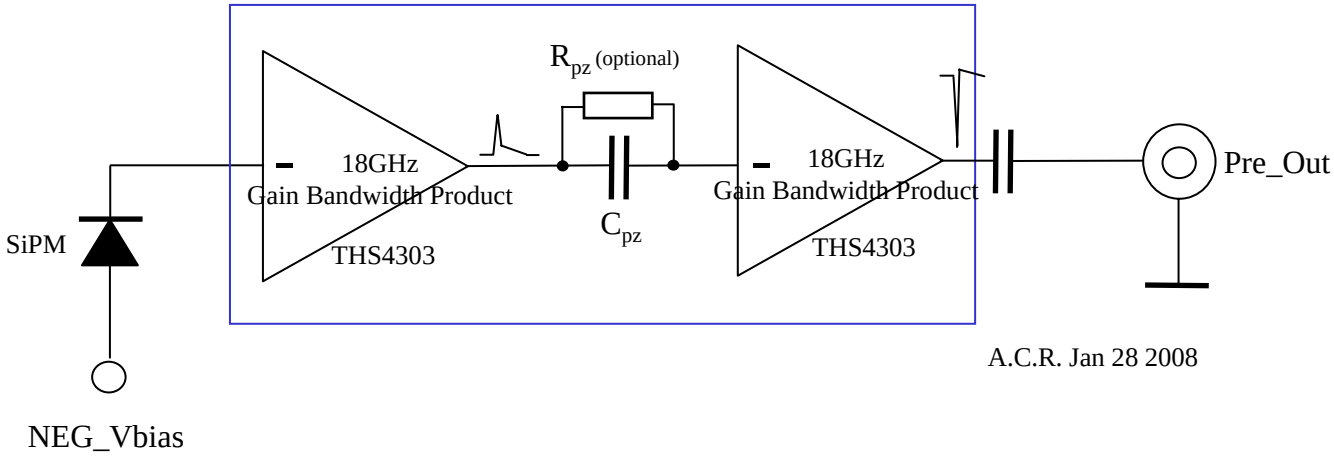
Candidate TDC ASICs for the SUperB IFR Front End

SiPM signal processing blocks

Unlike in the current LST-based barrel-IFR detector, SiPM signal processing (amplification and possibly discrimination) is VERY LIKELY needed as close as possible to the SiPMs and thus

inside the "iron".

The most straightforward SiPM signal processing block tested so far is a prototype amplifier based on the Texas Instruments' THS4303



A preamplifier for SiPM based on the Texas Instruments THS4303

Overview

A few designs based on operational amplifiers with a high gain-bandwidth product have been tested with SiPM from IRST and the details of the design which performed best, based on the Texas Instruments THS4303, are reported here, along with some preliminary test results.

Design guidelines were drawn after observing that:

• for the SiPM under test the anode was connected to the case, resulting in:

  • large stray capacitance

  • large amount of E.M.I. pick-up

  -> I thought it better to connect the SiPM cathode to the amplifier

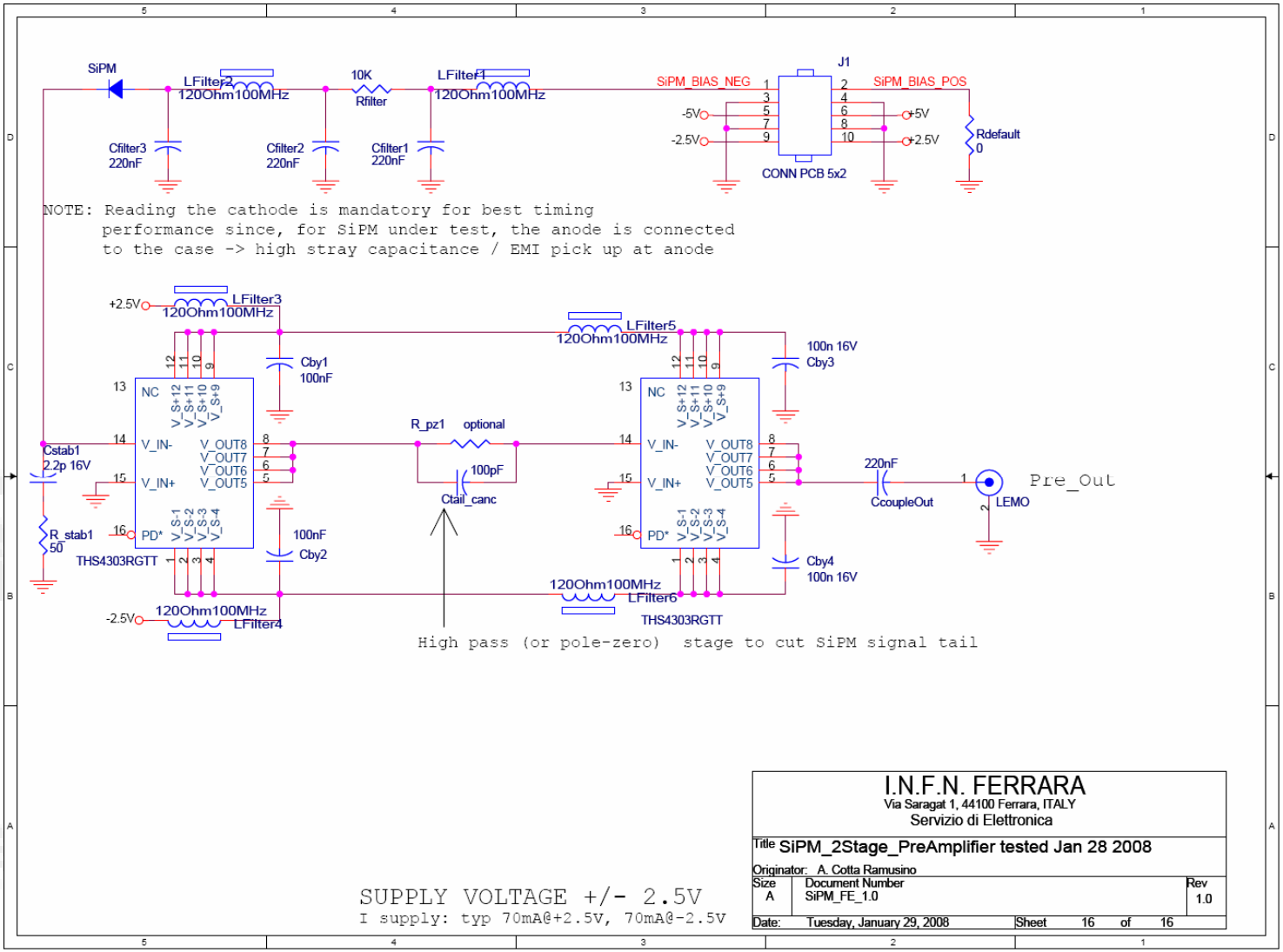
• the SiPM signal current shows a slow rise (“tail”) after the initial fast pulse. After pulses often appear on the “tail” of a previous pulse and this would, in my understanding, worsen the resolution of the pulse amplitude spectrum:

  -> I have used thus a high pass filter with a 5ns time constant to couple the second stage to the first. A pole-zero compensation resistor is also foreseen to improve the “tail cancellation”.

THS4303RGTT cost less than 3$ in the 1000 pieces range

A preamplifier for SiPM based on the Texas Instruments THS4303

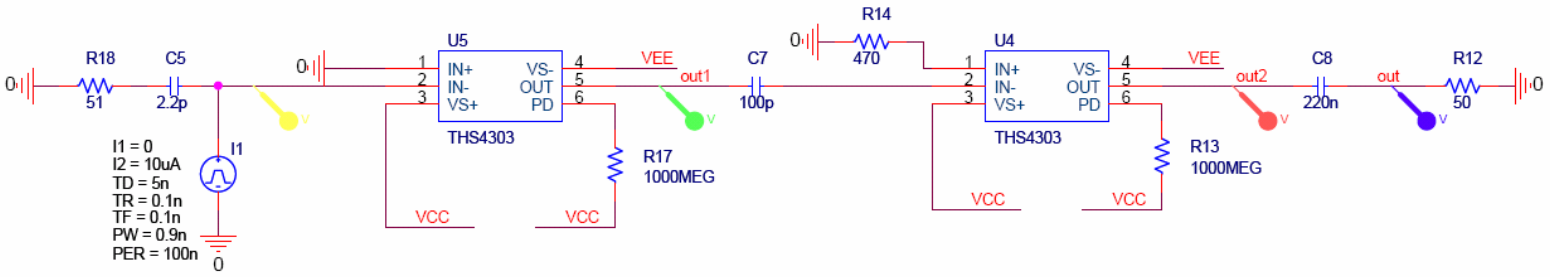
Schematic diagram of the prototype board



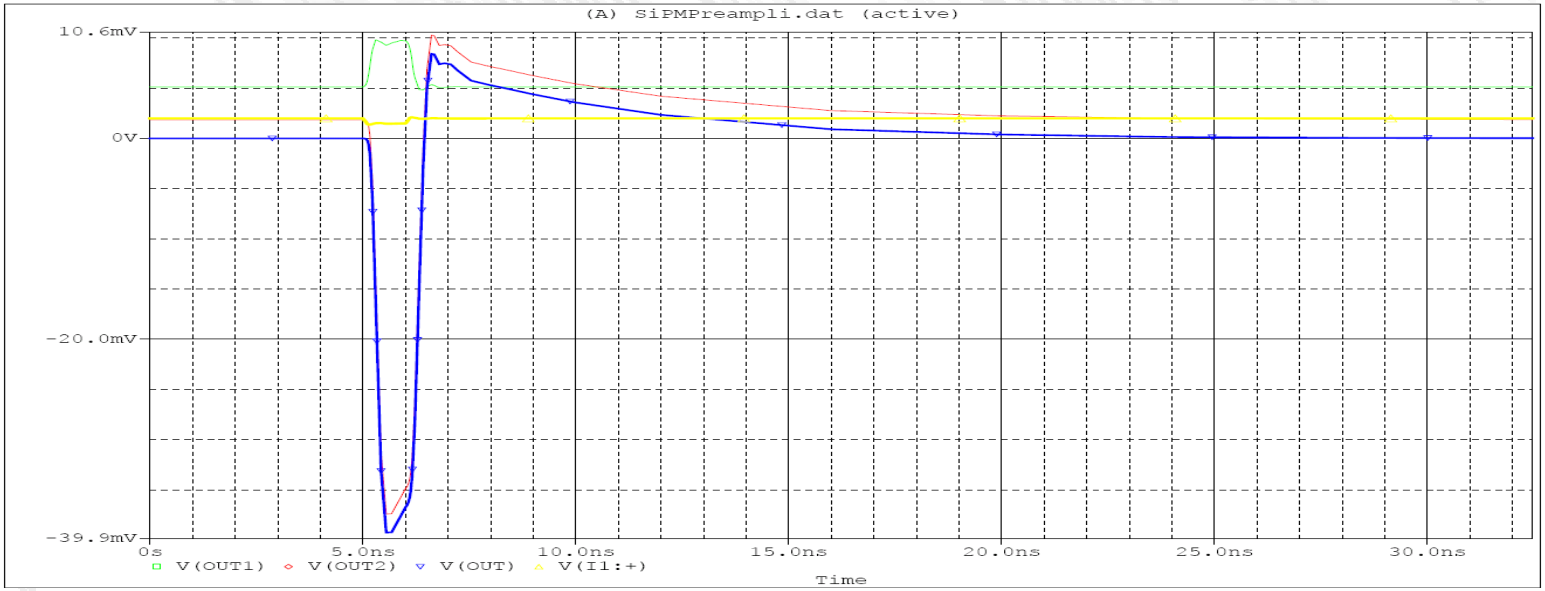
A preamplifier for SiPM based on the Texas Instruments THS4303

SPICE simulation: transient analysis of the THS4303 current amplifier

I / V converter stage **9 x Amplifier / cable driver**

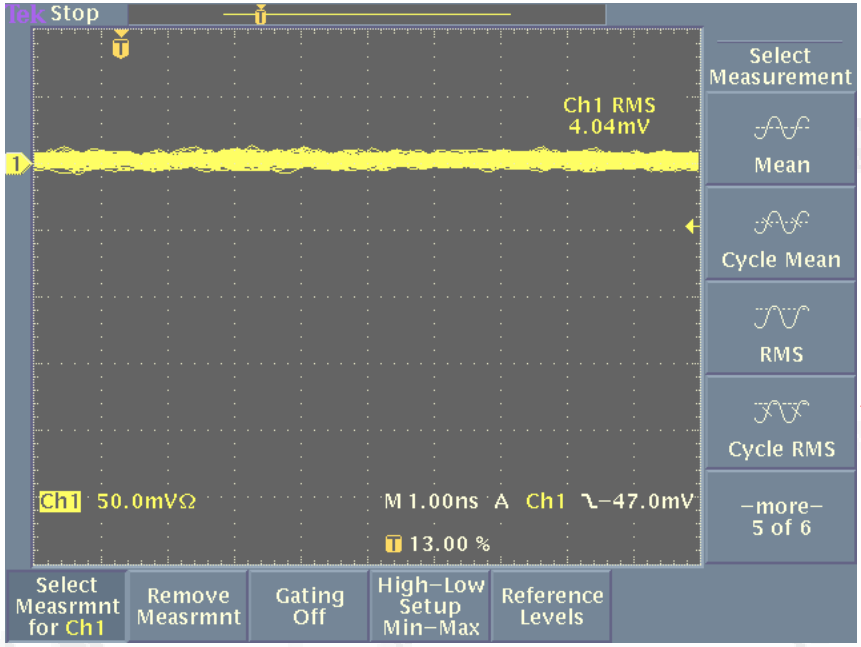


Used THS4303RGTT SPICE model from www.ti.com



Response to a 10fC charge

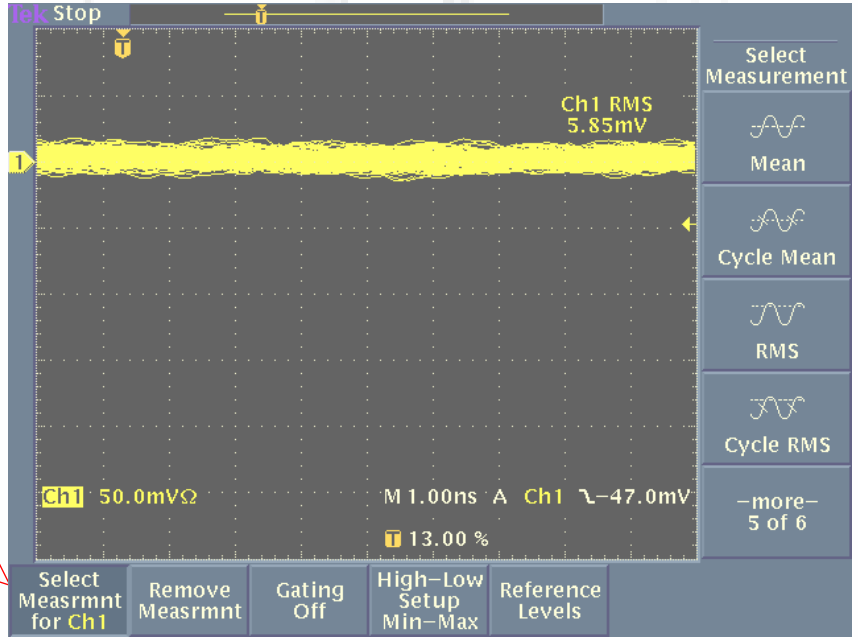
Preamplifier Noise floor



The noise floor at the preamp output with **NO** SiPM connected
Oscilloscope Tektronix TDS3054 (500MHz Bw)

CH1: 50Ohm terminated, 50mV/div

SiPM amplifier output with **NO** 50ohm series termination resistor



The noise floor at the preamp output with the SiPM connected and the SiPM bias turned OFF

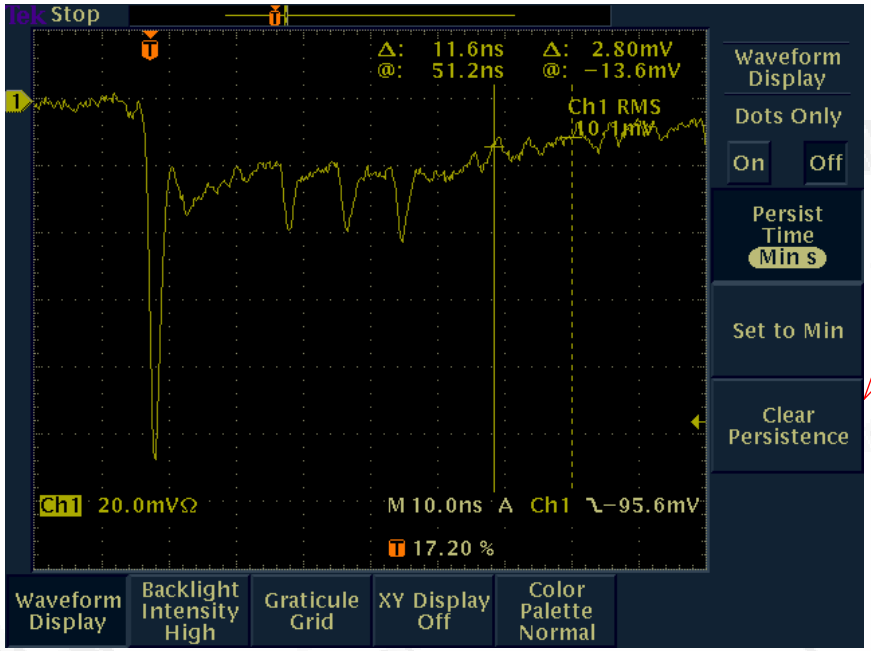
Oscilloscope Tektronix TDS3054 (500MHz Bw)

CH1: 50Ohm terminated, 50mV/div

SiPM amplifier output with **NO** 50ohm series termination resistor

A preamplifier for SiPM based on the Texas Instruments THS4303

SiPM signals

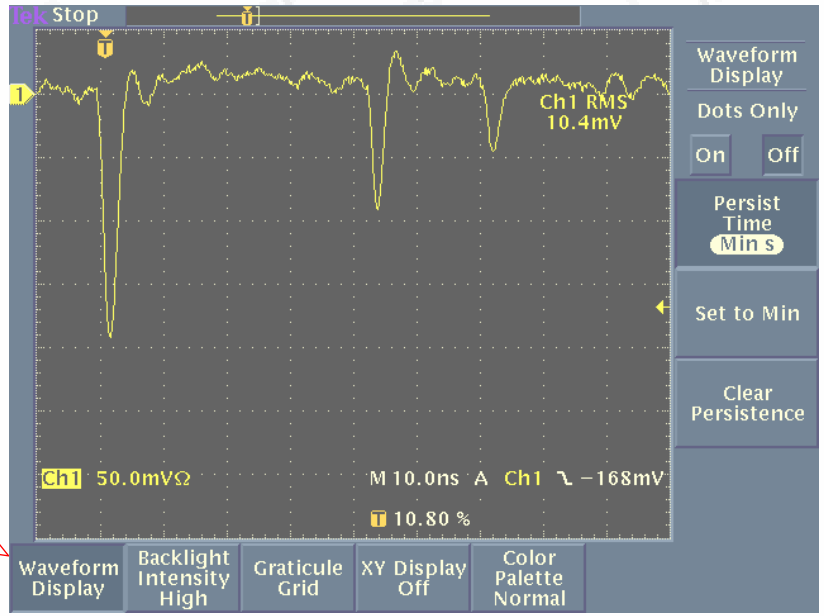


A SiPM signal waveform with SiPM@33V and **NO** "tail cancellation"

Oscilloscope Tektronix TDS3054 (500MHz Bw)

CH1: 50Ohm terminated, 20mV/div

SiPM amplifier output **WITH** 50ohm series termination resistor



A SiPM signal waveform with SiPM@35V and "tail cancellation"

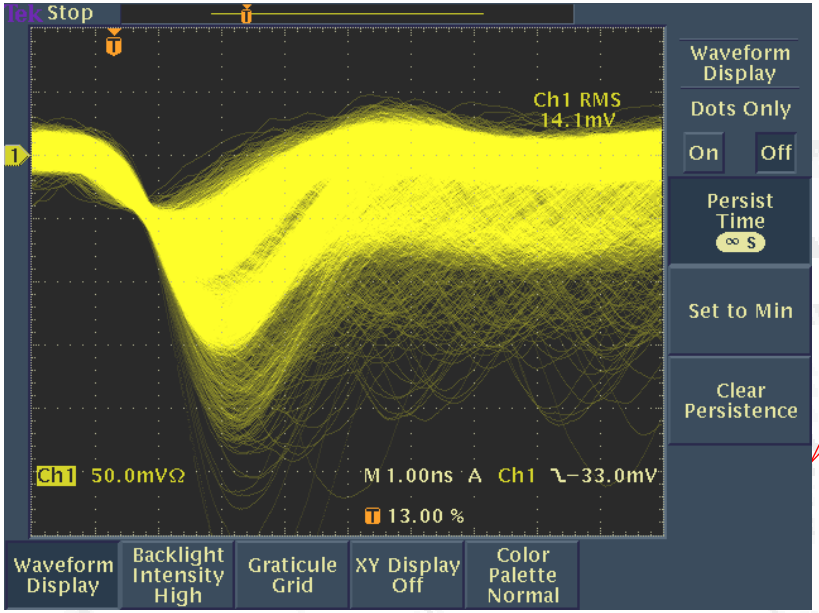
Oscilloscope Tektronix TDS3054 (500MHz Bw)

CH1: 50Ohm terminated, 50mV/div

SiPM amplifier output with **NO** 50ohm series termination resistor

A preamplifier for SiPM based on the Texas Instruments THS4303

SiPM pulse amplitude spectrum with different SiPM bias voltages



A SiPM signal waveform with **SiPM@ -37V**

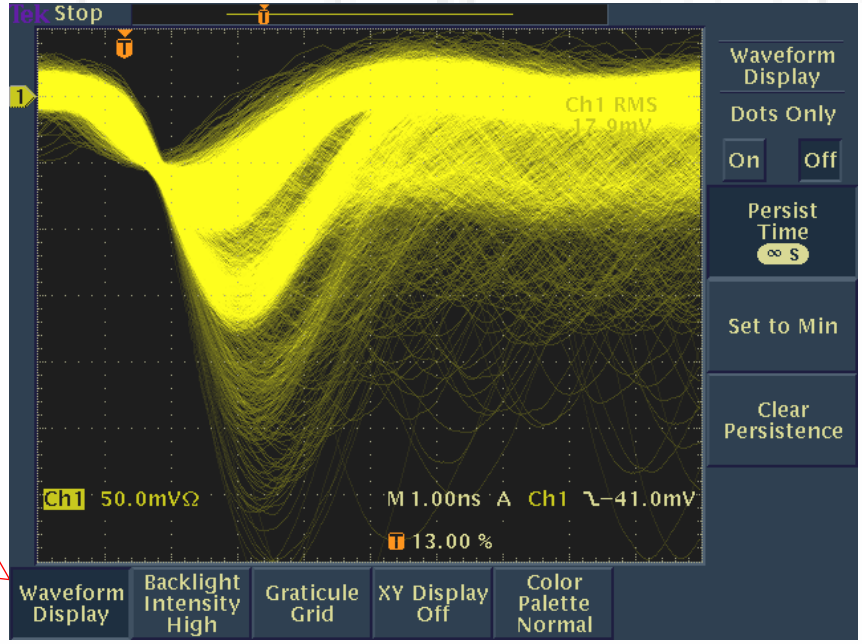
Oscilloscope Tektronix TDS3054 (500MHz Bw)
CH1: 50Ohm terminated, 50mV/div

SiPM amplifier output with **NO** 50ohm series termination resistor

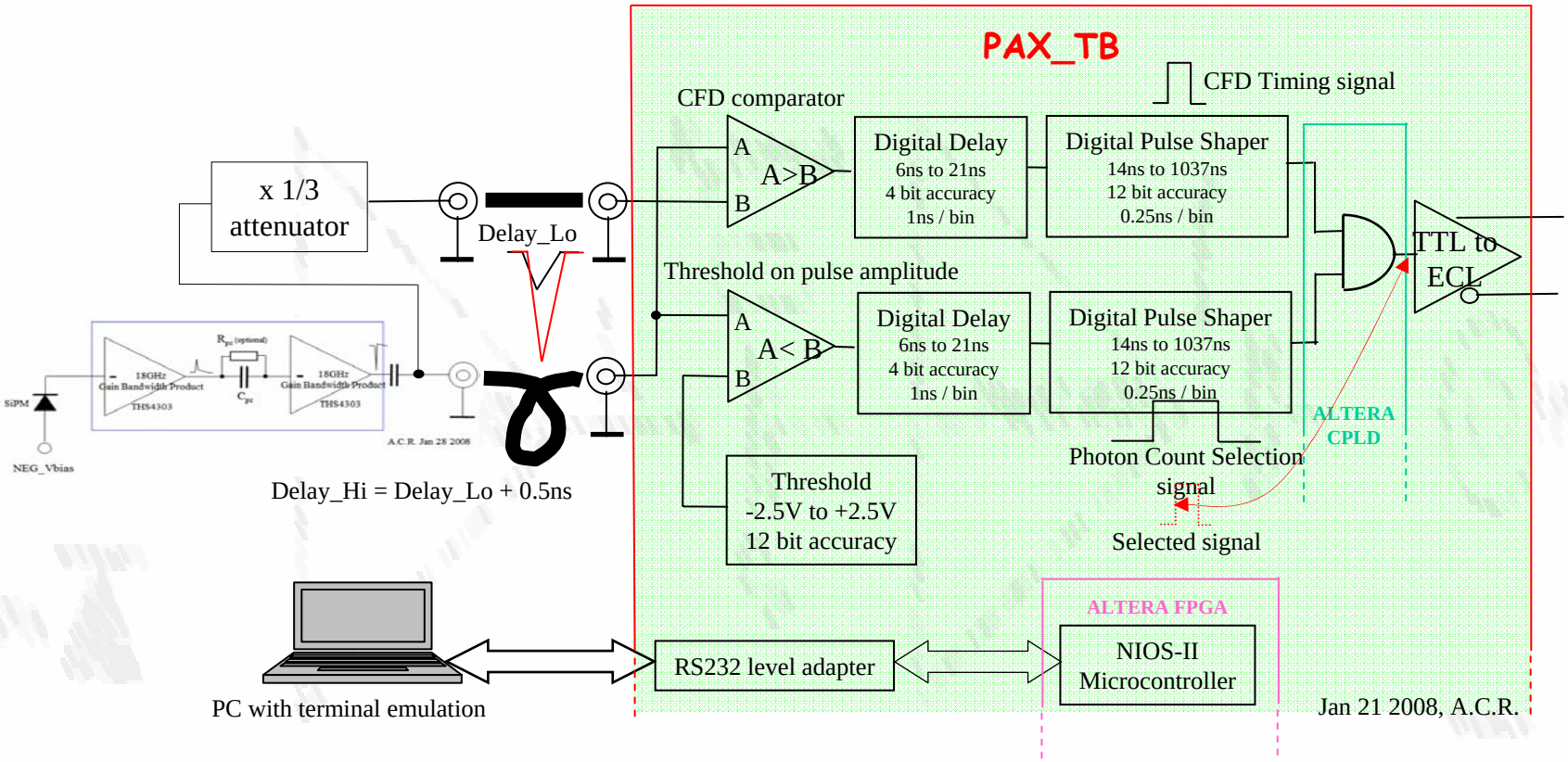
A SiPM signal waveform with **SiPM@ -38V**

Oscilloscope Tektronix TDS3054 (500MHz Bw)
CH1: 50Ohm terminated, 50mV/div

SiPM amplifier output with **NO** 50ohm series termination resistor



The next SiPM signal processing block about to be tested is a constant fraction discriminator



Block diagram of the SiPM signal processing chain proposed here to enhance, if necessary, the time resolution of the discrimination on the SiPM output.

A proposal for a SiPM Front End with constant fraction discriminator and "thermometer code" ADC: proof of principle implemented on the PAX Trigger Board (PAX_TB)

A proposal for a SiPM Front End with constant fraction discriminator and "thermometer code" ADC: proof of principle implemented on the PAX Trigger Board (PAX_TB)

The PAX_TB card has been recently developed at INFN-Ferrara as the programmable trigger unit for nuclear physics experiments preparing the future PAX experiment at GSI.

It is equipped with high speed (t_pd = 700ps) comparators (ADCMP562BRQ), programmable thresholds and programmable delays and pulse shaping. The PAX_TB card features 16 ECL outputs and 2 sets of NIM outputs. The function of these output can be redefined by re-programming the on-board CPLD and FPGA.

The output jitter with respect to the inputs is about 50ps.

In the current SiPM signal processing test setup the "PAX_TB" card comparators and resources will be used as shown in the previous slide for Constant Fraction Discrimination (CFD) and for gating the CFD output with the response of a pulse amplitude discriminator.

More on-board comparators (and delay elements, shapers and registers) could be used to implement a "thermometer code" ADC, with 4 levels for instance, to provide some coarse amplitude information on the pulse amplitude of a signal.

If the "thermometer code" information proves useful for off-line time-walk correction it might have to be included in the SuperB TDC Front End (and Dual Ported RAM circular buffers would then become mandatory to combine timing and coarse-amplitude information).