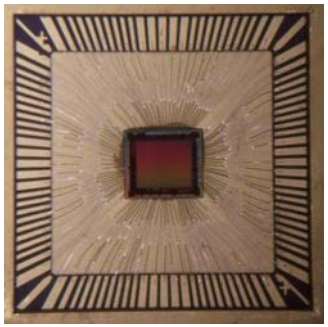
Compact, low-power readout: results from SLAC beam test, further improvements, and next development plans

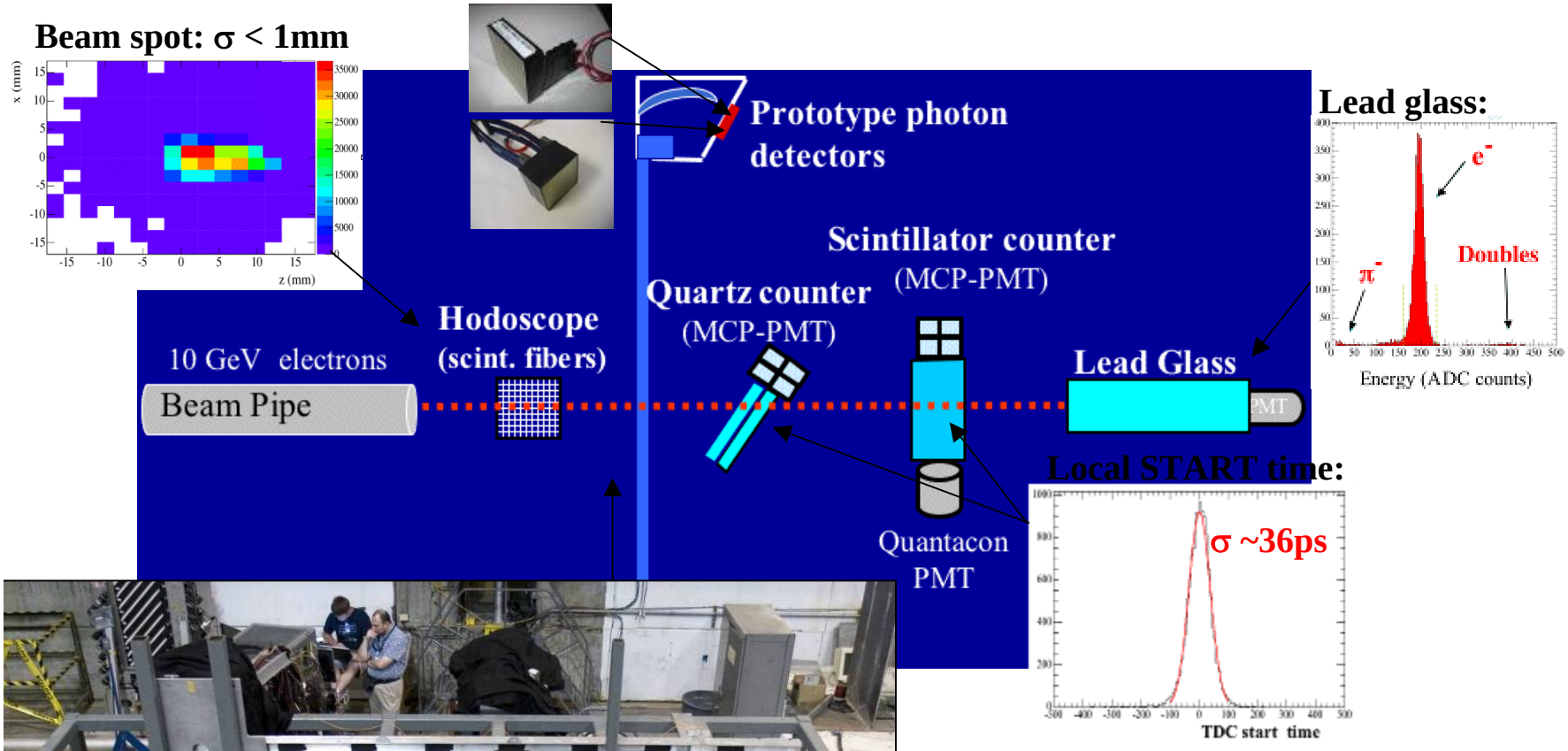
- T-492 results (what's new)
  - Waveform recording results
  - Compact test infrastructure
- Further prototype testing
  - Improved signal processing
  - Pipelined Processing
- BLAB2 ASIC and Large Scale test system

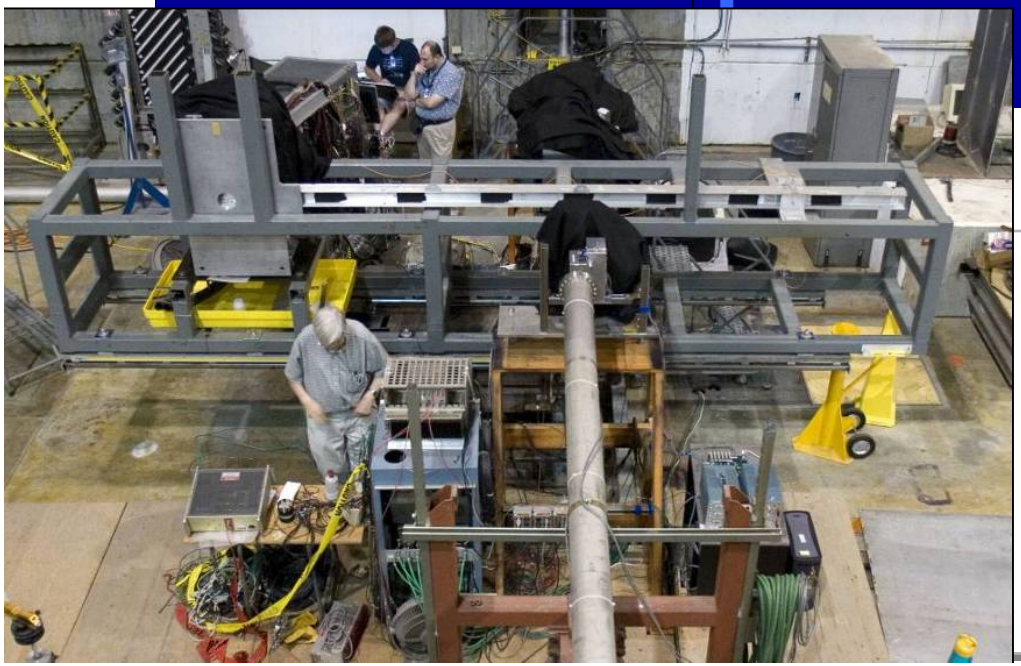
Larry Ruckman, Gary S. Varner (Univ. of Hawai'i)
Jochen Schwiening, Jerry Va'vra + EB others (SLAC)
Ke Wang (IHEP, Beijing)



Super-B PID Meeting 14-FEB-08

T-492 Focusing DIRC Test (Aug. 2007)





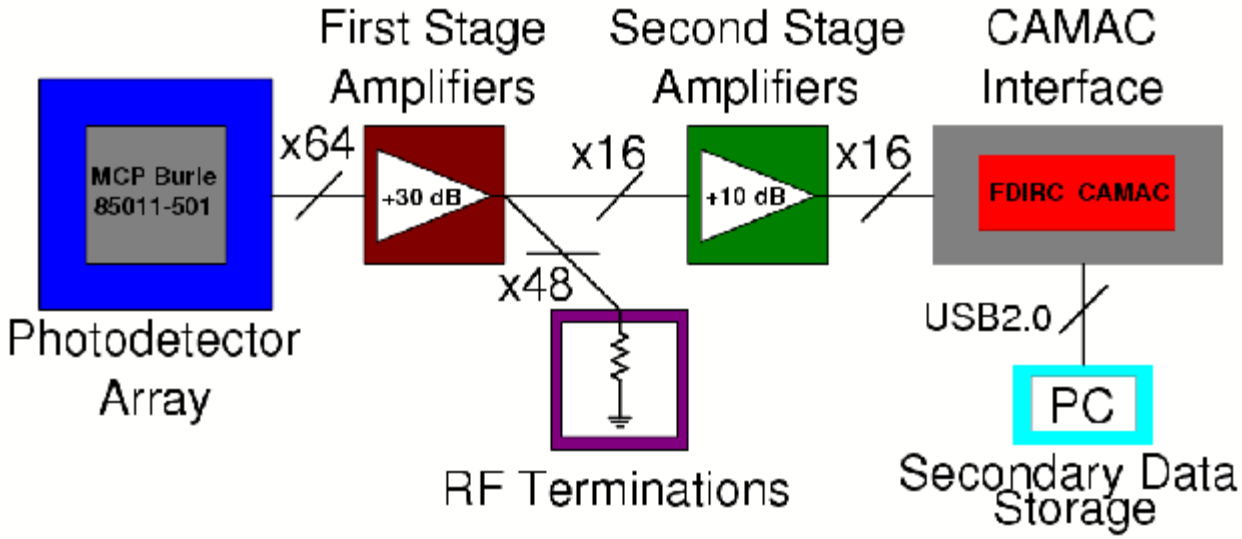
Focusing DIRC R&D effort at SLAC:

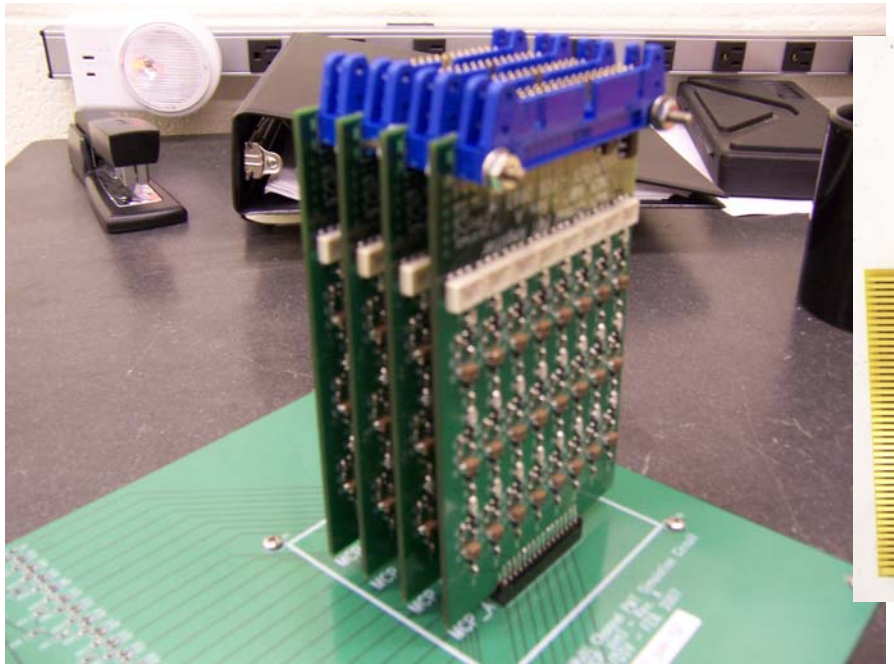
Jose Benitez [#] David W.G.S. Leith [#]
Gholam Mazaheri [#] Blair N. Ratcliff [#]
Larry L. Ruckman [+] Jochen Schwiening [#]
Gary S. Varner [+] Jerry Va'vra [#]

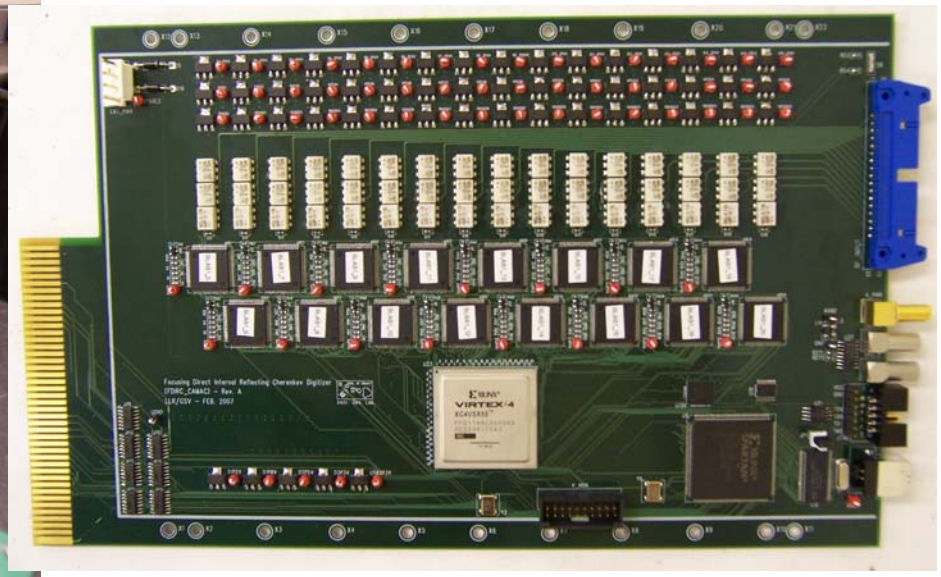
[#] SLAC [+] University of Hawaii

UH Prototype Readout Chain

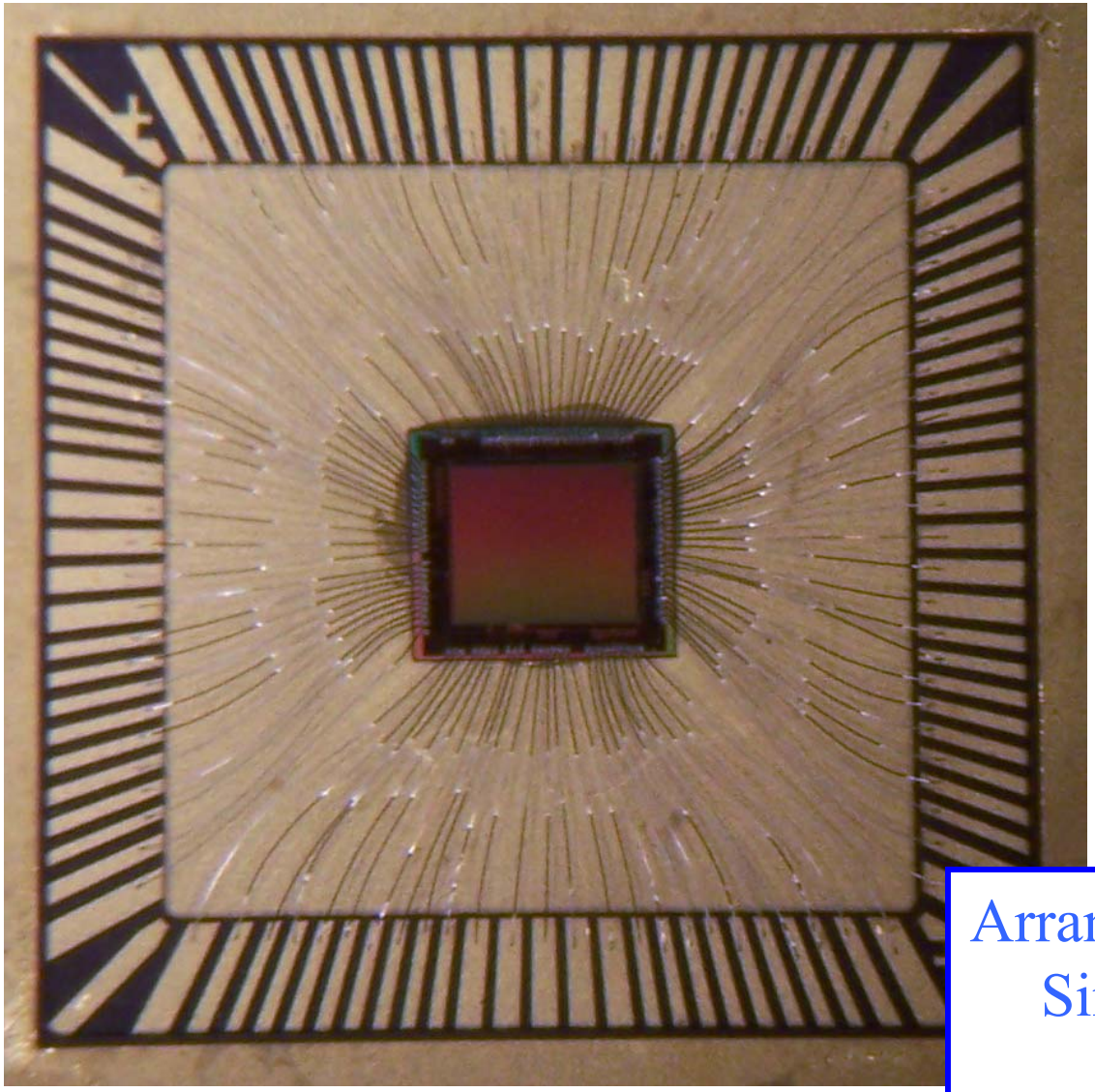
$G = 5x10^5$ single p.e. ~1mV







Buffered LABRADOR (BLAB1) ASIC



3mm x 2.8mm, TSMC 0.25um

- Single channel, actual storage ~few mm^2
- 64k samples deep, same SCA technique as LABRADOR (NIM A583: 447-460 [2007])
- Multi-MSa/s to Multi-GSa/s
- 12-64us to form Global trigger
- Details posted in paper to arXiv “today”

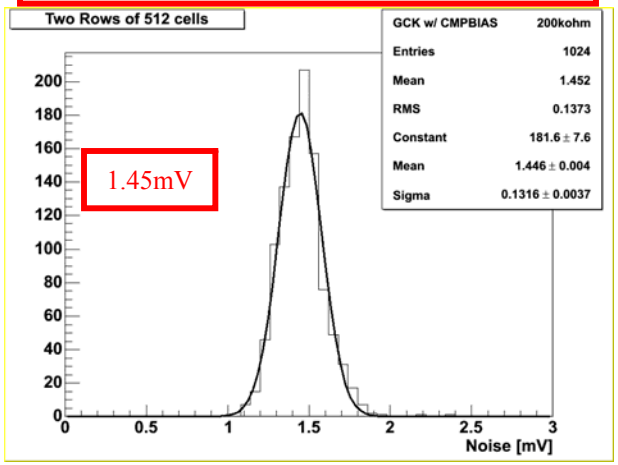
Arranged as 128 x 512 samples
Simultaneous Write/Read
➔ Pipelined

Buffered LABRADOR (BLAB1) ASIC

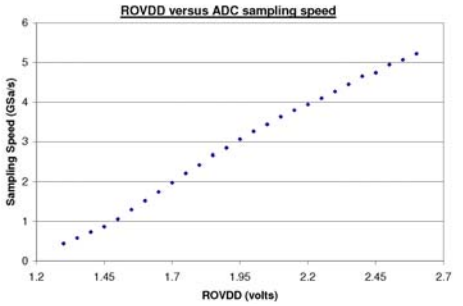
Key Features:

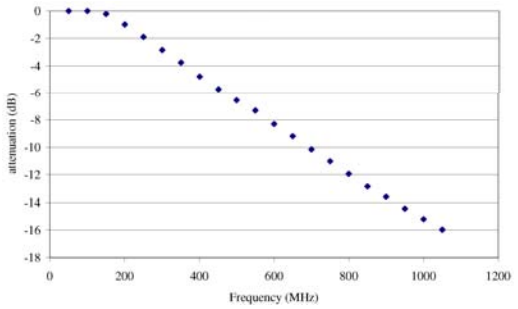
- Low noise, high dynamic range
  - Complete waveform sampling
  - >300MHz analog BW, ~6GSa/s
- Compact, low-power
  - Buffer for L1 trigger (<1mm^2/chan)
  - Few mW/channel (possibly less)
- Low-cost, flexible
  - < $10/chan in volume
  - Can adj. resolution vs. readout speed
- No high-power, noisy discriminator required, but still get excellent timing

1.6V dynamic range

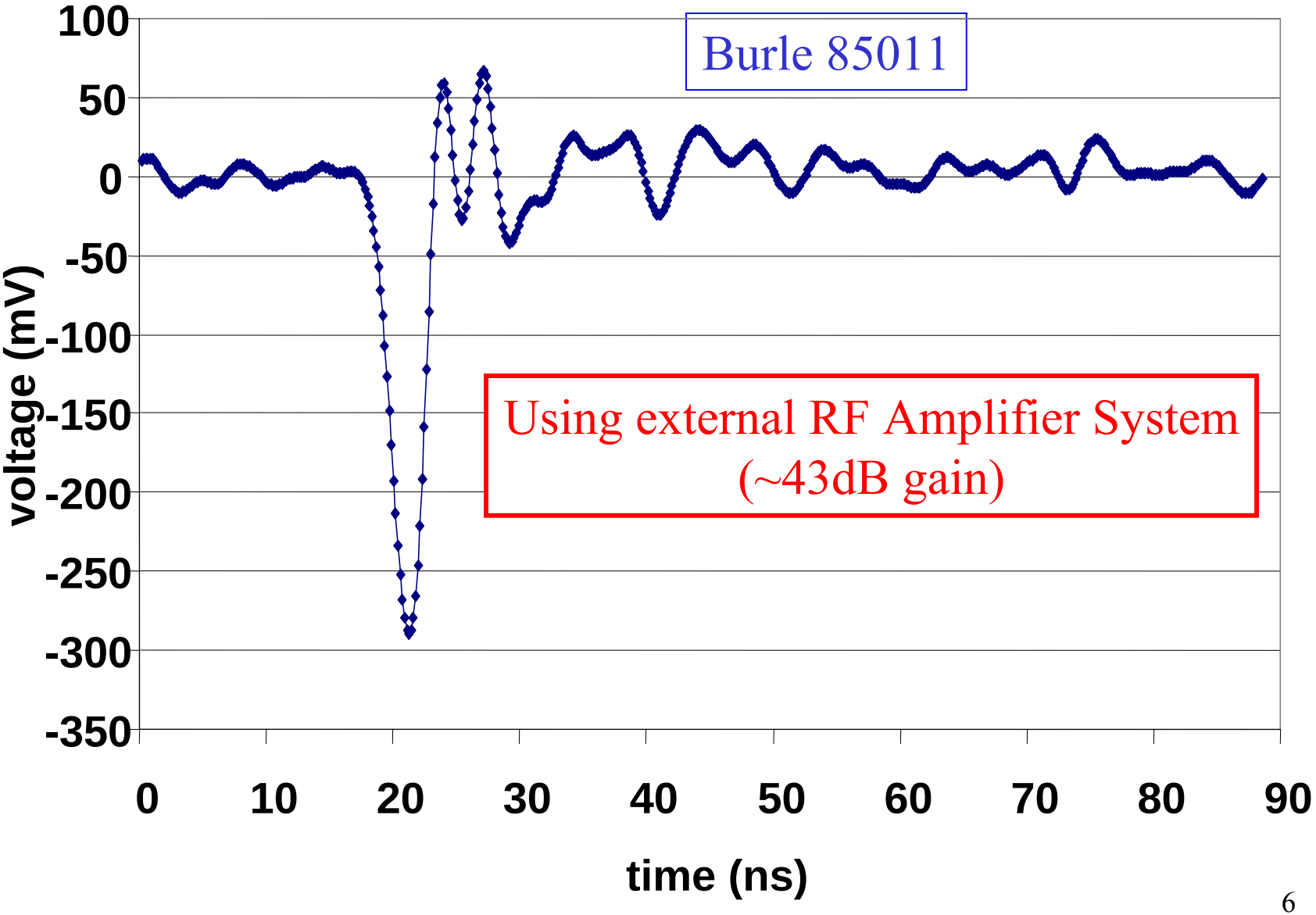


- 10 real bits of dynamic range, single-shot

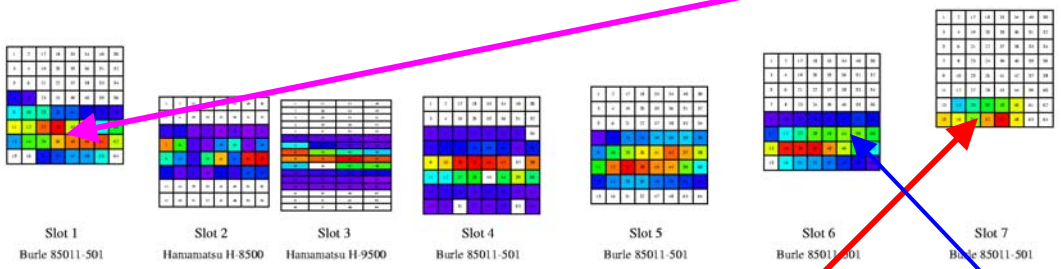




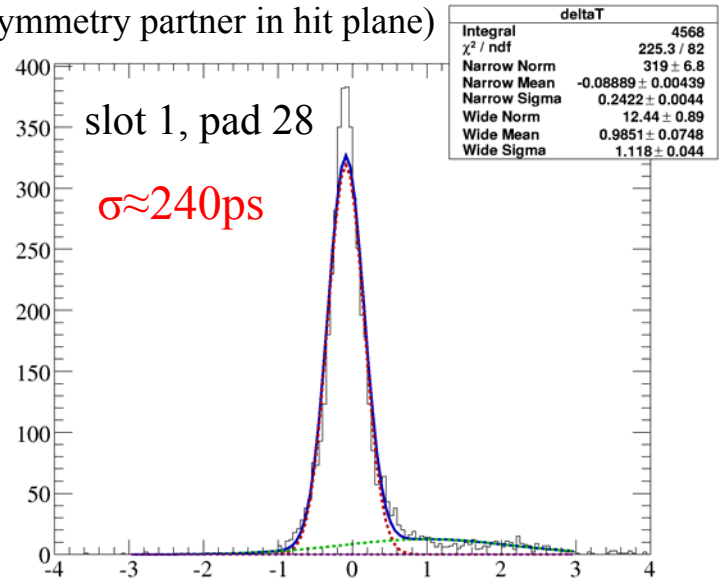
Single Photon Response

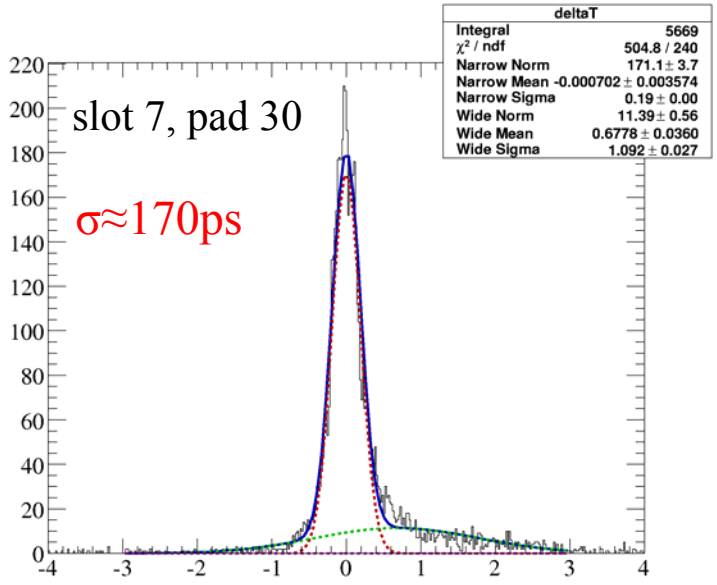


Comparison of UH timing slot 7, pad 15
to Philips slot 1&6
for run 27, pos 1, direct photons

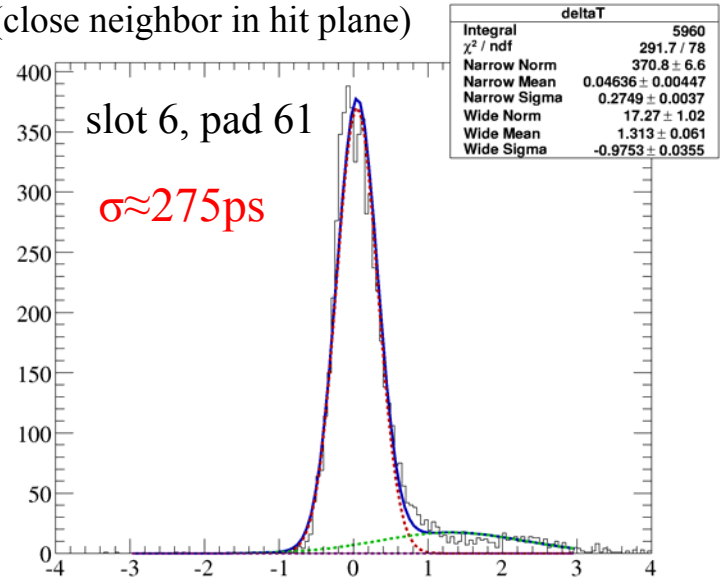


(symmetry partner in hit plane)





(close neighbor in hit plane)



Jochen Schwiening analysis (preliminary)

delta(time) (ns)

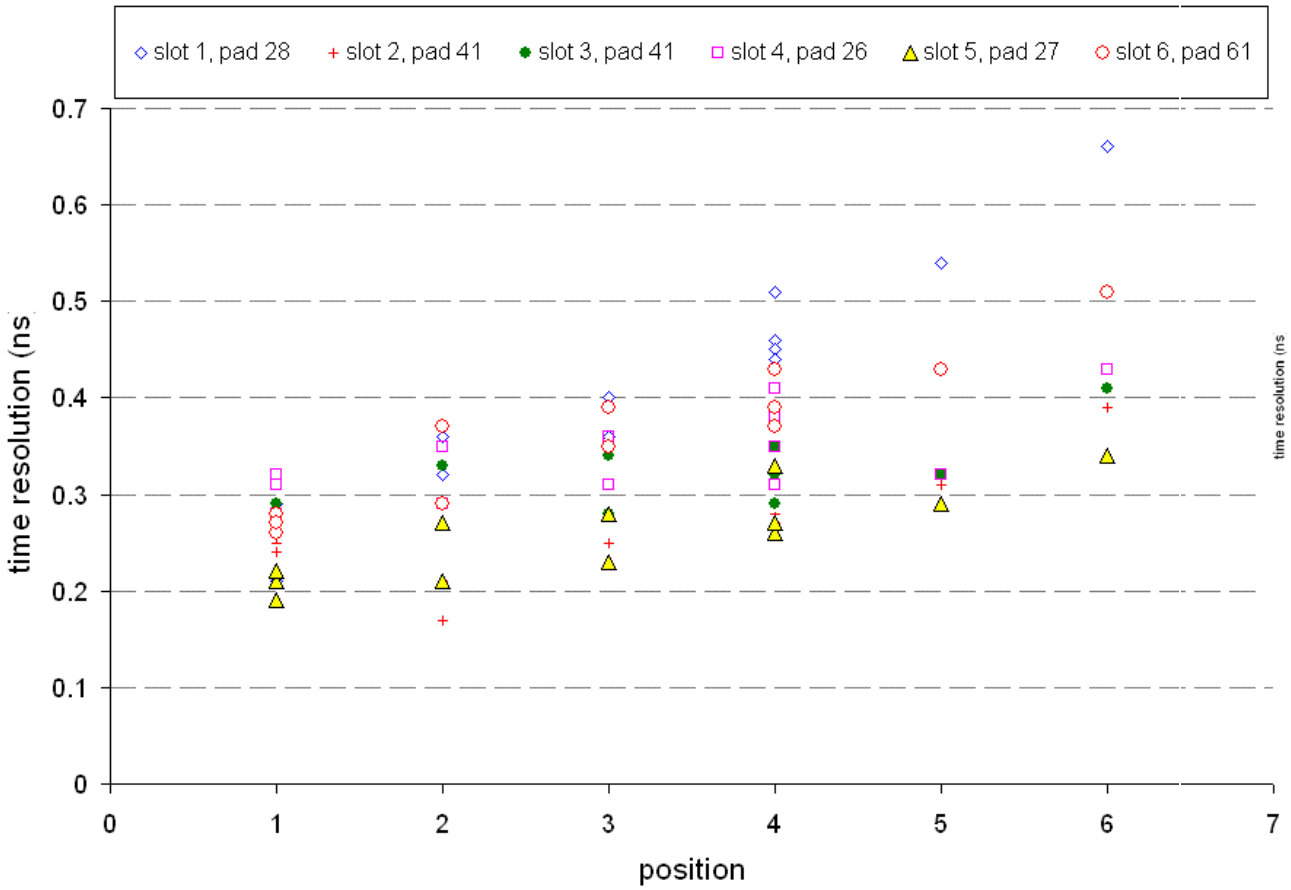
Super-B Fast PID Readout Update -- 14-FEB-08

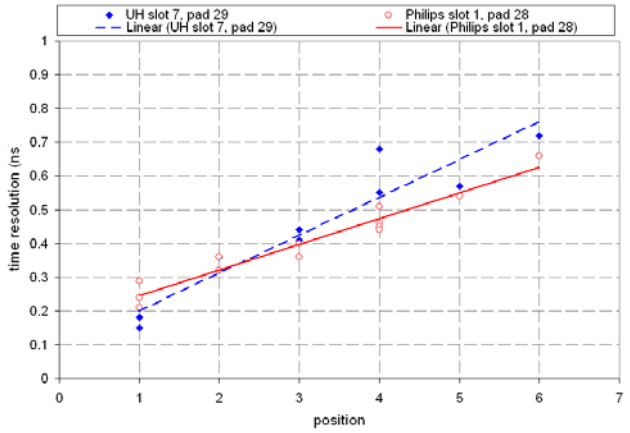
Don't currently have full G4 path prediction for slot 7

(would have to revive my code and run variable lambda analysis for 7 slots)

Compare slots as function of position number instead

selecting slot 1 pad which is expected to have very similar path length





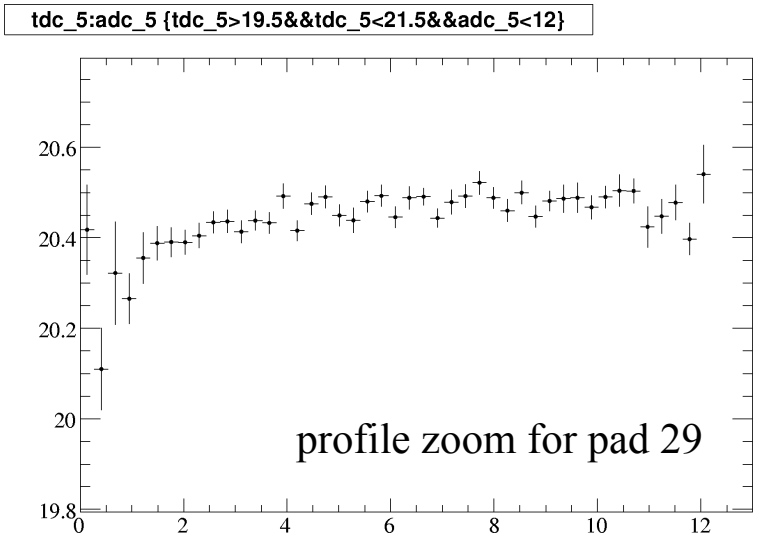
slopes get steeper as
you move toward wings

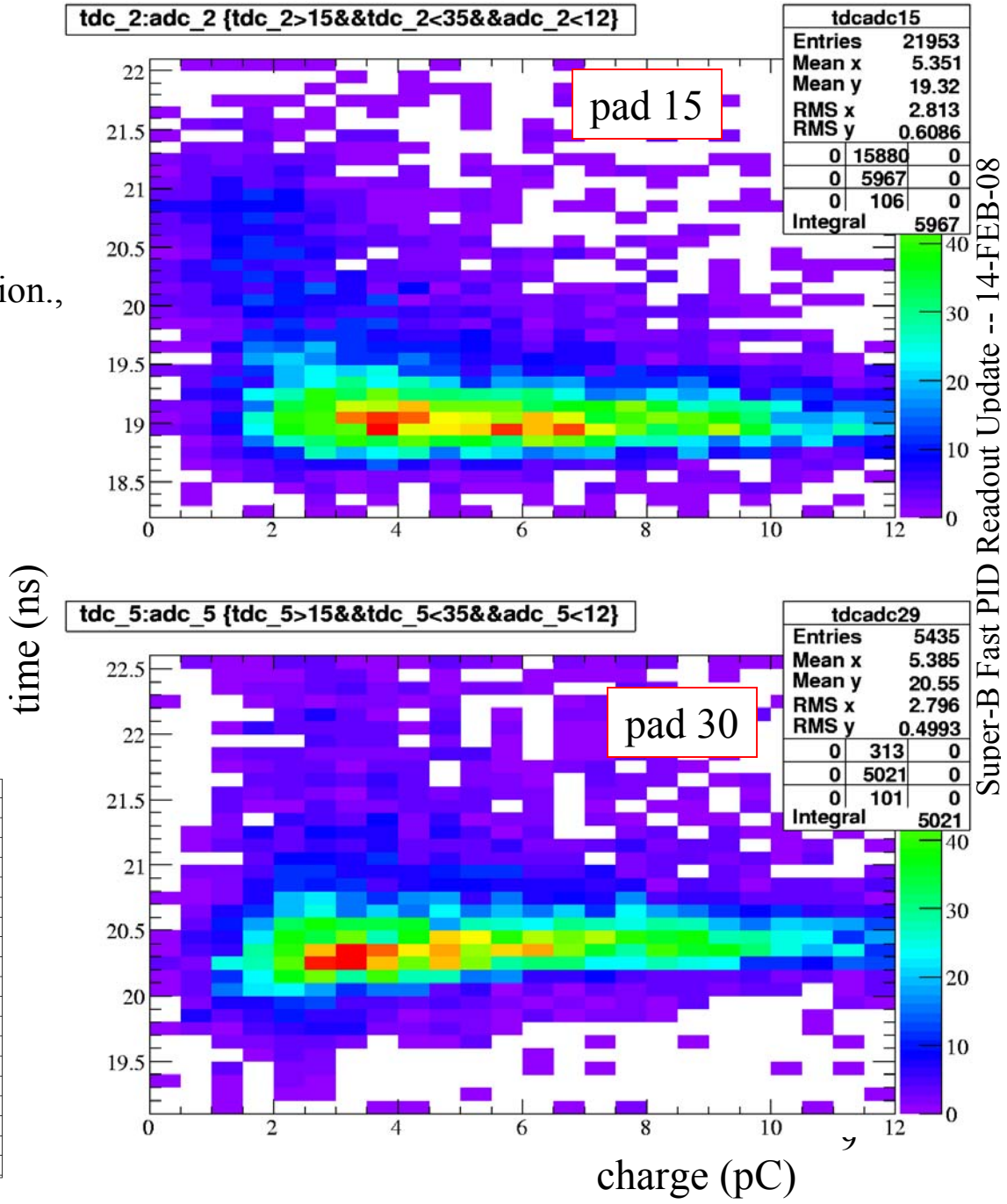
TDC vs. ADC for signal in run 27

Offline correction method seems to
come close to correcting time walk.

Some over-correction, some under-correction.,
more can be done offline with charge info.

Jochen Schwiening
analysis (preliminary)



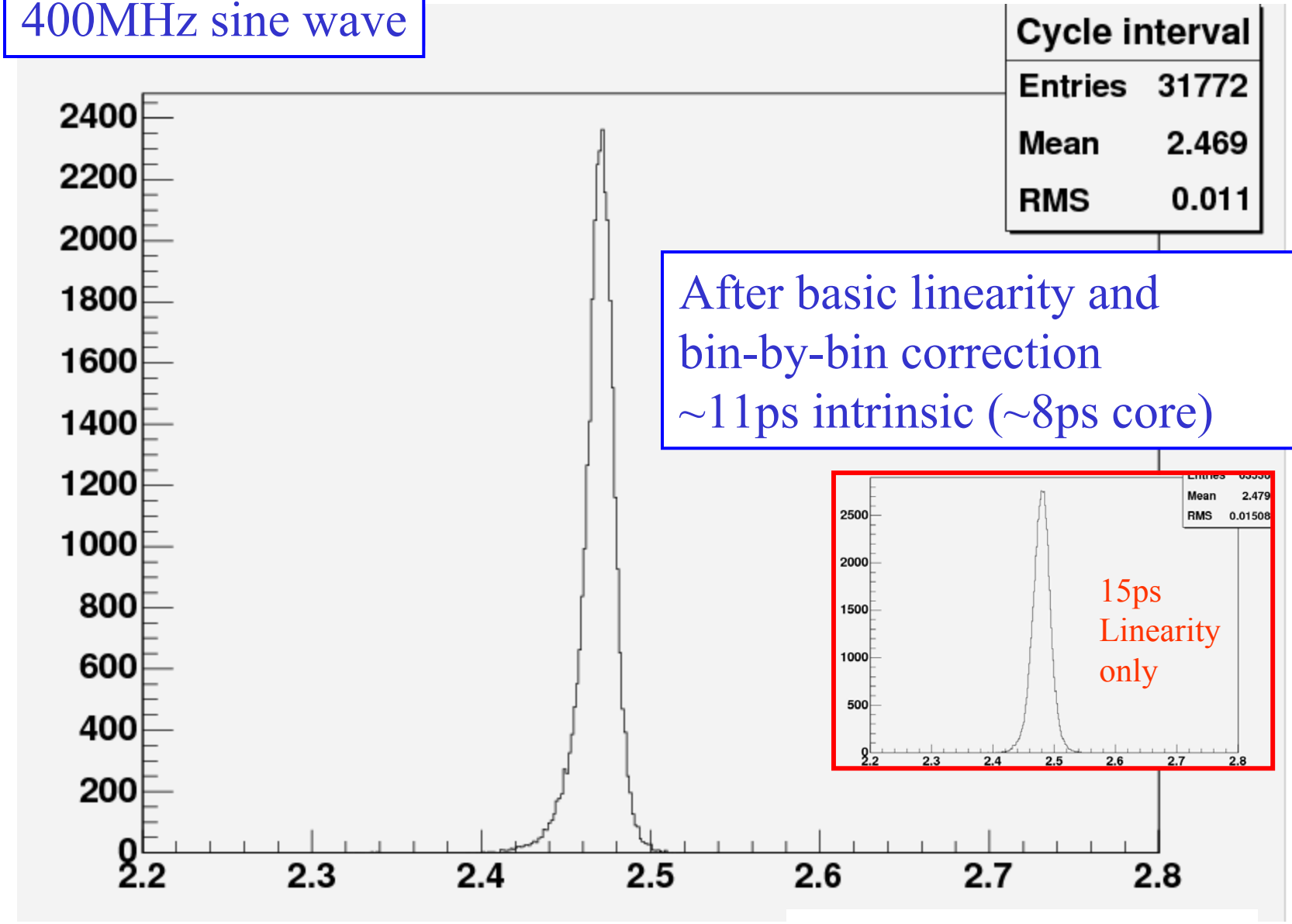


Super-B Fast PID Readout Update -- 14-FEB-08

Previously, after initial calibration

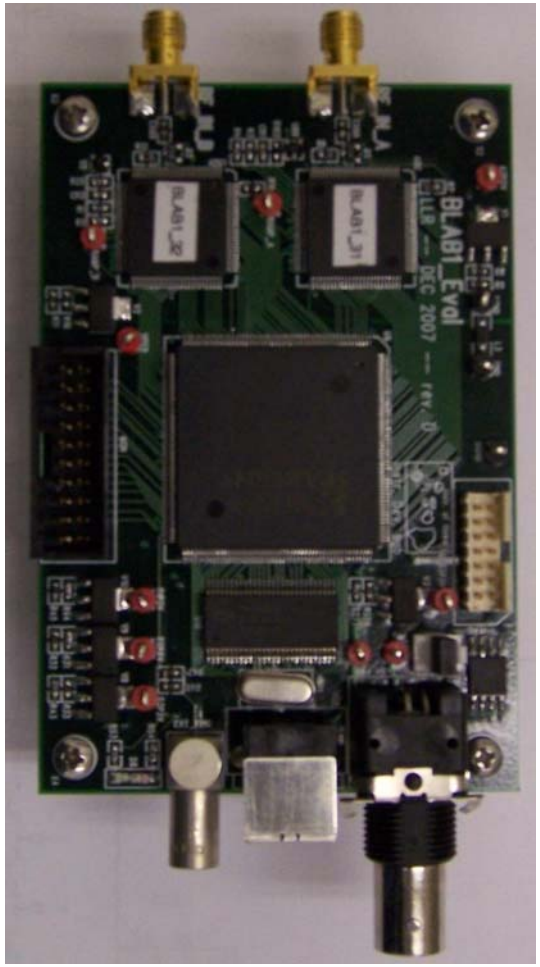
6GSa/s

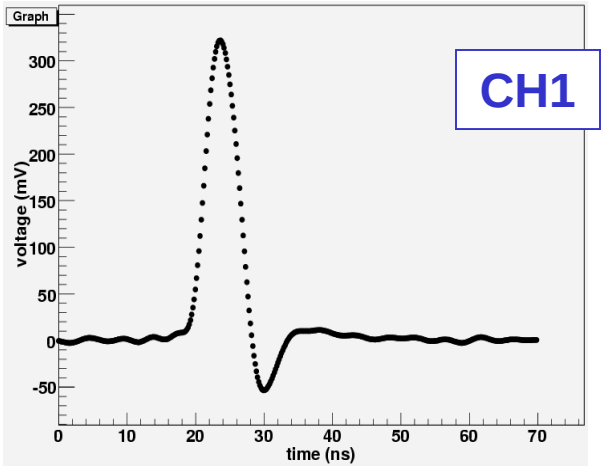
400MHz sine wave

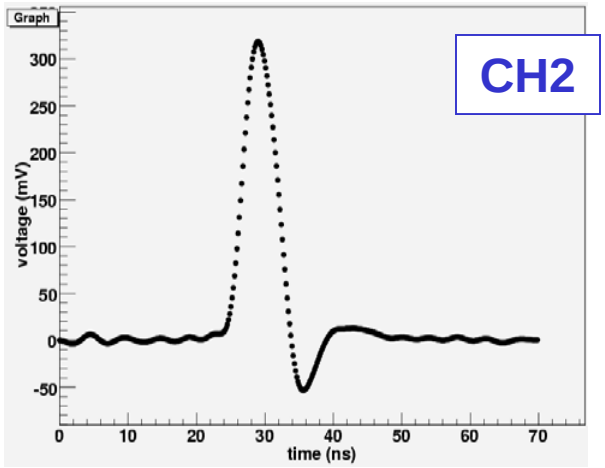


Agilent Pulse Measurement

- Two separate BLAB1 ASIC with a common sampling strobe
- RF split the Agilent pulse with additional cable delay in the 2nd channel

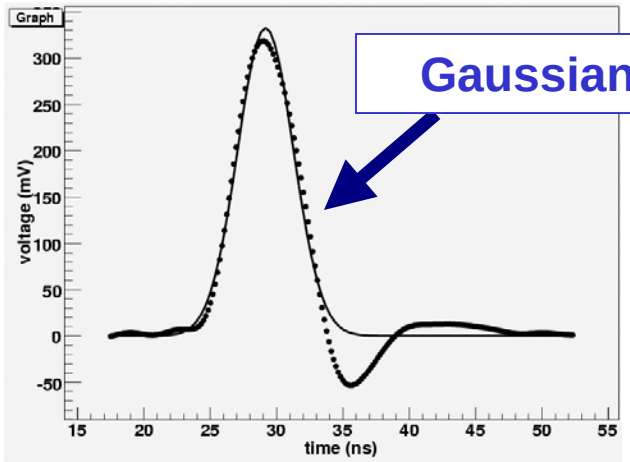


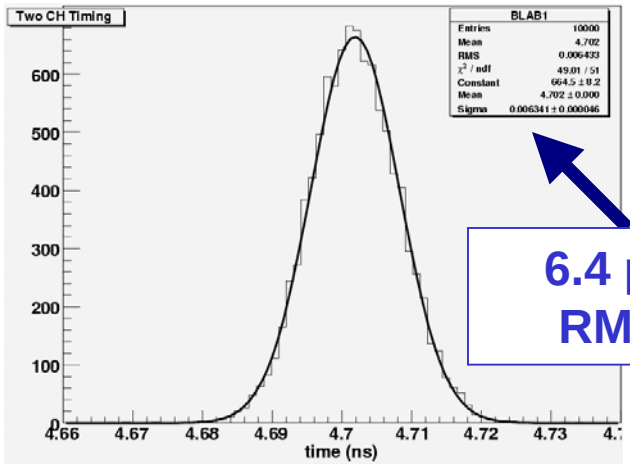




Agilent Pulse Fitting

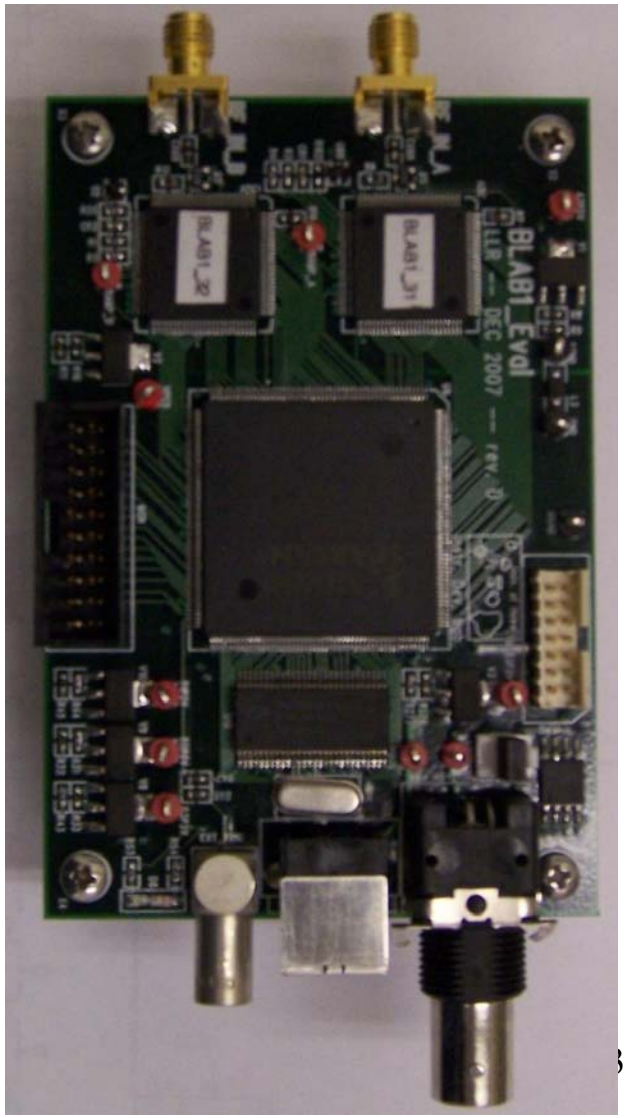
- Apply Gaussian fit to both functions
- Measure the time difference between the two fit means
  => single hit actually a factor sqrt(2) better (~4.5ps)
- Precise timing resolution for a fixed amplitude over a small timing window





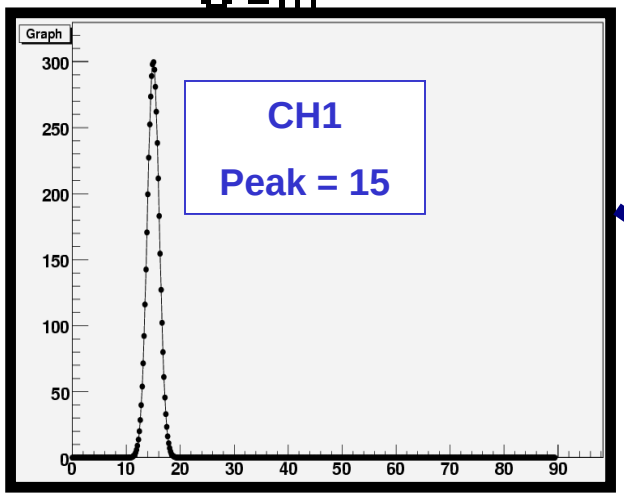
Pulse Fitting Disadvantages

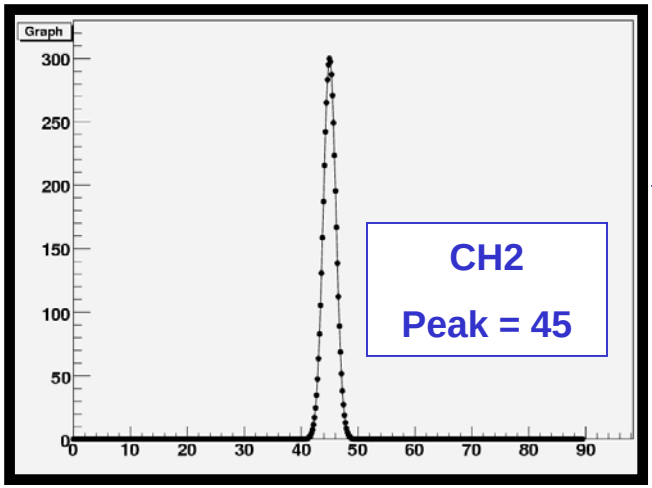
- Spend a lot of time developing an amplitude varying fit function
- Requires intense software effort
- Sluggish online processing duty cycle
- Offline processing requires very large data storage
- Offline processing requires a lot of CPU time

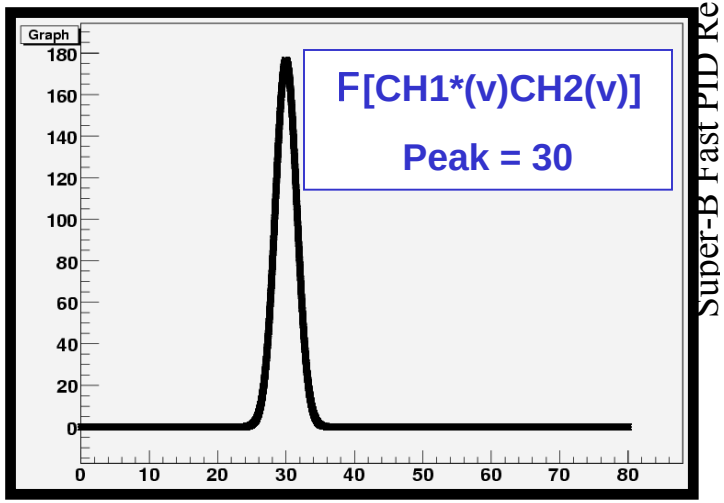


Cross-Correlation Theorem

$$f \star g = \int_{-\infty}^{\infty} \overline{f}(\tau)\, g(t+\tau)\, d\tau = \mathcal{F}\left[\overline{F}(\nu)\, G(\nu)\right],$$

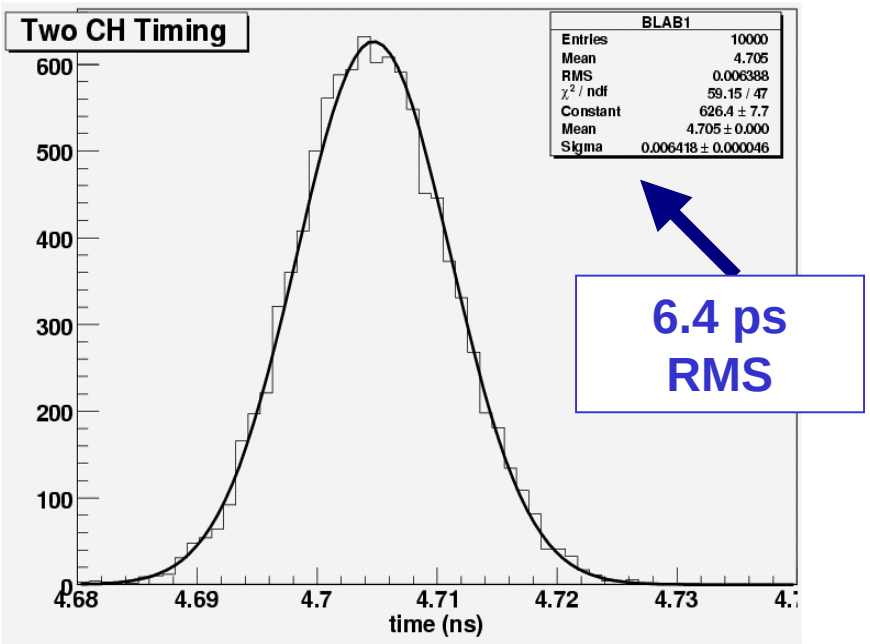






Agilent Pulse Cross-Correlation Method

- Also, excellent timing resolution
- Same timing jitter as the fitting method
- Perhaps hitting a timing resolution limit from time base drift
- Using full samples significantly reduces the impact of noise



Can pipeline process signals to extract T and Q, substantially reducing required data storage

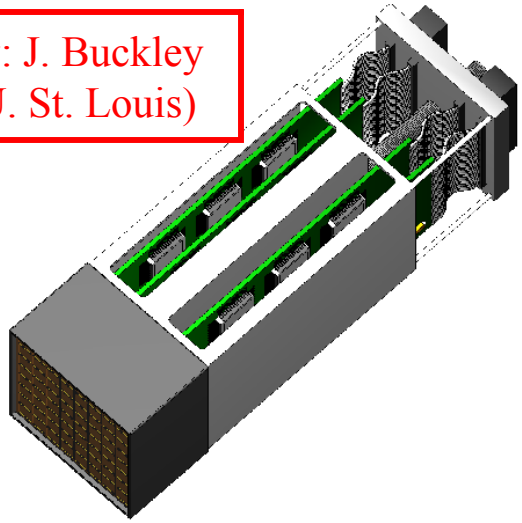
BLAB2

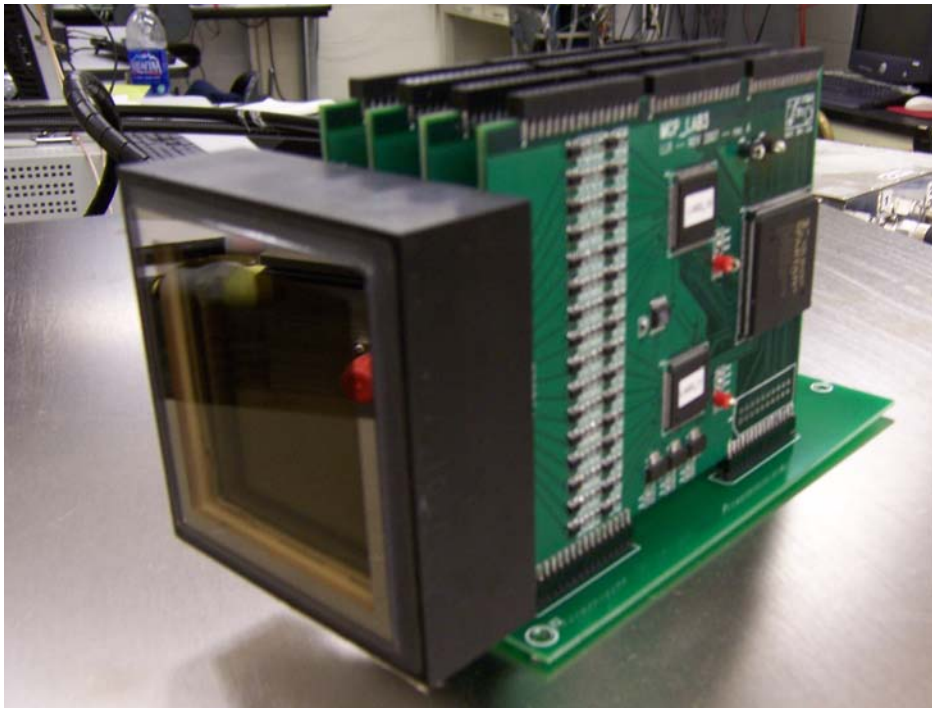
- **Initial Target: New f-DIRC/f-TOP Readout System**

TABLE II: *BLAB2 ASIC Specifications.*

Item	*Value*
Photodetector Input Channels	16
Linear sampling arrays/channel	2
Storage cells/linear array	512
Sampling speed (Giga-samples/s)	2.0 - 10.0
Outputs (Wilkinson)	32

Courtesy: J. Buckley
(Wash U. St. Louis)

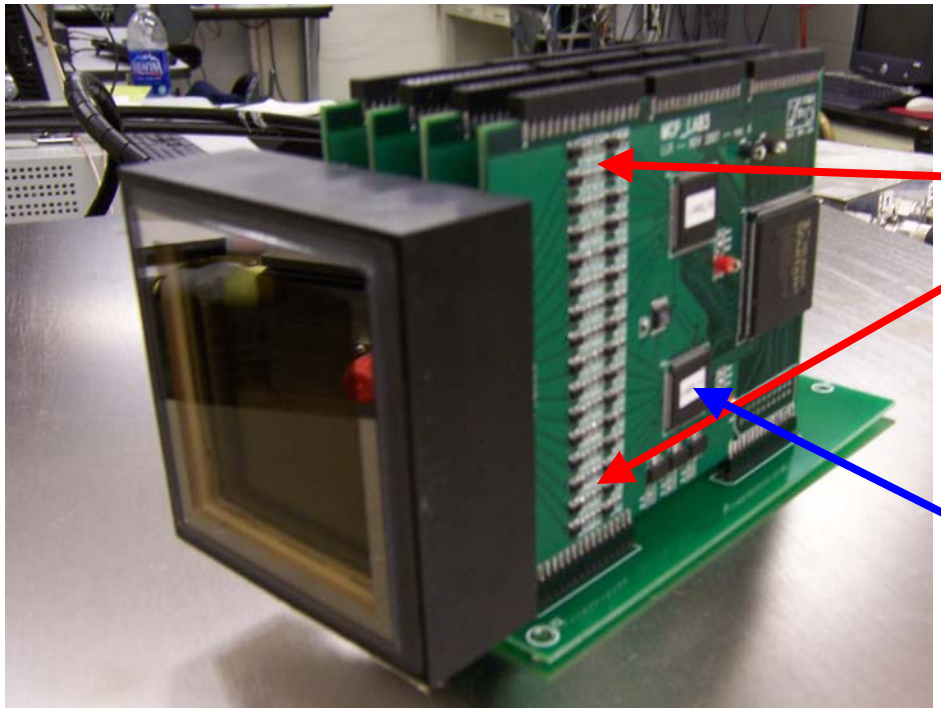




Gen. 0 Prototype (LAB3)

Target Submission: Apr. 4

Gain Needed



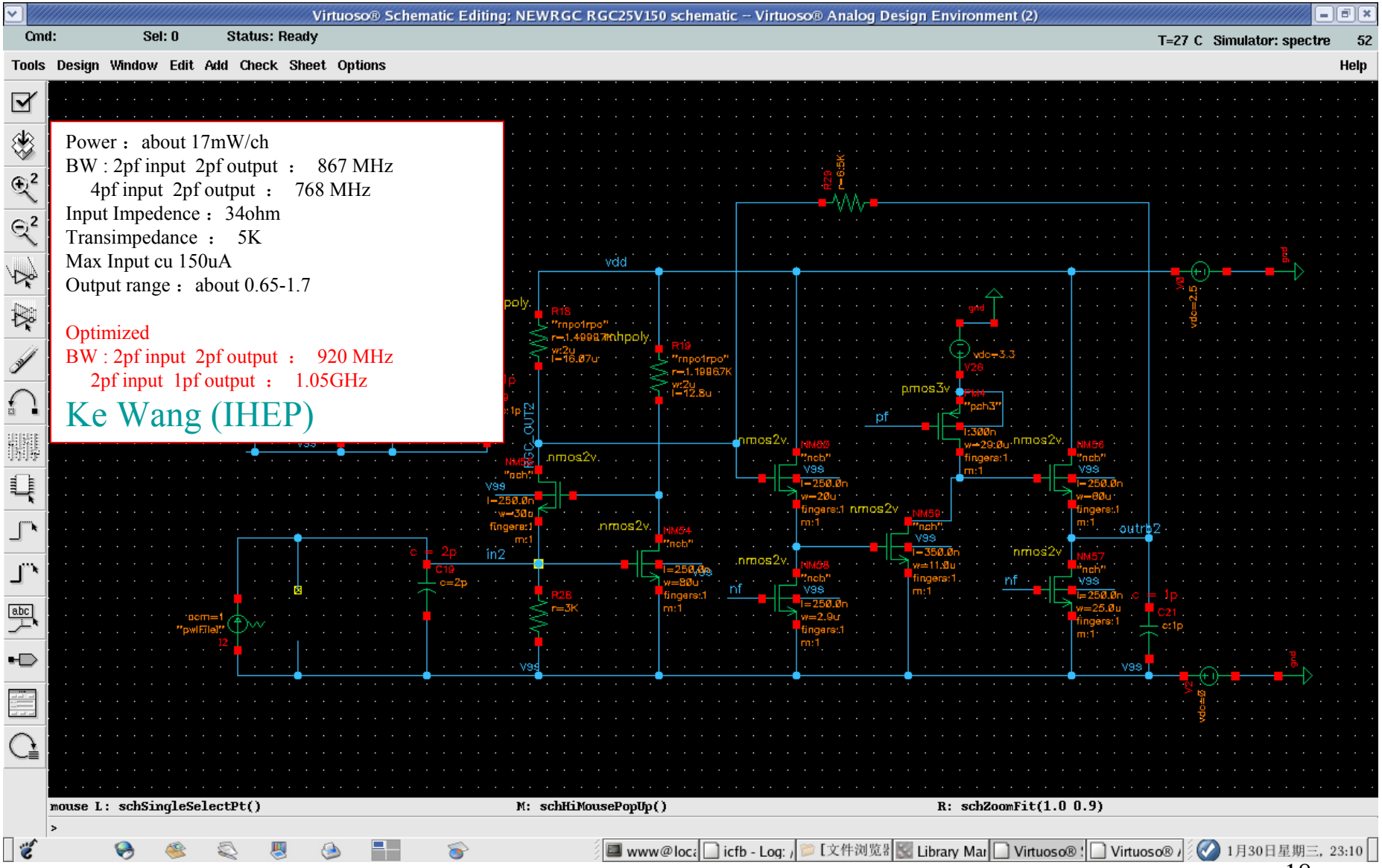
Amplifiers dominate board space

Readout ASIC tiny (14x14mm for 16 channels)

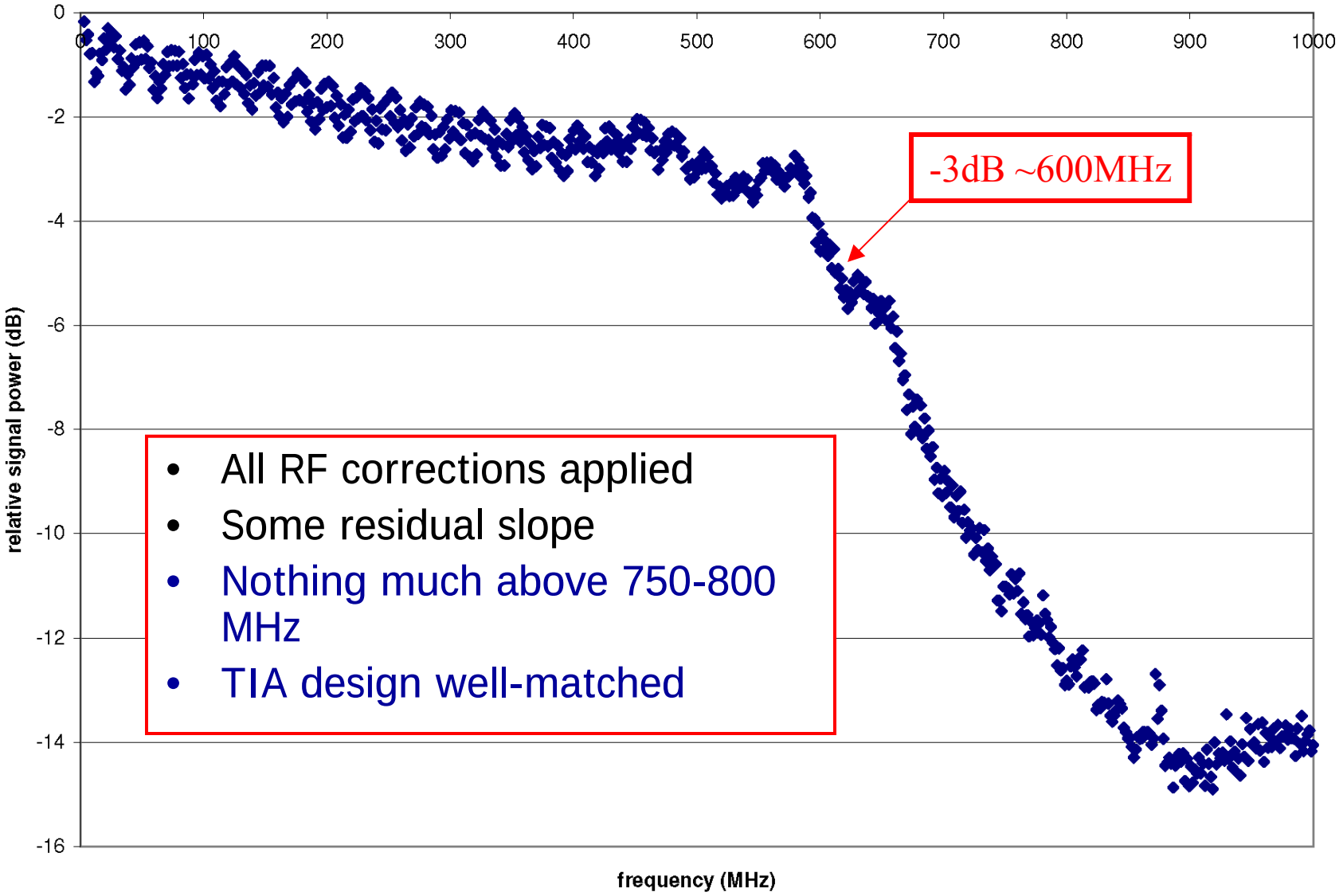
- What gain needed?
  - At 10^6 gain, each p.e. = 160 fC
  - At $2x10^5$ gain (better for aging), each p.e. = 32 fC
  - In typical ~5ns pulse, Vpeak = dQ/dt * R = 32uA * R = 32mV * R [kΩ] (6.4mV)

Gain Estimate	
Rterm	1 p.e. peak
50	1mV
1k	20mV
20k	400mV

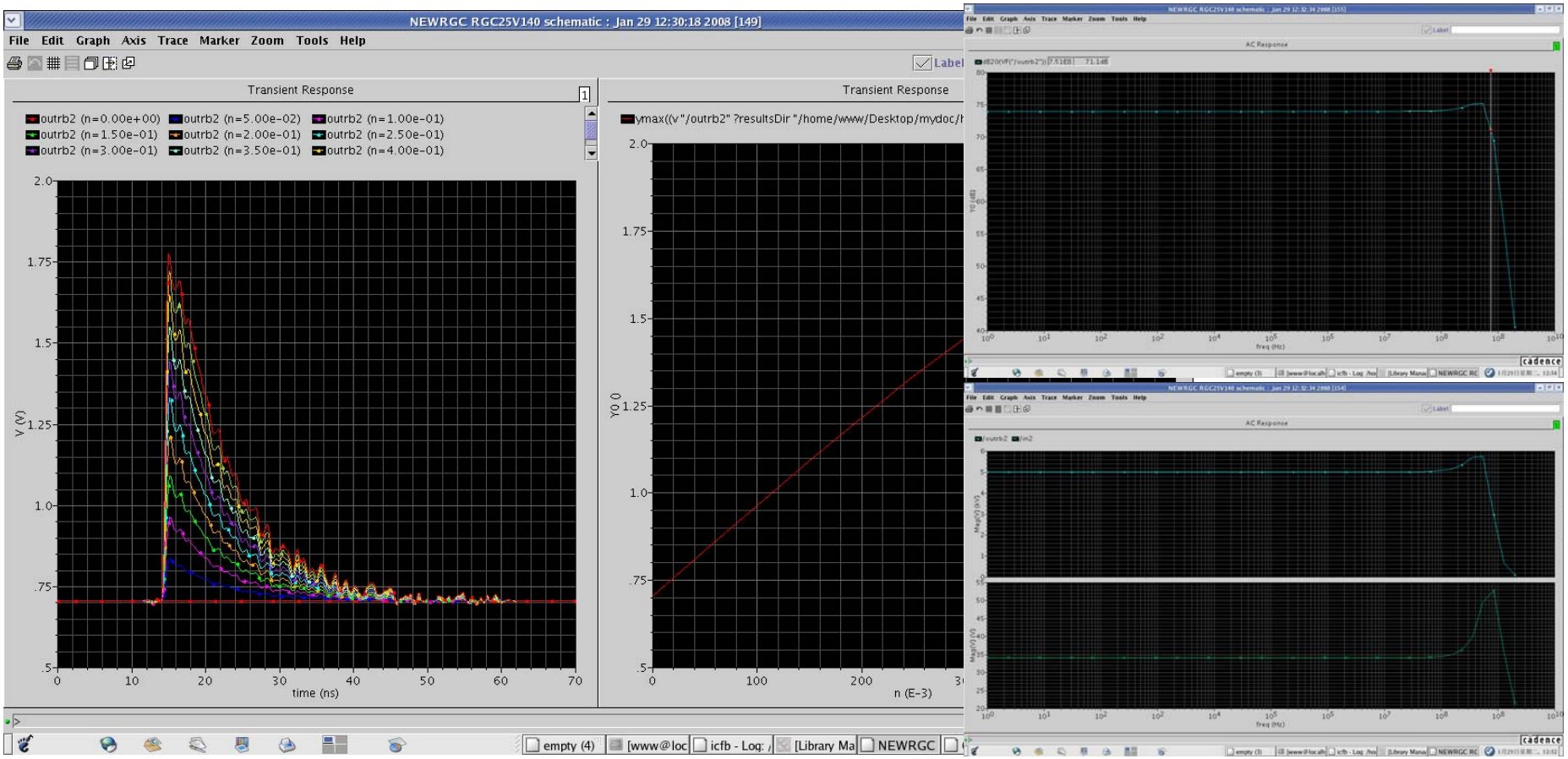
RGC_TIA Circuit



TDS Scope (>1GHz ABW) Measure

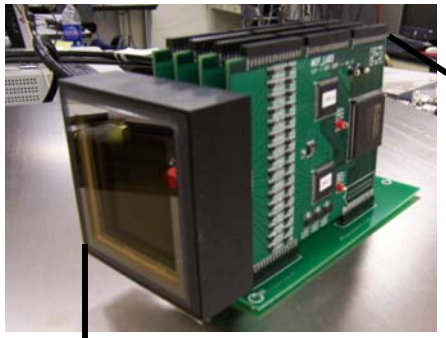


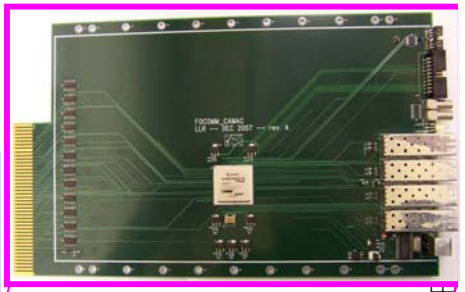
Simulated Performance



- Meets specs on previous slide
- 5k → ~100mV
- Sample noise ~2mV, if match input noise: 13pA/sqrt(Hz)
- SNR is then 50:1

Readout System Block Diagram





Giga-bit Fiber

CAMAC For beam-test only!

Photo-Sensor

BLAB2

BLAB2

BLAB2

BLAB2

MCP MAIN

x7

cPCI CARD

x1

cPCI Crate (Linux)

CAMAC CARD

CAMAC Backplane

- Up to 7x64 channels per cPCI card
- CAMAC card for SLAC beam test
- Up to 32,256 channels/cPCI crate

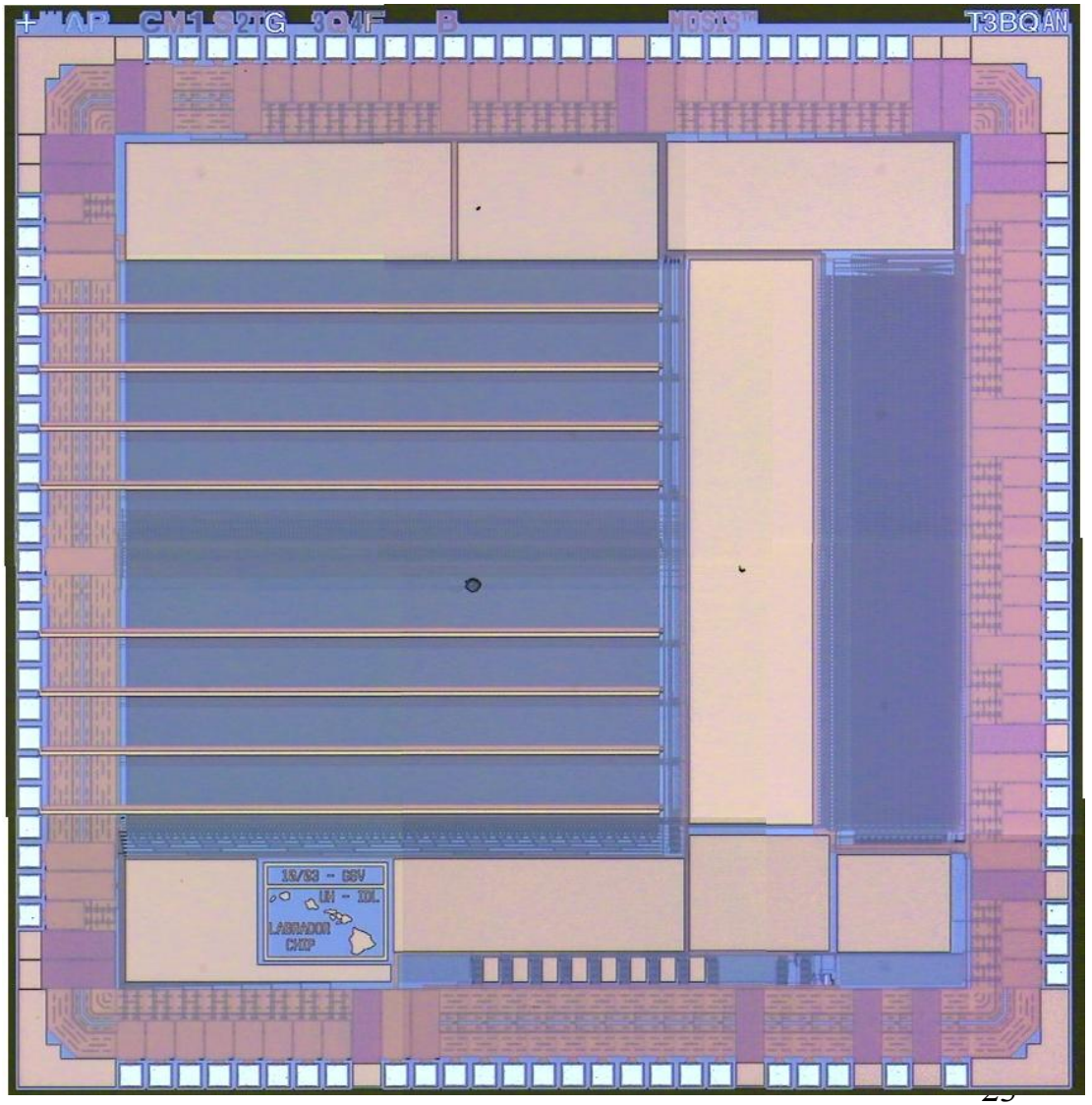
Very cost effective, board hardware already exists

Summary

Building toward a major system test

- Great progress toward dream of "ps" timing extraction being realized
- Demonstrator system for full detector readout
- No show-stoppers
- Get serious about a "1%" system (640) test? Readout all 448 channels of FDIRC proto [Sept?]
- What needed for demonstration in light of upcoming TDR?

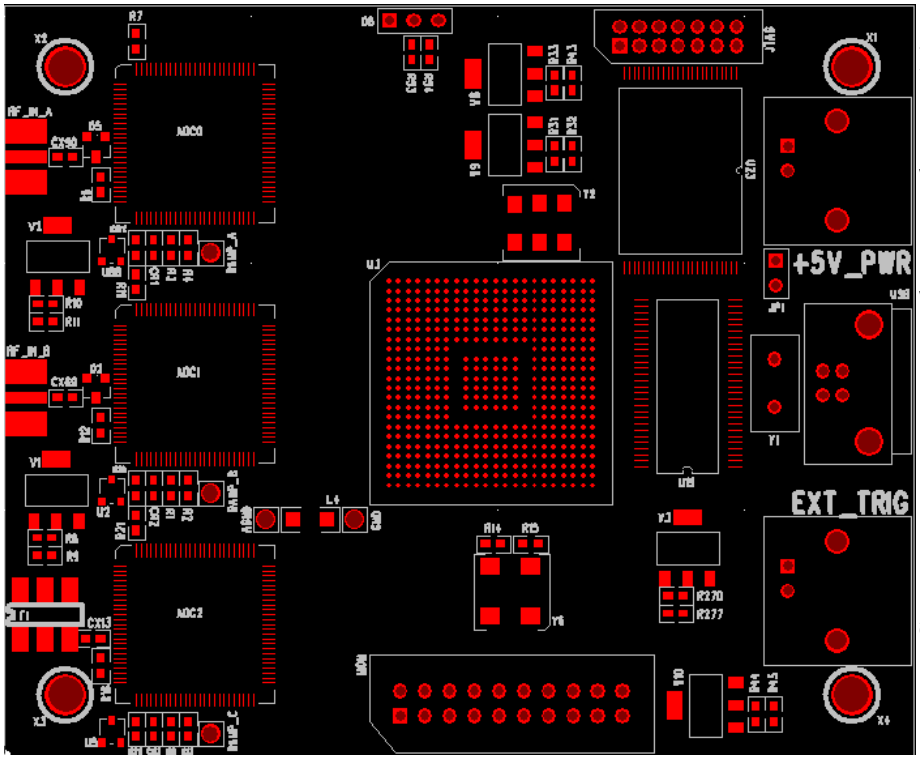
Back-up slides



Why use the Cross-Correlation Method?

- Universal method to find the time between the peaks of any two functions
- Cross-Correlation can be done in firmware

  => **“an online solution”**
- Currently Larry Ruckman working on a developing firmware to determine the required FPGA resources and readout speed for this method
- Demo board at left ➔

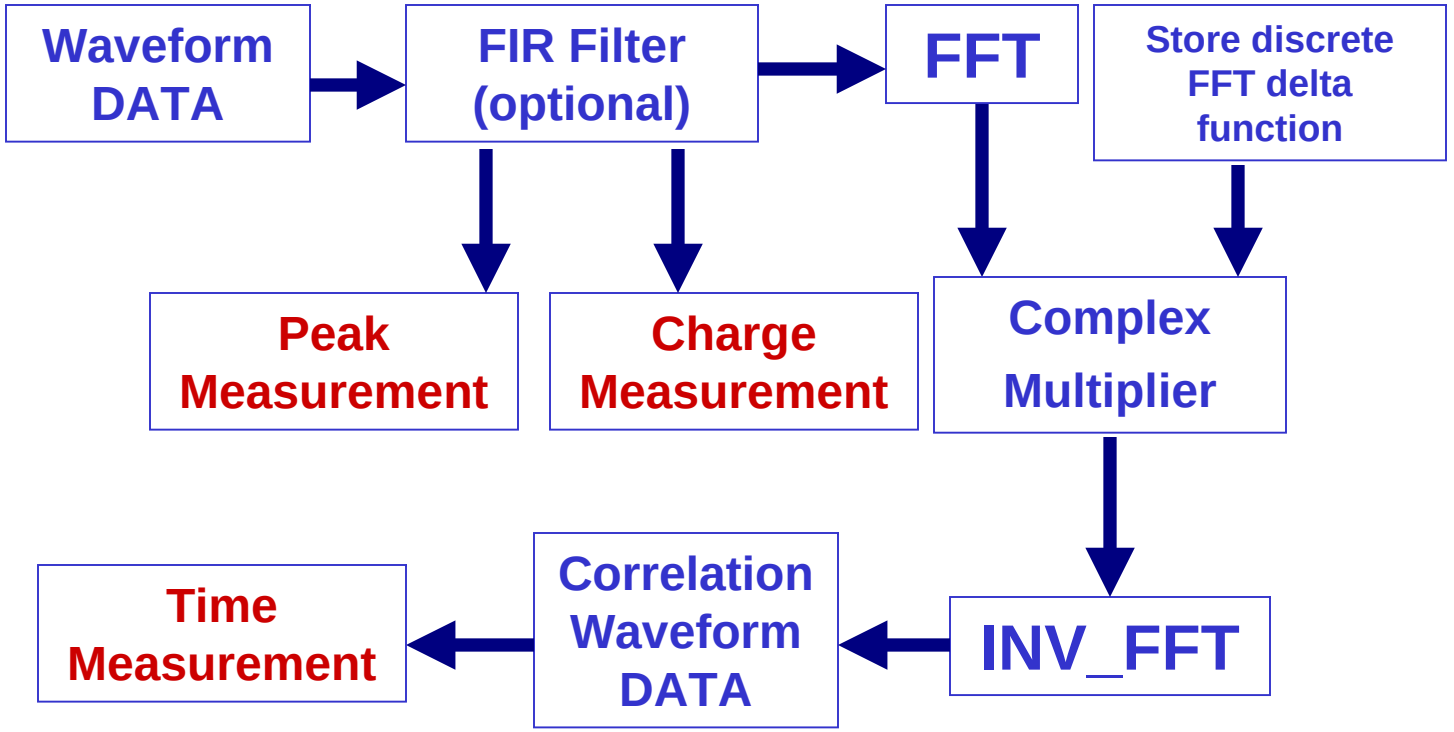


This next generation proto-board (larger FPGA) already in works,

Could mount pair MPPCs on front to measure timing performance (in beam)

Cross-Correlation with Firmware

- FFT, INV_FFT, FIR Filter, and Complex Multiplier are free IP cores from Xilinx



Cost Estimates

- Alternative to MCP-PMT: GaAs Geiger-mode APD
  - Estimate is $10-$40/cm^2
  - Fall-back is MPPCs (but not rad. Hard, poor timing)
- ASIC costing well understood, very competetive!