Study on:
Camera readout options and ADC components

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1. Camera readout options

Option 1: F. Grabber + FPGA

Komodo
CoaXPress
Frame Grabber with 8 channels

Ordering Information	KY-FGK-801

KAYA INSTRUMENTS

Komodo CXP Reference Guide

(Part-No. KY-FGK)

April 2019

www.kayainstruments.com

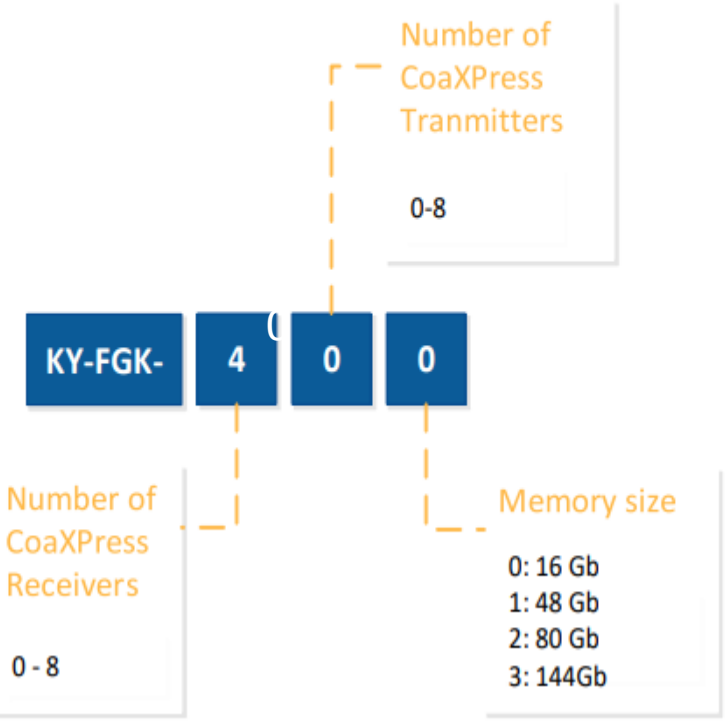
Option 1: F. Grabber + FPGA

Ordering codes

Komodo
CoaXPress
Frame Grabber with 8 channels

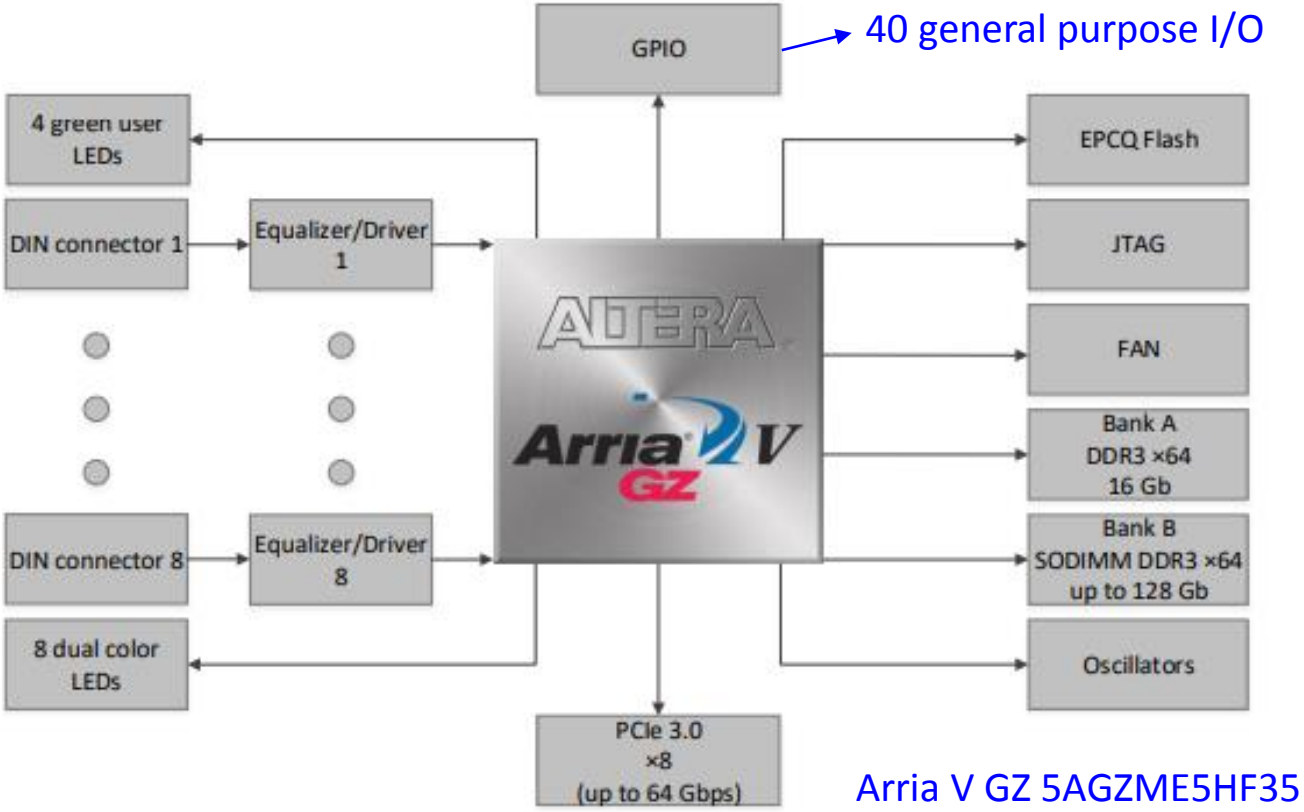
Ordering Information	KY-FGK-801

3.5 **Ordering Codes**



Option 1: F. Grabber + FPGA

Block Diagram



- The JTAG programming header provides a method for configuring the FPGA using an external USB-Blaster device with the Quartus II Programmer running on a PC.
- The Komodo CXP has an on board EPCQ256 flash memory for power up configuration

Option 1: F. Grabber + FPGA

Features

- 8 x CoaXPress channels at 6.25 Gbps each
- PCIe Gen3 x8 Half-length card
- Up to 144 Gb of DDR3 memory
- Altera Arria V GZ FPGA with:
  - NIOS II processor
  - 400K equivalent LEs
  - 1092 DSP blocks
  - 28Mbit of embedded memory
  - Hard IP PCIe Gen 3.0 block
- Supports Altera's PCIe IP
- Supports KAYA CoaXPress IP
- Supports Memory controller IPs
- Transfer Rate up to 60 Gbps through PCIe
- Transfer Rate up to 50 Gbps (8 x 6.25 Gbps) through the CoaXPress interfaces

40 flexible machine I/Os:

- 8 TTL configurable I/Os
- 8 LVCMOS configurable I/Os
- 4 LVDS inputs
- 4 LVDS outputs
- 8 opto-isolated outputs
- 8 opto-isolated inputs

Option 1: F. Grabber + FPGA

Asking KAYA company...

Question:

We need to implement some trigger structure based on some image processing methods in the board using therefore a custom algorithm.

Would it be possible to do it with this board using its FPGA device? Is there any document explaining how to add algorithms to the reference design offered by KAYA?

Answer:

Unfortunately, we are unable to load to user logic to the frame grabber FPGA.

Alternatively we can offer a two options:

1. Embed your user logic to our design based on NRE. This is subject to a discussion on the opportunity size, as we are heavily invested in several projects.
2. You can use our vast I/O trigger configuration in order to achieve your goal. This can be modified via our provided API.

Can you please share with us more information about your project, opportunity size, time frame etc.. This can be very helpful for us, so we could provide you with suitable solution.

Option 2: F. Grabber + GPU

GPU Solutions

Accelerated Processing & Reduced Latency

- **Support for NVIDIA's GPUDirect for Video**
- **Support for AMD's DirectGMA**
- **SDK sample code available**
- **Easy integration of modern GPU processing**

Active Silicon
COMPUTER IMAGING PRODUCTS

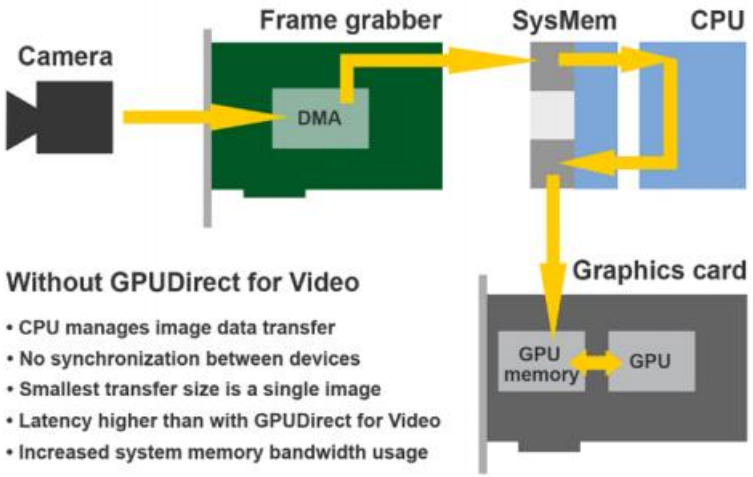
FEATURES

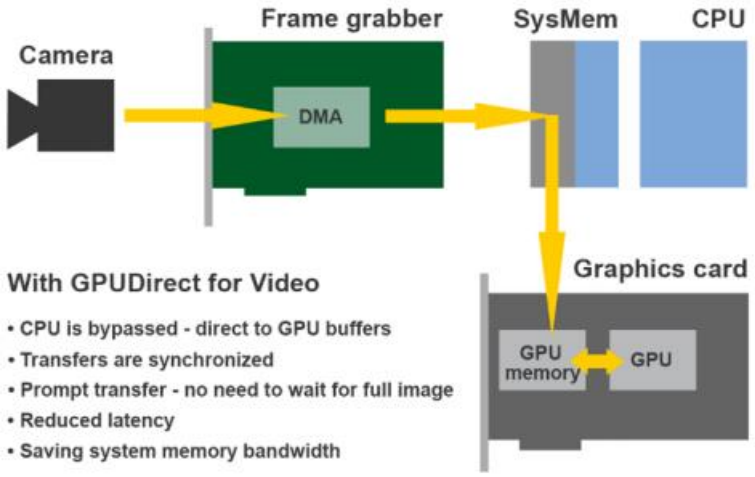
- All FireBird and Phoenix frame grabbers compatible with GPUDirect for Video and DirectGMA.
- GPU memory directly accessible to frame grabber.
- CPU is bypassed.
- Immediate image transfer – no need to wait for full image.
- All devices are synchronized.
- Reduced latency.
- Reduced system memory bandwidth usage.

NVIDIA and AMD

Option 2a: CoaXPress + GPU

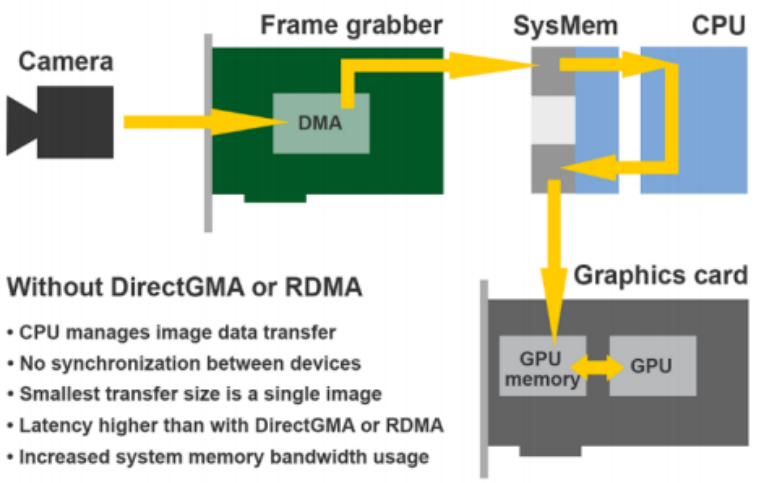
- NVIDIA GPUDirect™ for Video
  - Helps IO board manufacturers write device drivers that efficiently transfer video frames in and out of NVIDIA GPU memory.

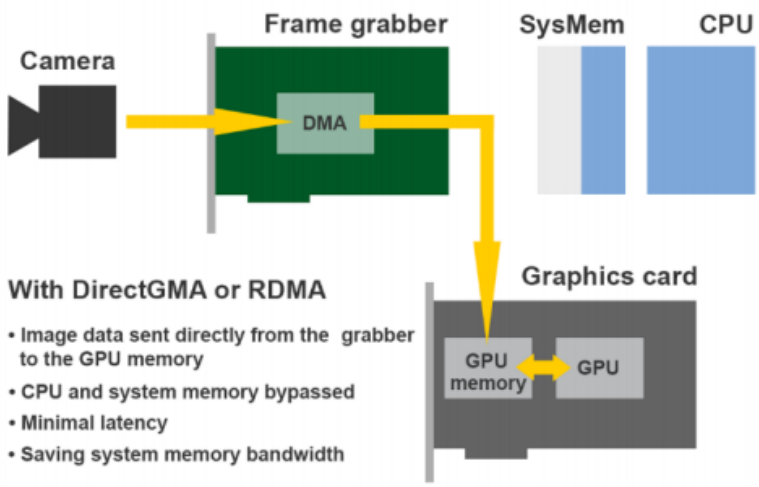




Option 2b: CoaXPress + GPU

- AMD's DirectGMA
  - This allows the frame grabber to DMA image data directly into GPU memory, with no CPU involvement at all and bypassing system memory completely, resulting in minimal latency data transfer with the added benefit of saving memory bandwidth.





Option 2: F. Grabber + GPU

- Example of a compatible F. Grabber

euresys
Empowering Computer Vision

Coaxlink Octo

PCIe 3.0 eight-connection CoaXPress frame grabber

At a Glance

- Eight CoaXPress CXP-6 connections: 5,000 MB/s camera bandwidth
- Connect up to eight CoaXPress cameras to one card
- PCIe 3.0 (Gen 3) x8 bus: 6,700 MB/s bus bandwidth
- Feature-rich set of 10 digital I/O lines
- Extensive camera control functions
- Memento Event Logging Tool

Conclusions

- FPGA solution
  - Simpler hardware solution
  - Lower cost (250 USD per channel)
  - More difficult to program (VHD - probably not possible)

All these statements must be investigated more deeply

- GPU solution
  - More devices needed (F. Grabber + GPU board)
  - Higher cost (should be investigated)
  - Easier to program (Python is a possibility)
  - Probably more image processing capability (speed, algorithms, etc)

2. ADC components for CYGNO PM-DAQ

Some ADC options

ANALOG DEVICES

8-Bit, 500 MSPS, 1.8 V Analog-to-Digital Converter (ADC)

Data Sheet AD9286

FEATURES

- Single 1.8 V supply operation
- SNR: 49.3 dBFS at 200 MHz input at 500 MSPS
- SFDR: 65 dBc at 200 MHz input at 500 MSPS
- Low power: 315 mW at 500 MSPS
- On-chip interleaved clocking
- On-chip reference and track-and-hold
- 1.2 V p-p analog input range for each channel
- Differential input with 500 MHz bandwidth
- LVDS-compliant digital output
- On-chip voltage reference and sample-and-hold circuit
- DNL: ±0.2 LSB
- Serial port control options
  - Interleaved clock timing adjustment
  - Offset binary, Gray code, or twos complement data format
  - Optional clock duty cycle stabilizer
  - Built-in selectable digital test pattern generation
- Pin-programmable power-down function
- Available in 48-lead LFCSP

GENERAL DESCRIPTION

The AD9286 is an 8-bit, monolithic sampling, analog-to-digital converter (ADC) that supports interleaved operation and is optimized for low cost, low power, and ease of use. Each ADC operates at up to a 250 MSPS conversion rate with outstanding dynamic performance.

The AD9286 takes a single sample clock and, with an on-chip clock divider, time interleaves the two ADC cores (each running at one-half the clock frequency) to achieve the rated 500 MSPS. By using the SPI, the user can accurately adjust the timing of the sampling edge per ADC to minimize the image spur energy.

The ADC requires a single 1.8 V supply and an encode clock for full performance operation. No external reference components are required for many applications. The digital outputs are LVDS compatible.

The AD9286 is available in a Pb-free, 48-lead LFCSP that is specified over the industrial temperature range of −40°C to +85°C.

- Dual channel
- 500 MSPS
- 8 bits (ENOB = 7.9 bits)
- 1.2 Vpp input range

- Unit Price: USD 43 ($22/ch)

ANALOG DEVICES

14-Bit, 500 MSPS LVDS, Dual Analog-to-Digital Converter

Data Sheet AD9684

FEATURES

- Parallel LVDS (DDR) outputs
- 1.1 W total power per channel at 500 MSPS (default settings)
- SFDR = 85 dBFS at 170 MHz f_{IN} (500 MSPS)
- SNR = 68.6 dBFS at 170 MHz f_{IN} (500 MSPS)
- ENOB = 10.9 bits at 170 MHz f_{IN}
- DNL = ±0.5 LSB
- INL = ±2.5 LSB
- Noise density = −153 dBFS/Hz at 500 MSPS
- 1.25 V, 2.50 V, and 3.3 V supply operation
- No missing codes
- Internal analog-to-digital converter (ADC) voltage reference
- Flexible input range and termination impedance
  - 1.46 V p-p to 2.06 V p-p (2.06 V p-p nominal)
  - 400 Ω, 200 Ω, 100 Ω, and 50 Ω differential
- SYNC± input allows multichip synchronization
- DDR LVDS (ANSI-644 levels) outputs
- 2 GHz usable analog input full power bandwidth
- >96 dB channel isolation/crosstalk
- Amplitude detect bits for efficient AGC implementation
- Two integrated wideband digital processors per channel

FUNCTIONAL BLOCK DIAGRAM

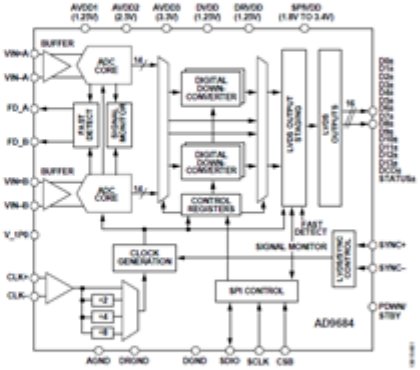


Figure 1.

GENERAL DESCRIPTION

- Dual channel
- 500 MSPS
- 14 bits (ENOB = 10 bits)
- 2.06 Vpp input range

- Unit Price: USD 320 ($160/ch)

Some ADC options

TEXAS INSTRUMENTS

ADC08D502

www.ti.com

SNOSC85A – AUGUST 2012 – REVISED APRIL 2013

ADC08D502 High Performance, Low Power, Dual 8-Bit, 500 MSPS A/D Converter

Check for Samples: ADC08D502

FEATURES

- Internal Sample-and-Hold
- Single +1.9V ±0.1V Operation
- Choice of SDR or DDR Output Clocking
- Multiple ADC Synchronization Capability
- Specified No Missing Codes
- Serial Interface for Extended Control
- Fine Adjustment of Input Full-Scale Range and Offset
- Duty Cycle Corrected Sample Clock

APPLICATIONS

- Direct RF Down Conversion
- Digital Oscilloscopes
- Satellite Set-top boxes
- Communications Systems
- Test Instrumentation

KEY SPECIFICATIONS

- Resolution: 8 Bits
- Max Conversion Rate: 500 MSPS (min)
- Bit Error Rate: 10^{-18} (typ)
- ENOB @ 250 MHz Input: 7.5 Bits (typ)

DESCRIPTION

The ADC08D502 is a dual, low power, high performance CMOS analog-to-digital converter that digitizes signals to 8 bits resolution at sampling rates up to 500 MSPS. Consuming a typical 1.4 Watts at 500 MSPS from a single 1.9 Volt supply, this device is specified to have no missing codes over the full operating temperature range. The unique folding and interpolating architecture, the fully differential comparator design, the innovative design of the internal sample-and-hold amplifier and the self-calibration scheme enable a very flat response of all dynamic parameters beyond Nyquist, producing a high 7.5 ENOB with a 250 MHz input signal and a 500 MHz sample rate while providing a 10^{-18} B.E.R. Output formatting is offset binary and the LVDS digital outputs are compatible with IEEE 1596.3-1996, with the exception of an adjustable common mode voltage between 0.8V and 1.2V.

Each converter has a 1:2 demultiplexer that feeds two LVDS buses and reduces the output data rate on each bus to half the sampling rate.

The converter typically consumes less than 3.5 mW in the Power Down Mode and is available in a 128-lead, thermally enhanced exposed pad HLQFP and operates over the Industrial ($-40°C \le T_A \le +85°C$) temperature range.

- Dual channel
- 500 MSPS
- 8 bits (ENOB = 7.5 bits)
- 870 mVpp input range

- Unit Price: USD 59 ($30/ch)

TEXAS INSTRUMENTS

ADS5404

www.ti.com

SLAS945B – APRIL 2013 – REVISED JANUARY 2014

Dual Channel 12-Bit 500Msps Analog-to-Digital Converter

Check for Samples: ADS5404

FEATURES

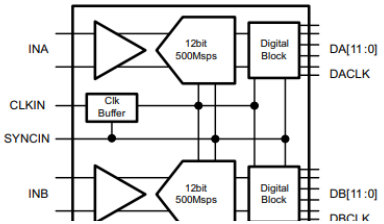
- Dual Channel
- 12-Bit Resolution
- Maximum Clock Rate: 500 Msps
- Low Swing Fullscale Input: 1.0 Vpp
- Analog Input Buffer with High Impedance Input
- Input Bandwidth (3 dB): >1.2 GHz
- Data Output Interface: DDR LVDS
- 196-Pin BGA Package (12x12mm)
- Power Dissipation: 910 mW/ch
- Performance at f_{in} = 230 MHz IF
  - SNR: 60.6 dBFS
  - SFDR: 77 dBc
- Performance at f_{in} = 700 MHz IF
  - SNR: 59.4 dBFS
  - SFDR: 70 dBc

APPLICATIONS

- Test and Measurement Instrumentation
- Ultra-Wide Band Software Defined Radio
- Data Acquisition

DESCRIPTION

The ADS5404 is a high linearity dual channel 12-bit, 500 MSPS analog-to-digital converter (ADC) easing front end filter design for wide bandwidth receivers. The analog input buffer isolates the internal switching of the on-chip track-and-hold from disturbing the signal source as well as providing a high-impedance input. Optionally the output data can be decimated by two. Designed for high SFDR, the ADC has low-noise performance and outstanding spurious-free dynamic range over a large input-frequency range. The device is available in a 196-pin BGA package and is specified over the full industrial temperature range (–40°C to 85°C).



- Dual channel
- 500 MSPS
- 12 bits (ENOB = 9.8 bits)
- 1.0 Vpp input range

- Unit Price: USD 220 ($110/ch)