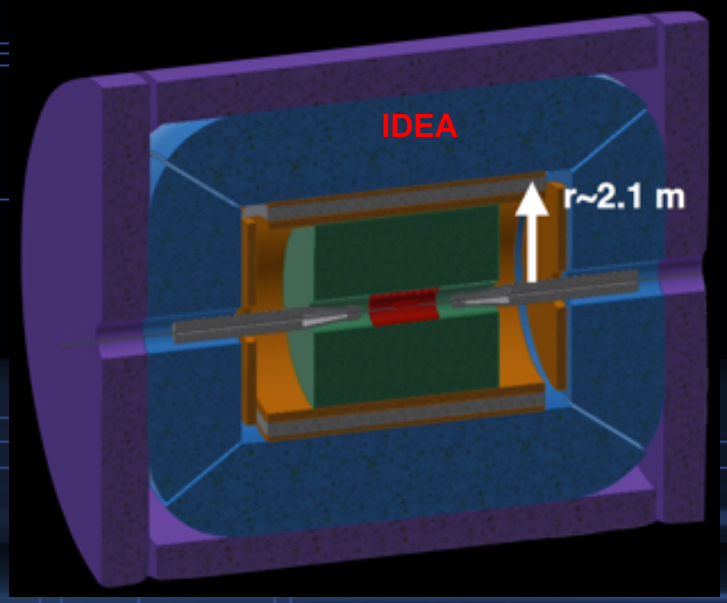
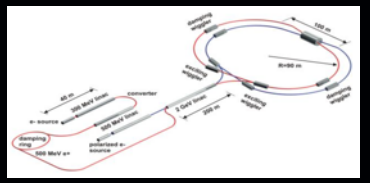


RD_FA
Drift Chamber

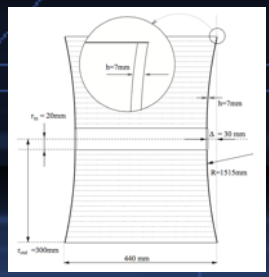
F. Grancagnolo
N. De Filippis

referees CSN1
11 Marzo, 2020

Super charm/tau
Factory at BINP



CMD-3 at
VEPP-2000



Activity #1 2020

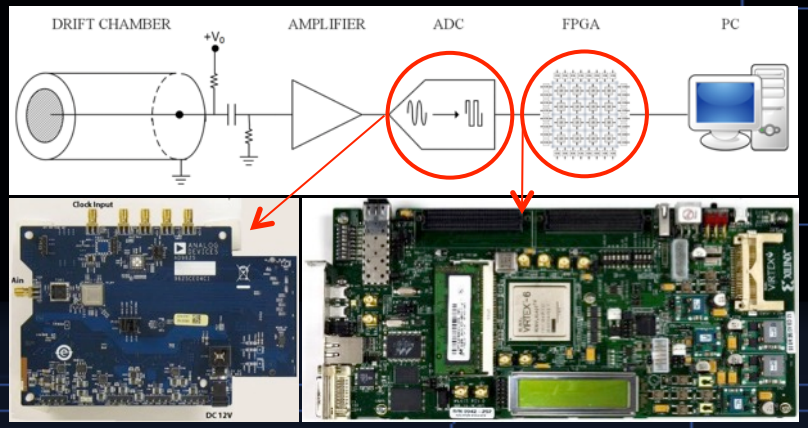
Cluster Counting/Timing: data reduction and pre-processing of drift chamber signals sampled at high rate. Multi-channel version with improved peak finding algorithms.

The verified solution for a **single channel**

The solution consists in transferring, for each hit drift cell, **instead of the full spectrum of the signal**, only the minimal information relevant to the application of the cluster timing/counting techniques, i.e. **the amplitude and the arrival time of each peak associated with each individual ionisation electron**.

This is accomplished by using a **FPGA** for the real time analysis of the data generated by the drift chamber and successively digitized by an ADC.

A fast readout algorithm (**CluTim**) for identifying, in the digitized drift chamber signals, the individual ionization peaks and recording their time and amplitude has been developed as **VHDL/Verilog** code implemented on a **Virtex 6 FPGA**, which allows for a maximum input/output clock switching frequency of **710 MHz**. The hardware setup includes also a 12-bit monolithic **pipeline sampling ADC** at conversion rates of up to **2.0 GSPS**.



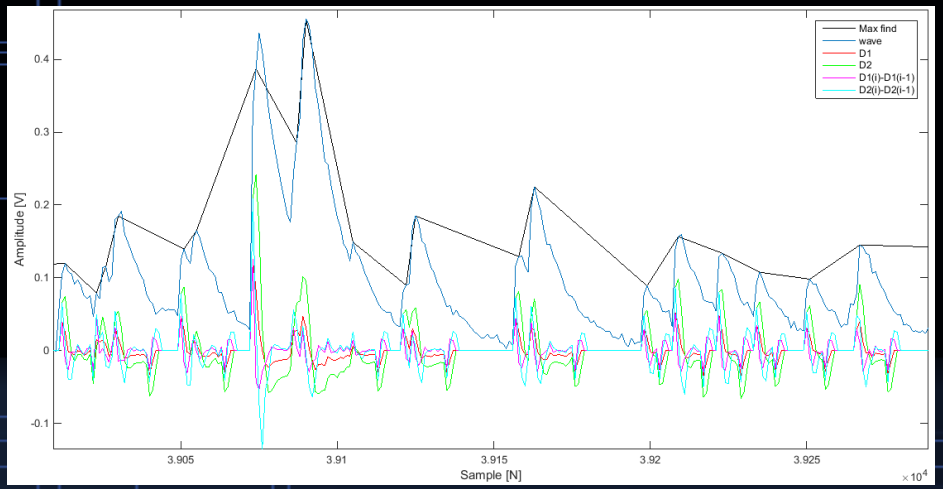
AD9625-2.0EBZ Evaluation Board

Xilinx ML605 Evaluation Board

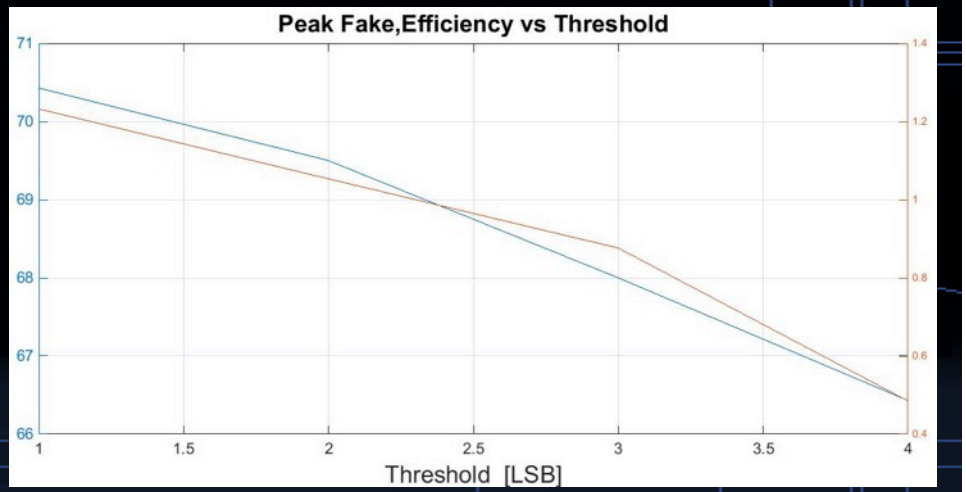
G. Chiarello, C. Chiri, G. Cocciolo, A. Corvaglia, F. Grancagnolo, M. Panareo, A. Pepino and G. Tassielli
The Use of FPGA in Drift Chambers for High Energy Physics Experiments
ISBN 978-953-51-3208-0, Print ISBN 978-953-51-3207-3, May 31, 2017, doi:10.5772/66853, http://dx.doi.org/10.5772/66853

Example: CluTim algorithm

At the beginning of the signal processing procedure, a counter starts to count, providing the timing information related to the signal under scrutiny. The determination of a peak is done by relating the i-th sampled bin to a number n of preceding bins, where n is related to the rise times of the signal peak. Once a peak is found, it is sent to pipeline memories which are continuously filled as new peaks are found. When a trigger signal occurs at time t_0, the reading procedure is enabled and only the data relative to the found peaks in the $[t_0; t_0 + t_{max}]$ time interval are transferred to an external device



Input signal, values of the auxiliary functions and found peaks.

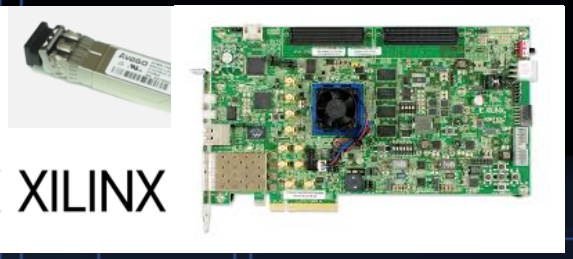


Efficiency and fake rate

Finanziamento 2019 da CSN1 : 2+2 Keuro

KIT EVAL ULTRASCALE FPGA KCU105

- KINTEX® UltraScale™ XCKU040-2FFVA1156E
- Quadruplo generatore di clock a frequenza fissa Si5335A
- Transceiver 20 GTH
- 2 moduli SFP+ da 10Gbps



AD9689 - 2000EBZ

- 14-bit
- Dual channel
- 2.6 GSPS
- JESD204B
- 1,55W at 2,6 GSPS

INFN
Istituto Nazionale di Fisica Nucleare
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Via Arnesano
73100 LECCE (LE)
Telefono: +39 0832 325127
Fax: +39 0832 325128

prot@le.infn.it

Ordine di acquisto n. 1630 del 25-OTT-19
(Da citare in fattura, nelle comunicazioni e sugli imballaggi)
Vs. riferimento rdo mepa
Codice Fornitore INFN: 19263
Ns. Riferimento CIG ZE72A15F91
Codice Univoco Ufficio di Fatturazione Elettronica: LR2ADE

Spett.le
CARTO COPY SERVICE SRL
VIA ADOLFO OMODEO, 21
00179 ROMA RM Italia
P.IVA 04864781002

Con la presente ci pregiamo ordinarvi quanto segue, alle condizioni sottoindicate:

Descrizione sintetica: Sistema di acquisizione dati

QUANTITA'	DESCRIZIONE	SCONTO	%	PREZZO UNITARIO	IMPORTO
1,0	EK-U1-KCU105-G	0,00	0	3.082,19	3.082,19
1,0	AD9689-2000EBZ-ND	0,00	0	1.272,45	1.272,45

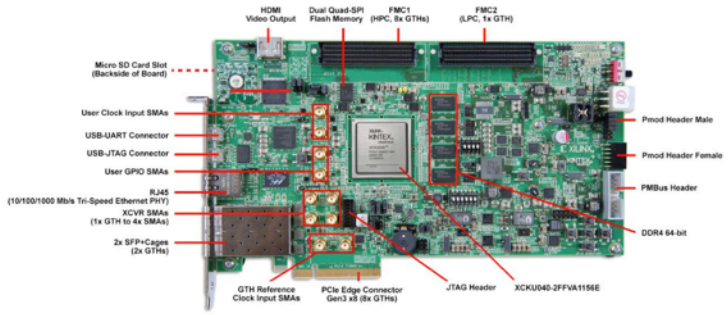
IVA AL 22% EUR 968,02
TOTALE EUR : 4.354,64
TOTALE EUR (Ivato): 5.312,66

LUOGO DI CONSEGNA	Via Arnesano 73100 LE IT
TERMINE DI CONSEGNA	30 Giorni
METODO DI SPEDIZIONE	Vs. Carico
PAGAMENTO	30 GG. D.R.F.
SUBAPPALTO	Il subappalto parziale o totale del presente contratto non e' permesso senza autorizzazione formale dell'INFN
GIURISDIZIONE	Per qualsiasi controversia relativa al presente contratto e' competente, in via esclusiva, il Foro di Roma
NORME DI SICUREZZA	la commessa deve essere conforme alla legislazione vigente in materia di sicurezza sul lavoro
SPLIT PAYMENT	E' OBBLIGATORIO A PARTIRE DAL 01/07/17 (ART.1 D.L. 50/2017)
MATERIA DI ANTICORRUZIONE	Il fornitore e' obbligato a seguire quanto disposto dal Codice di comportamento in materia di Anticorruzione del personale INFN pubblicato nella sezione" amministrazione trasparente" sul sito WWW.INFN.IT
Resp. Unico del Procedimento	CORVAGLIA ALESSANDRO — Indirizzo Mail alessandro.corvaglia@le.infn.it
Alla consegna Contattare	Corvaglia Alessandro

IL RESPONSABILE AMMINISTRATIVO
RAG. DANILA GENTILE

IL DIRETTORE
DOTT. FABIO ROSSI

XILINX Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit



Configuration

- Onboard JTAG configuration circuitry to enable configuration over USB
- JTAG header provided for use with Xilinx download cables such as the Platform Cable USB II
- Quad SPI Flash with 2 x 256 Mb of non-volatile storage

Memory

- 2GB DDR4 component memory (four [256 Mb x 16] devices) at 1200MHz / 2400Mbpsps
- 64MB (512Mb) Quad SPI Flash
- 8Kb IIC EEPROM
- Micro SD Card Slot

Communication & Networking

- Gigabit Ethernet GMII, RGMII and SGMII
- 2x SFP / SFP+ cage
- GTX port (TX, RX) with four SMA connectors
- UART To USB Bridge
- PCI Express x8 edge connector

Expansion Connectors

- FMC-HPC (Partial Population) connector (8 GTX Transceiver, 114 single-ended or 57 differential (34 LA & 24 HA) user defined signals)
- FMC-LPC connector (1 GTX Transceiver, 68 single-ended or 34 differential user defined signals)
- 2x PMOD headers
- IIC

Display

- HDMI Video output
- External Phy/codec device driving an HDMI Connector
- 8x GPIO user LEDs

Clocking

- 8x programmable clocks
- System clocks, EMC clock, user clocks, Jitter attenuated clocks
- 2x SMA input clocks

Control & I/O

- 5X Directional Push Buttons
- 4X DIP Switches
- 1x Rotary switch
- Diff Pair I/O (1 SMA pair)

Power

- 12V wall adapter or ATX

ANALOG DEVICES 14-Bit, 2.0 GSPS/2.6 GSPS, JESD204B, Dual Analog-to-Digital Converter

Data Sheet **AD9689**

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
  - Support for lane rates up to 16 Gbps per lane
- Noise density
  - −152 dBFS/Hz at 2.56 GSPS at full-scale voltage = 1.7 V p-p
  - −154 dBFS/Hz at 2.56 GSPS at full-scale voltage = 2.0 V p-p
  - −154.2 dBFS/Hz at 2.0 GSPS at full-scale voltage = 1.7 V p-p
  - −155.3 dBFS/Hz at 2.0 GSPS at full-scale voltage = 2.0 V p-p
- 1.55 W total power per channel at 2.56 GSPS (default settings)
- SFDR at 2.56 GSPS encode
  - 73 dBFS at 1.8 GHz A_{IN} at −2.0 dBFS
  - 59 dBFS at 5.53 GHz A_{IN} at −2.0 dBFS
  - full-scale voltage = 1.1 V p-p
- SNR at 2.56 GSPS encode
  - 59.7 dBFS at 1.8 GHz A_{IN} at −2.0 dBFS
  - 53.0 dBFS at 5.53 GHz A_{IN} at −2.0 dBFS
  - full-scale voltage = 1.1 V p-p
- SFDR at 2.0 GSPS encode
  - 78 dBFS at 900 MHz A_{IN} at −2.0 dBFS
  - 62 dBFS at 5.53 GHz A_{IN} at −2.0 dBFS
  - full-scale voltage = 1.1 V p-p
- SNR at 2.0 GSPS encode
  - 62.7 dBFS at 900 MHz A_{IN} at −2.0 dBFS
  - 53.1 dBFS at 5.5 GHz A_{IN} at −2.0 dBFS
  - full-scale voltage = 1.1 V p-p
- 0.975 V, 1.9 V, and 2.5 V dc supply operation
- 9 GHz analog input full power bandwidth (−3 dB)
- Amplitude detect bits for efficient AGC implementation
- Programmable FIR filters for analog channel loss equalization
- 2 integrated, wideband digital processors per channel
  - 48-bit NCO
  - Programmable decimation rates
- Phase coherent NCO switching
  - Up to 4 channels available
- Serial port control
  - Supports 100 MHz SPI writes and 50 MHz SPI reads
  - Integer clock with divide by 2 and divide by 4 options
  - Flexible JESD204B lane configurations
- On-chip dither

APPLICATIONS

- Diversity multiband and multimode digital receivers
- 3G/4G, TD-SCDMA, W-CDMA, and GSM, LTE, LTE-A
- Electronic test and measurement systems
- Phased array radar and electronic warfare
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers

FUNCTIONAL BLOCK DIAGRAM

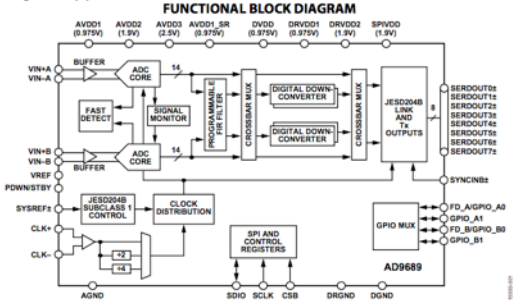


Figure 1.

Test da effettuare nel corso del 2020:

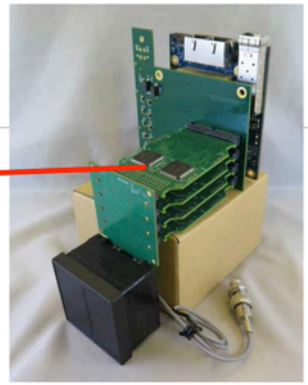
- Implementazione dell'algoritmo originario di cluster counting/timing sulla nuova FPGA, questo permetterà di migliorare la velocità di trasferimento
- Utilizzo della massima banda di trasmissione dei dati tra ADC multi canale (per adesso 2) e FPGA
- Implementazione di nuovi algoritmi di cluster counting/timing per migliorare l'efficienza e limitare il "fake rate"
- Test dell'algoritmo prima con segnali simulati e successivamente con segnali reali
  - su segnali reali si possono anche implementare delle tecniche di filtraggio digitali con le features della nuova FPGA

SiREAD chip

SiREAD: a low-cost, low power and high density System-on Chip (SoC) capable of analog signal conditioning, fast waveform sampling and integrated readout and signal processing capabilities. The SiREAD device will also have calibration and monitoring circuitry in addition to a deep sampling buffer making it suitable for large HEP experiments. Design and development of the advanced SiREAD chip is built by integrating into one SoC analog signal conditioning circuits and bias monitoring and digital readout and signal processing block capabilities (triggering, sparsification and data reduction).

Synergies: MaPMT Readout for EIC R&D

Photograph of the 64 channel SiREAD based (2x SiREAD rev.1) readout card as a building block for the 256 MA-PMT readout.



Photograph of the first generation of 256-anode 2" PMT readout for use with mRICH prototype in the Fermilab beam test facility.

Nalu Scientific SBIR Project: ASoC

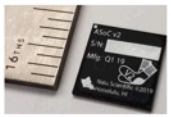
Compact, high performance waveform digitizer

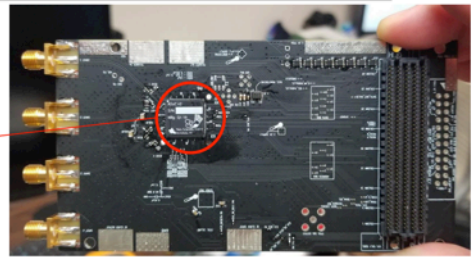
Nalu Scientific
Data Acquisition Systems

Parameter	Spec (measured)
Sample rate	2.4-3.2GSa/s
Number of Channels	4
Sampling Depth	16kSa/channel
Signal Range	0-2.5V
Resolution	12 bits*
Supply Voltage	2.5V
RMS noise	~1 mV
Digital Clock frequency	25MHz
Timing resolution	<25ps**
Power	140mW/channel
Analog Bandwidth	950MHz

Key Contribution:

- High performance digitizer: 3+ Gsa/s
- Highly integrated
- Commercially available
- 5mm x 5mm die size





Chip fabricated in 250nm CMOS
Very low cost to prototype and mass produce

All chips, are designed with commercial grade tools and licenses and can be sold once commercialized.

Activity #2 2020

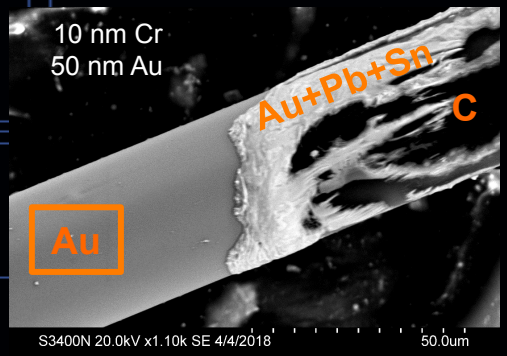
New wire materials for ultra-light drift chambers at the next generation of lepton colliders

C wire metal coating

BINP
A. Popov
V. Logashenko

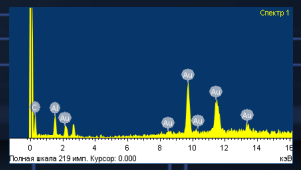
HiPIMS: High-power impulse magnetron sputtering

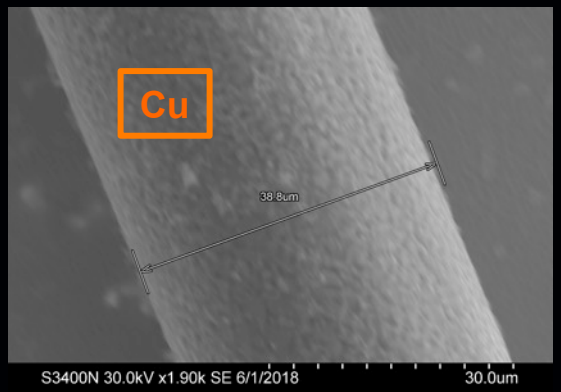
physical vapor deposition (PVD) of thin films based on magnetron sputter deposition (extremely high power densities of the order of kW/cm^2 in short pulses of tens of microseconds at low duty cycle <10%)



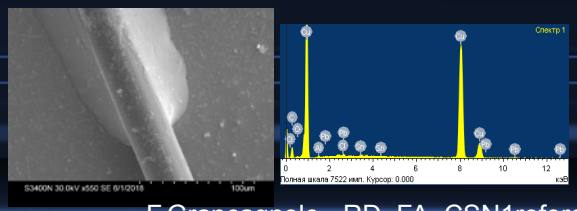
soldering attempt

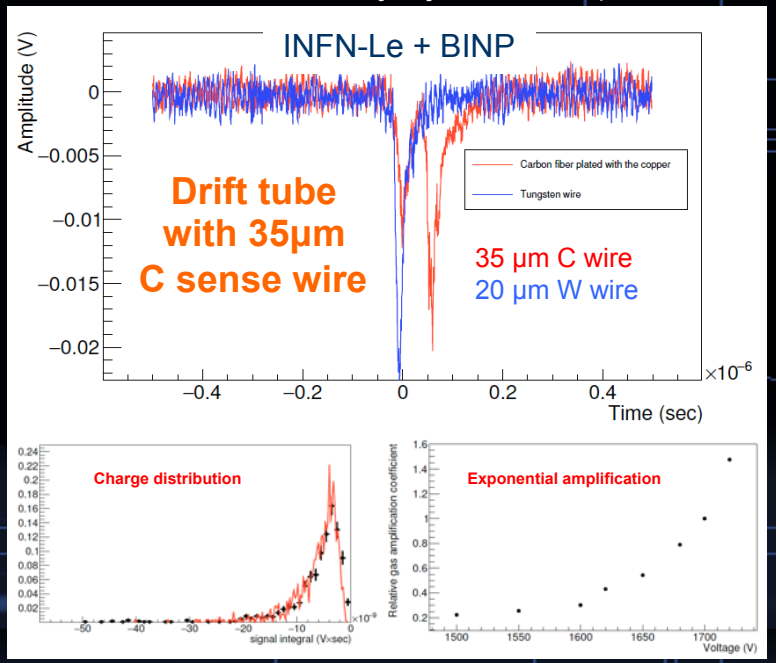
Lead forms intermetallic compound with gold and completely dissolves the 50 nm Au layer.





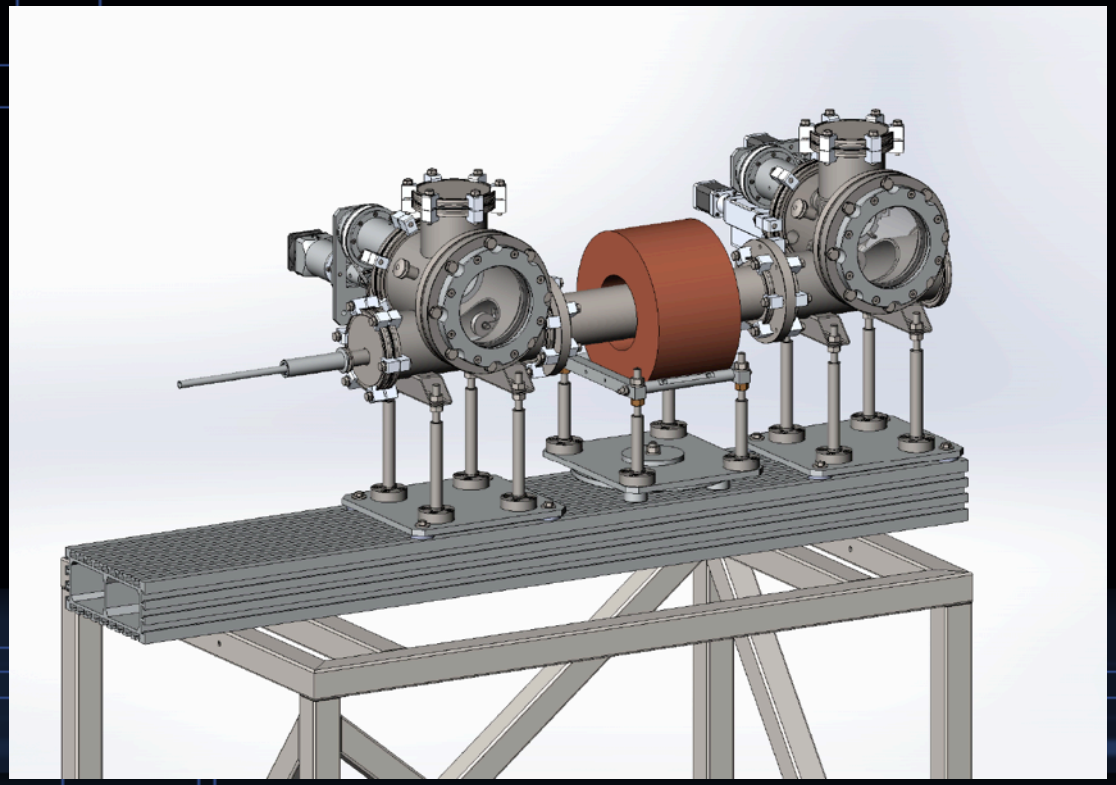
good solder wettability on Cu

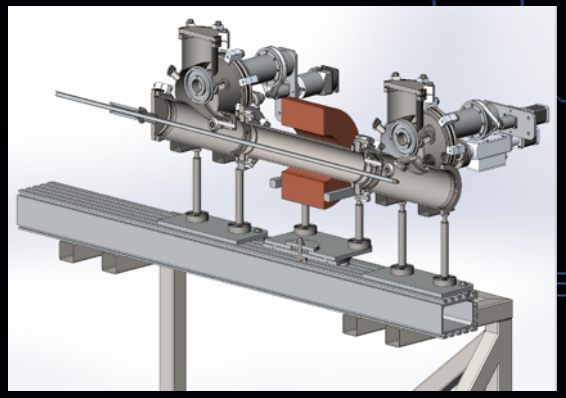


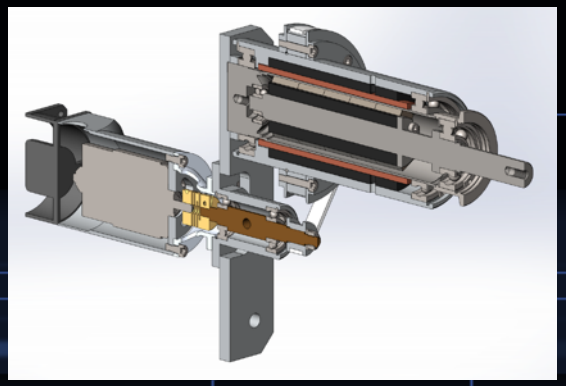


Wire metal coating: BINP proposal

BINP
A. Popov
V. Logashenko







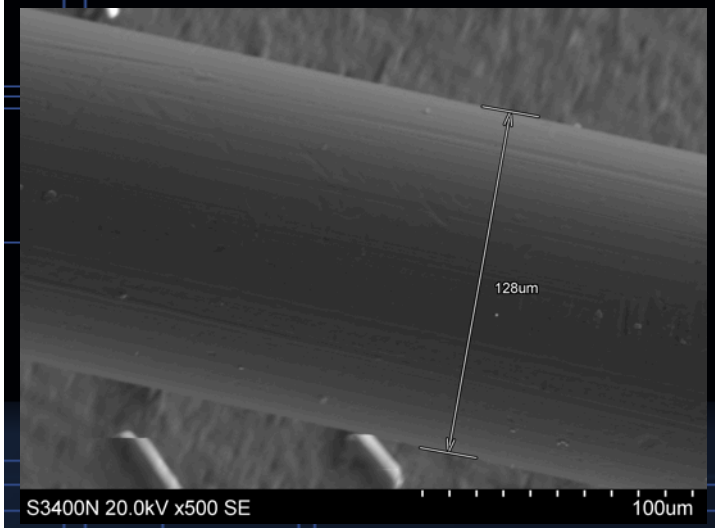
Wire metal coating: BINP real setup

BINP
A. Popov
V. Logashenko

125 μm Al wire Cu coating

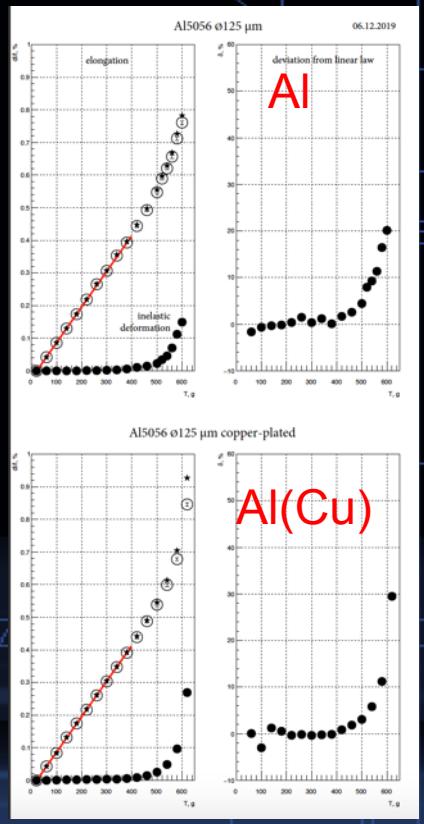
BINP
A. Popov
V. Logashenko

highly uniform coating



good solder wetting

elastic limit



Test da effettuare nel corso del 2020:

- Acquisto monofilamento di Carbonio su opportuna spoletta
- Procuramento di fili polimerici per studi di deposizione di rame
- Test di deposizione di metalli saldabili su polimeri, C, Al, Ti
- Test di saldatura con laser ad IR
- Test di incollaggio con colle conduttive
- Realizzazione di camerette di prova con diversi catodi per studi di ageing
- Realizzazione di un setup a Bari per condivisione test su camerette di prova

Activity #3 2020

Integration in full GEANT4 simulation of drift chamber including track finding and fitting in collaboration with BINP

Activity #4 2020

Participation in WP5 of CREMLINplus "Joint Technology Development around SCT and Future Lepton Colliders"

Task 5.5 "Development and Design of Central Tracker for the SCT Detector"

CREMLIN PLUS

Connecting Russian and European Measures for Large-scale Research Infrastructures

CREMLINplus Kick-off Workshop

19-20 February 2020
DESY,
Notkestrasse 85, 22607 Hamburg

Facts about CREMLINplus

A European-Russian flagship project

- Funded under EU´s Research and innovation Programme Horizon 2020
- EU´s **Flagship project** in the EU-Russian cooperation in the domain of RI
- CEMLINplus is a Research and Innovation Action (RIA), following INFRASUPP-01-2018-2019
- Project duration: 4 years, 01.02.2020-31.01.2024
- **Budget: 25 million EUR**
- **Consortium: 35 partners**
- Building on "First CREMLIN Recommendations"
- Coordinator: DESY

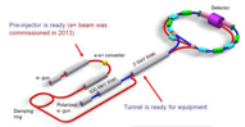
Collaboration with NICA	FAIR & JINR INR RAS; MEPhI; EKUT; NPI CAS; Wigner RCP; WUT
Collaboration with PIK	FZJ & NRC KI-PNPI JINR; PTI; SPSU; HZG; TUM; CEA-LLB; ILL; UCA; MTA EK; UNIMIB; ESS
Collaboration with USSR	NRC KI & ESRF DESY; European XFEL; INFN
Joint technology development around SCT and future lepton colliders	BINP & CERN JLU; CNRS-LAL; INFN
Joint technology development around XCELS	IAP & CEA-LIDYL ELI-DC AISBL; Laserlab-Europe AISBL
Joint development of detector technologies	FAIR & JINR DESY; BINP; NRC KI-PNPI; GUF; CNRS-IPHC; UNIMIB; CERN; ESS; INR NASU
Access to Russian RI	ICISTE & DESY NRC KI; NUST MISIS
Staff exchange and training for RI management	UNIMIB & NUST MISIS DESY
Joint long-term sustainability of RIs	NRC KI & DESY

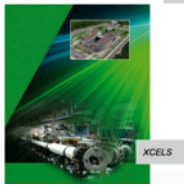
5 Russian megascience projects

- **NICA**: Superconducting accelerator complex („Nuclotron-based ion collider facility"); Dubna
- **PIK**: High-flux research reactor (International Centre for Neutron Research, ICNR); Gatchina
- **USSR**: Ultima Synchrotron Storage Ring; Protvino
- **SCT**: Lepton Collider „Super Charm-Tau Factory"; Novosibirsk
- **XCELS**: High power laser „Exawatt Center for Extreme Light Studies"; Nizhniy Novgorod


USSR sketch, NRC KI

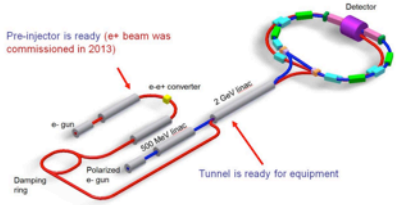

PIK


SCT sketch


XCELS

WP5 Joint technology development around SCT and future lepton colliders

- **Consortium** BINP & CERN (coordinating partners); and JLU; CNRS_LAL; INFN
- **Budget** 2.19 MEUR
- **Objectives**:
  - support and develop EU and Russian scientific cooperation in the SCT project
  - make an example of good practice on establishing collaboration around Russian RI with extensive participation of EU institutions
  - support joint EU - Russian efforts on development of future lepton colliders
  - increase visibility of SCT project in EU and world-wide scientific and decision-makers communities



CREMLIN PLUS

Connecting Russian and European Measures for Large-scale Research Infrastructures

CREMLINplus Kick-off Workshop

19-20 February 2020
DESY,
Notkestrasse 85, 22607 Hamburg

WP5: Joint technology development around SCT and future lepton colliders

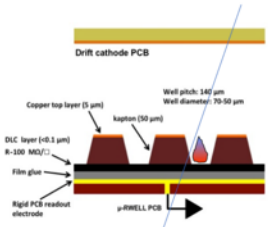
Vitaly Vorobyev
for the WP5 partners

WP5 Tasks

1. Fostering internationalization and visibility of the SCT project, support of outreach activities related to SCT
2. Development of collider technologies and fostering synergy between SCT, CLIC, and FCC-ee collider projects
3. Development of software for the design of an SCT detector
4. Development and design of Inner Tracker for the SCT detector
5. Development and design of Central Tracker for the SCT detector
6. Development and design of Particle Identification system for the SCT detector

Task 5.4 Development and design of Inner Tracker for the SCT detector

- Three options for the SCT inner tracker
  1. Si strips
     - Robust technology, but not optimized for low-momentum tracks
  2. Cylindrical μ-RWELL (INFN LNF & Ferrara)
     - Low material
     - Spatial resolution better than 60 μm
     - Time resolution ~5.7 ns
  3. TPC (BINP)
     - Best capability for low-momentum track detection
     - But challenging readout and reconstruction



D5.4 M24. Status report on R&D work on Inner Tracker for the SCT detector
D5.5 M44. Final report on R&D work on Inner Tracker for the SCT detector
Milestone. M42. Prototype for the SCT inner tracker based on the C-RWELL or Compact TPC

Task 5.5 Development and design of Central Tracker for the SCT detector

- An ultra-low mass Tracking Chamber with Particle Identification capabilities (TraPId) concept (INFN Lecce)
  - Low material
  - Improved identification with cluster counting
  - Synergy with MEG2 DC and the IDEA DC project for FCC-ee and CEPC
  - New drift chamber for the CMD3 detector as a prototype for the SCT central tracker

D5.6 M24. Status report on R&D work on Central Tracker for the SCT detector
D5.7 M44. Final report on R&D work on Central Tracker for the SCT detector
Milestone. M42. Prototype for the SCT central chamber

CREMLIN PLUS

Connecting Russian and European Measures for Large-scale Research Infrastructures

CREMLINplus Kick-off Workshop

19-20 February 2020
DESY,
Notkestrasse 85, 22607 Hamburg

Task	Subtask	Subtask leader	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12
5.1. Internationalization and visibility	Plenary talk on SCT at CHARM20	Vitaly Vorobyev												
	Workshop on future SCT factories	Vitaly Vorobyev												
	Public SCT webpage development	TBD												
5.2. Collider technologies	TBD													
5.3. SCT detector software	Full detector geomentry in DD4Hep (barrel)	Andrey Sukharev												
	Full detector geomentry in DD4Hep	Andrey Sukharev												
	Simplified reconstruction algorithm for each subsystem	Andrey Sukharev												
	Full simulation and reconstruction of TPC as inner tracker	Andre Sailer												
	CVMFS repository at CERN	Andre Sailer												
5.4. Inner tracker	Technical Design of TPC prototype	Lev Shekhtman												
	Technical design of cylindrical muRWELL prototype	Giovanni Benchivenni												
5.5. Central tracker	Conceptual design of the prototype	Franco Grancagnolo												
	Mechanical design of the prototype	Alessandro Miccoli, Alexander Popov												
	Simulation of the prototype	Fedor Ignatov												
	Study of the wire properties	Alexander Popov												
5.6. Particle identification	PID requirements for endcup and barrel from physics													
	Optimized conceptual design of the PID system	Michael Dueren												
	Prototyping FARICH option (full ring detect)	Alexander Barnyakov												
	Prototyping FDIRC option with SiPM readout (?)	Michael Dueren												
	Beam tests of existing prototypes (both options) (?)	Alexander Barnyakov												