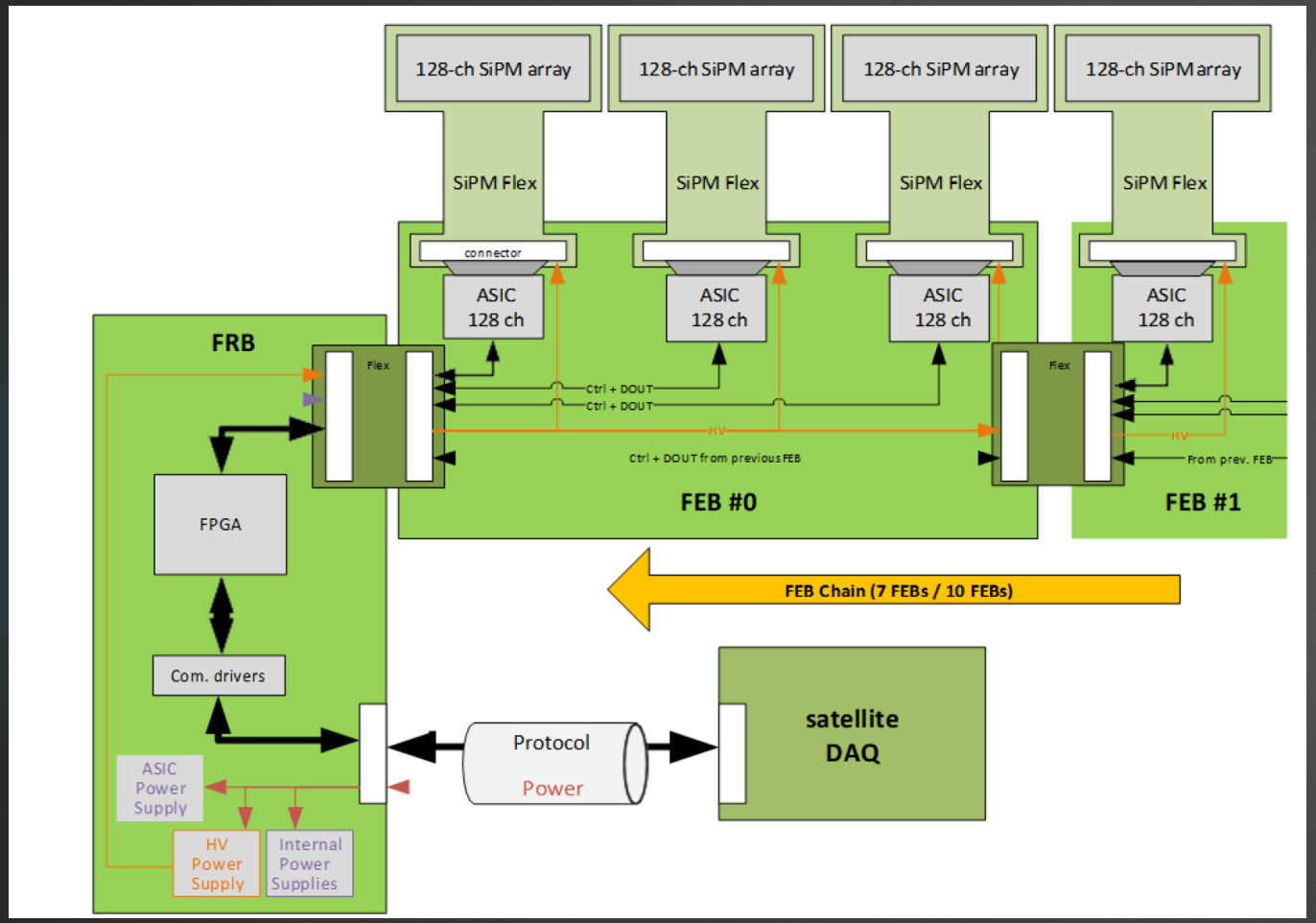
HERD-β (BETA) ASIC for FIT

- Project founded @ UNIGE in 2018 - PRODEX



A FEB equipped with 3 128 ch ASICs is connected through 3 flex cables to 3 SiPM arrays that read out one fiber mat. Up to 10 FEBs will be interconnected through flex cables. All 10 FEBs will then be read out by one FRB board, connected to FEB#0 through a dedicated flex cable.

The power budget for the FEB part of the FIT-Side is ~100W, which leads to a specification of power consumption for the ASIC at <0.5mW/channel, with a target at **0.3mW/channel**

FEB ASIC

the FEB ASIC stringent requirements in:

- Power consumption below 0.3 mW/ch
- High dynamic range as the chip must perform charge measurements up to Z=26 (equivalent ~700x of Minimum Ionizing Particle (MIP) energy deposition).
- Integration and density: analogue front end, ADCs and digital back-end must be integrated with very high channel density and minimal IO (input/output) overhead.

Since the main purpose of the chip are tracking (MIP) and charge measurement, the key parameters are noise and dynamic range. The requirement on the rise time is less stringent, because the event rate is below 1 kHz, thus, shaping time will be about **1-20 µs**.

PSD???

Should be ready for B Phase - 2020.02 - 2021.06

Specification	Target
Channels	64 or 128
Input rate	~1 kHz
Power consumption	Target: 0.3mW/ch
Radiation Hardness	80 Gray
Dynamic Range	676 MIP (18748 pe/ch) or 12 bits
Minimum detectable charge	0.1 MIP (or 2 pe/ch)
On chip digitization and zero suppression	1 single serial output
Slow control	SPI

Table 1. FIT ASIC specification

Block diagram

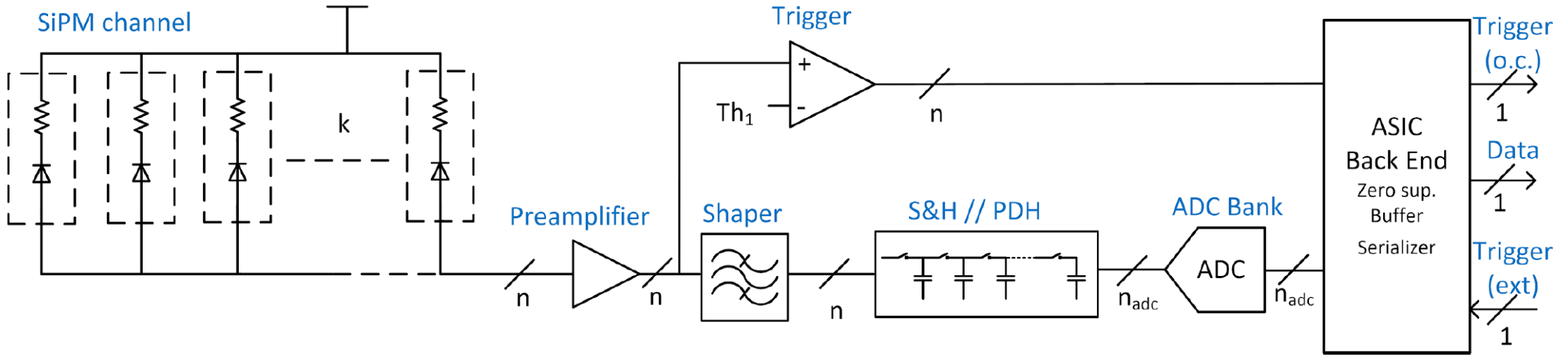


Figure 5. Preliminary block diagram of the HERD's FIT ASIC.

The ASIC reads n (64 or 128, to be studied) channels of the SiPM array. A preamplifier is followed by a tuneable shaper. The preamplifier will probably be based on a **dynamic gain switching architecture** to cover the full dynamic range with a single path and thus to minimize power consumption. **The shaper will be tunable** to compensate for potential signal shape variation due to radiation damage in the sensors or the fibres.

After shaping, a Sample and Hold (S&H) or Peak Detector and Hold (PDH) circuit will sample the signal. A bank of n_{adc} ADCs (with $n<n_{adc}$) will digitize the signal.

- The Preamplifier
  - The preamplifier to be used in this design should have as small power consumption as possible. It is also desired that it has low input impedance to avoid modification on the signal shape. As a convention 50Ω should be desirable since it may be coupled to the transmission line impedance in the printed circuit boards. Different low power Charge Sampling Amplifiers (CSA) or even just a termination resistor of higher value should be studied to obtain the desired noise performance.
  - **The bandwidth requirement for the preamplifier should be quite low since the shaper will be quite slow, but also the overall power consumption with less than 100µW. ---- for PSD should be different**
- SiPM voltage adjustment
  - The SiPM overvoltage should be tunable channel by channel to cope with manufacturing variations. Even if this is expected to be a second order effect on data output, the option should be possible in the electronics. A desirable range of at least 1V variation in the DC level at the SiPM connection should be foreseen. Input voltage control range 500 mV should be ok but 1 V may be need to control temp variations (several SiPMs controlled by the same power supply).

- To cope with the different ranges needed for the electronics (1 MIP signal for calibration and 700 MIP) a dual gain input stage will be designed.
- **Shaper**
  - The main purpose of the shaper is to provide a slow stable signal with reduced noise to the ADC. For this reason a configurable slow shaper (around ~10μs peaking time, 1-20) should be designed.
  - The GBW of the designed OTA would be 500kHz to 100kHz. A pedestal feedback circuit should be used to have a stable pedestal between channels.
- **ADC**
  - ADC will be included in less granularity than the number of channels. The main goal is to reduce the power consumption by adjusting the number of ADCs needed for the expected occupancy of the detector. ---- **this cannot be done for PSD**
  - Using a 12 bit resolution ADC, at high gain, assuming an LSB of 0.1 pe, and 10 ADC for 1 pe, the effective dynamic range would be (4096 - PED)/10 = 400 which can cover up to Z = 5. The large abundance of Z=4 allows for cross calibration between high gain and low gain. At low gain, it would be useful to see the separate Z-peaks from Z=1 on. Assuming 1 LSB is 0.25MIP i.e. 2 pe, a 12 bit ADC allows a dynamic range of 4096x2 = 8192 pe. The readout channel will have 13 bits: 12 for ADC and 1 for range.

- We need to contact all the collogue involved to ask them if they can help us in the design of the ASIC for PSD
- We need to define a set of parameter as soon as possible