HERD - fi**B**re track**E**r readou**T** **A**sic **(BETA)**

Specifications document

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1. Introduction

This document is devoted to summarize the basic specifications desired for the fi**B**re track**E**r readou**T** **A**sic (**BETA**) to be used in the **H**igh **E**nergy cosmic-**R**adiation **D**etection **FI**bre **T**racker (**HERD-FIT**). It is expected to be a constantly evolving document with the updates relevant on the experimental outcome during the design phase.

1.1. HERD

1.1.1. Present and future of high energy cosmic rays and gamma rays detection

A century after the discovery of cosmic rays, we are still a long way from answering fundamental questions about their nature, because of the daunting challenge to disentangle many unknown initial and boundary conditions by studying only particles reaching the Earth. Nevertheless, important progress has been made thanks to the complementarity between the indirect detection performed by large ground-based experiments, such as AUGER, IceCube, HESS/MAGIC, and the direct detection performed by space-borne missions, such as PAMELA, FERMI, AMS, and DAMPE.

Several unexpected features in the flux of cosmic ray electrons, protons and light ions have been observed recently by the AMS-02 [1] and DAMPE [2] missions, which could indicate either Dark Matter annihilation or nearby sources, or some missing pieces in the current cosmic ray acceleration and propagation models. Following these observations, a big next step forward is to advance in the energy frontier of direct cosmic ray detection towards the “knee” region (~1 PeV), with a detector able to measure electrons, photons and nuclei with excellent energy resolution and large acceptance (~1 m^2sr).

So far, very high energy cosmic rays have only been measured by ground-based air shower detectors, which suffer from large systematic uncertainties. On the other hand, space-borne experiments can measure flux and composition of primary cosmic rays with high accuracy but the energy range to which they are sensitive is limited by the size of the payload that can be deployed. At present, there are very few individual flux measurements around the “knee” region, but it is precisely in this region that interesting features in the total flux are being observed by ground-based experiments [3]. Therefore, *a new space instrument with ~10 times larger acceptance compared to the current generation of missions is needed to measure precisely the spectrum and the elemental composition, more specifically, to achieve more than 1 m^2sr at 1 PeV*.

Several generations of wide field of view (FOV) space gamma-ray telescopes in the GeV energy regime and ground based narrow FOV gamma-ray telescopes in hundreds of GeV energy regimes have discovered new populations of astrophysical objects, which allow a deeper understanding of the laws of nature under extreme physical conditions only available in these cosmic laboratories. In particular, wide FOV space gamma-ray telescopes often provide crucial guidance to the observations of the ground-based narrow FOV telescopes. Unfortunately, the much more powerful ground-based Cherenkov Telescope Array (CTA), currently under development, may not have the needed guidance from a space wide FOV gamma-ray telescope, once the FERMI satellite will stop its operations. *A new wide FOV space gamma-ray telescope is urgently needed to replace FERMI. The all-sky monitoring of high energy gamma-ray sources, either persistent or transient, in space is crucial in the era of the multi-messenger and multi-wavelength astronomy*, as has been demonstrated by the recent detection by FERMI of the counterpart of the gravitational wave from a neutron star merger detected by LIGO.

1.1.2. The HERD space mission

In order to address the above major problems in fundamental physics and astrophysics, the High Energy cosmic-Radiation Detection (HERD) [4] facility has been proposed as one of several space astronomy payloads onboard the future China's Space Station (CSS), which is planned for operation starting around 2025 for about 10 years.

The scientific goals of HERD are:

1. *to search for signatures of the annihilation/decay products of dark matter particles in the energy spectra and anisotropy of high energy electrons from 10 GeV to 100 TeV and in the gamma-ray spectrum from 500 MeV to 100 TeV.*
2. *to measure precisely the energy spectra and composition of primary cosmic rays from 30 GeV up to PeV in order to determine the mechanism of the cosmic rays 'knee' structure.*
3. *to provide wide FOV monitoring of the high energy gamma-ray sky from 500 MeV for gamma-ray bursts, active galactic nuclei, and Galactic gamma-ray binaries and microquasars.*

HERD (Figure 1) aims at achieving the ambitious goal of performing cosmic ray measurements with >3 m^2sr acceptance for electrons and >2 m^2sr acceptance. It will also be an excellent detector to search for Dark Matter using electrons and photons at high energy (TeV and above). *These features make HERD mission unique, competition does not exist as there is no other planned or approved experiment with comparable scientific capabilities in the foreseeable future.*

In the baseline design [5], HERD is composed of a deep 3-D cubic imaging calorimeter (CALO) made of LYSO crystals with an innovative design that ensures the same accuracy in the energy measurement and e/p separation for particles entering the detector from five out of the six sides. The CALO top side (zenith oriented) and its four lateral sides are instrumented with micro-strip silicon trackers (STKs) to reconstruct the direction of the impinging particles and measure their charge. The whole instrument is surrounded by a plastic scintillator detector (PSD), providing gamma-rays and charged particle triggers, as well as redundant charge measurement. A Transition Radiation Detector (TRD), located on one of the lateral sides, is used for the energy calibration of TeV nuclei. The total weight of the HERD payload is about 4 tons, within a dimension envelope of 2.3 x 2.3 x 2.6 m^3.

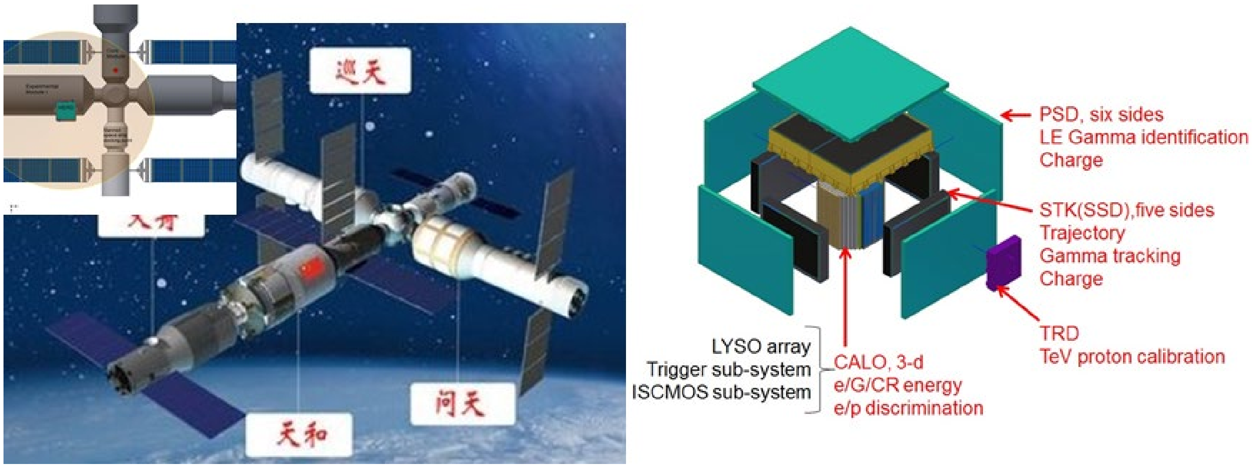

Figure 1. The HERD detector onboard the “Experiment module I” of the Chinese Space Station (left). Sketch of the HERD detector (right).

Besides the baseline design, different technical approaches are developed, such as the FIber Tracker (FIT) and the Tracker In Calorimeter (TIC) techniques, that could be used to further optimise the HERD performances. The final layout of the instrument will be defined after a deep detailed analysis of the detector performances and mission constraints [4].

1.1.4. International collaboration and status of the project

An international scientific collaboration is growing around the HERD initiative. Besides the involvement of Chinese institutions, led by CSU and IHEP, researchers from several European institutes have expressed significant interest and provided scientific contributions to the project. They include researchers from Italy (Universities and INFN of Bari, Florence, Lecce, Pisa/Siena, Pavia, Perugia and Gran Sasso Science Institute), Spain (CIEMAT Madrid) and Switzerland (University of Geneva).

On May 11th 2018, the HERD proposal [4] was presented to an evaluation panel designated by the Italian (ASI) and China (CMSA / CSU) space agencies. The recommendation of the evaluation panel was the immediate approval of the mission by the agencies and that the formed consortium remained open to interested international institutions. As said above, there is no other planned or proposed space mission that can fulfil HERD’s scientific goals, nor in indirect DM searches nor as wide field of view high energy gamma ray observatory. NASA’s AMEGO mission is not yet approved and targets the MeV range. Although the activities on prototypes and test with beam have already started, HERD is assumed to be officially adopted in 2018 (official agreement between CSU and ASI is expected before the end of the year). The expected launch time is 2025, and considering the complexity of the payload development and construction and the CERN availability of beam test the tentative project schedule is the following:

● Phase A, 2018.09 - 2020.02 (18 months). Prototypes of instruments are built, and main performances are verified. Key technologies of instruments are defined.

● Phase B, 2020.02 - 2021.06 (16 months). Development of Structural-Thermal model and Engineering/electrical model is completed.

● Phase C, 2021.06 - 2022.10 (16 months). Development of Qualification model is completed and calibration tests using CERN beams are implemented.

● Phase D, 2022.10 - 2024.10 (24 months). Flight Models are constructed and calibration tests using CERN beams are completed.

1.2. Scintillating Fiber Tracker (FIT)

For the lateral micro-strip silicon trackers (STK), the requirement of a full acceptance puts very stringent constraints on the placement of front-end and readout electronics. *For this reason, a scintillating fiber tracker (FIT) provides a very interesting alternative to a silicon microstrip tracker since fiber mats can be easily adapted to the needed geometry*. A tracker based on scintillating fiber technology enables to save weight, as the detector itself is lighter. As no wire bonds are used, the space between two support trays can be reduced. The support trays can also be thinner. It is estimated that in the space occupied by four silicon tracker trays, five FIT trays could be mounted. Since a FIT module is less complex than a microstrip detector module, production and integration times are expected to be shorter. A FIT ladder (Fig. 2, left) is a 6-layer scintillating fiber mat, of 1060 mm or 770 mm length. The fiber diameter is 0.25 mm. End pieces are mounted on both ends of the fiber mat for the optical connection to 3 SiPM arrays mounted on special PCBs with flex cable (SiPM Flex). The SiPM arrays are the same or similar as those used for the final version of the fiber tracker of the LHCb experiment at CERN (SciFi).

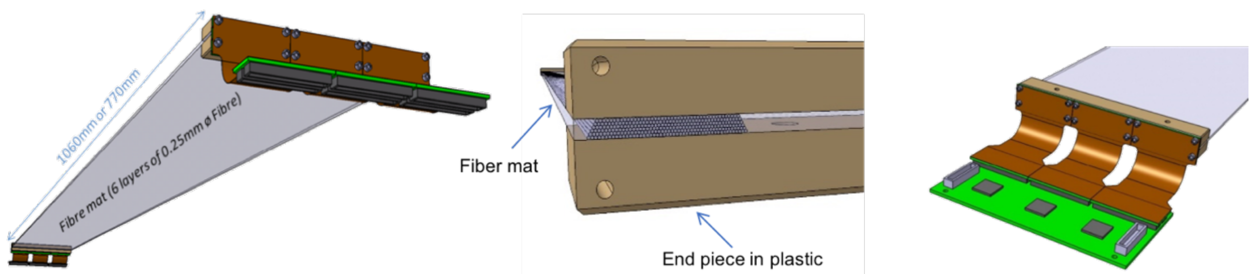

Figure 2. Sketch of a FIT ladder (left). Drawing of the details of the end of a fiber mat with the end piece, before the mounting of the SiPM flex (middle). Detail on the connection between the SiPMs, mounted on the ladder end piece, and connected through flex cables to the front-end electronics (FEB) board (right).

The 100 cm long fiber module has been installed in the center of a beam telescope composed with five AMS-02 silicon micro-strip ladders and the whole set-up mounted for a beam test at CERN. The computed spatial resolution is 65 μm, which is better than the requirement for HERD. However, the readout is based on commercial ASICs (VATA HDR64) with much higher power consumption than the < 0.5 mW/ch required for HERD. In summary, a FIT HERD prototype exists and would improve the performance of the tracker system with respect to STK, but a new and dedicated FE ASIC is required for the FIT to become viable.

The University of Geneva (UNIGE) group is a founding member of the HERD international collaboration established in October 2012 and is the group proposing the FIT tracker. Indeed, the UNIGE group has submitted a funding proposal for the Phase B of FIT tracker to PRODEX programme (http://sci.esa.int/prodex/) through the State Secretariat for Education, Research and Innovation SERI Swiss Space Office. The proposal has been approved and thus the execution of the phase B for FIT is granted. As discussed above, the only key element missing for FIT phase B is a dedicated ASIC. Considering the strong synergies between HERD FIT tracker and LHCb SciFi tracker, the UNIGE contacted the ICCUB to propose the development of the FE ASIC for FIT based on the know-how accumulated with several projects: the PACIFIC chip [6] for LHCb SciFi as well as other FE electronics for PMT and SiPM readout (7] to [11]).

1.2.1. FIT Geometry

The FIT Side Tracker (**FIT-Side**) has four sides, or 4 Tracker Sectors (**TS**). Current mechanical design allows up to 9 Tracker Planes (**TP**) on each TS, for a total of **36 TP** for the FIT-Side. Each TP consists of 2 Tracker Layers (**TL**): one (z-TL) for the z coordinate and another (x-TL) for the x/y coordinate. A z-TL has 5 long (1m) Tracker Modules (**z-TM**), while an x-TL has 10 short (0.7m) Tracker Modules (x-TM). Each TM is readout by three 128-channel SiPM MPPC S13552-10, for a total of 384 channels. The SiPM and ASICs are integrated on the Front-End Board (FEB).

In summary:

- Each TP has 17 TM, 51 SiPM and 6528 channels.
- Each TS has 153 TM/FEB, 459 SiPM and 58752 channels.
- The full 9-plane FIT-SC has 612 TM/FEB, 1836 SiPM and 234008 channels.

2. HERD-β (BETA) ASIC

The basic concept and components of a scintillating fiber tracker have already been tested. The most important parameter for a tracker, the position resolution, has been measured to be ~65 μm, with proton beams at CERN with fiber tracker prototypes produced by the UNIGE group, well within the required position resolution of 75 μm. However large fiber trackers have never been used in space. The assembly of fiber mat with SiPM needs therefore to be qualified for space application, in particular in view of the resistance to the required vibration, shock and thermal-vacuum conditions. These tasks will be carried out by UNIGE and the funding for phase A and B is secured thanks to an application approved by PRODEX in 2018.

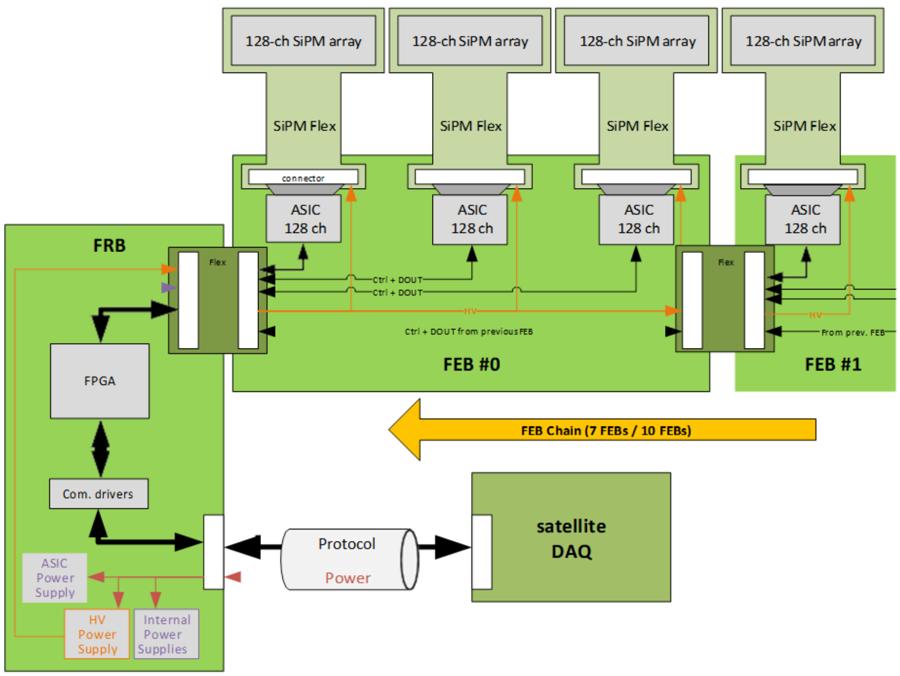

Figure 3 (from UNIGE PRODEX proposal): Architecture of the FIT data read-out chain. A FEB equipped with 3 128 ch ASICs is connected through 3 flex cables to 3 SiPM arrays that read out one fiber mat. Up to 10 FEBs will be interconnected through flex cables. All 10 FEBs will then be read out by one FRB board, connected to FEB#0 through a dedicated flex cable.

Furthermore, the front-end electronics used for the test beam is far from final in terms of power consumption, lack of some special functionalities and density. The front-end read-out system development includes the design and production of a space qualified multilayer rigid-flex circuit board, the SiPM Flex, which houses a SiPM, a bias filter circuit, a temperature sensor and a space qualified high density connector (Figure 3).

Strict mechanical constraints require a precise alignment of the SiPM on the support circuit. Another part of this activity is the front-end electronics board (FEB) to which the SiPM Flex will be connected.

The detector signal amplification and digitization will be done by dedicated ASICs. The bare dice ASICs will be directly mounted on the board to save space and thus wire bonding will be necessary.

The power budget for the FEB part of the FIT-Side is ~100W, which leads to a specification of power consumption for the ASIC at <0.5mW/channel, with a target at **0.3mW/channel** to leave room for adding more layers or using fibers for the top tracker.

The key element missing in this picture is the FEB ASIC as no existing device match the stringent requirements in:

- Power consumption below 0.3 mW/ch
- High dynamic range as the chip must perform charge measurements up to Z=26 (equivalent ~700x of Minimum Ionizing Particle (MIP) energy deposition).
- Integration and density: analogue front end, ADCs and digital back-end must be integrated with very high channel density and minimal IO (input/output) overhead.

Such ASIC should become available for the phase B of the project. This development will be based on the previous know-how of the research team in the development of different ASICs for SiPM readout: the PACIFIC chip [6] for the LHCb fiber tracker, the MUSIC chip [12] for the CTA project and the FlexToT chip family ([9], [10], [11]).

Since the main purpose of the chip are tracking (MIP) and charge measurement, the key parameters are noise and dynamic range. The requirement on the rise time is less stringent, because the event rate is below 1 kHz, thus, shaping time will be about 1-20 μs.

One challenging aspect of the design is to perform the signal processing with less than 0.3mW/ch. Note that, decreasing the power consumption, more tracking layers can be proposed to have a more robust tracker design and, as said above, with better acceptance for gamma rays.

The requirements for the FIT ASIC are summarized in table 1.

Specification	**Target**
Channels	64 or 128
Input rate	~1 kHz
Power consumption	Target: 0.3mW/ch
Radiation Hardness	80 Gray
Dynamic Range	676 MIP (18748 pe/ch) or 12 bits
Minimum detectable charge	0.1 MIP (or 2 pe/ch)
On chip digitization and zero suppression	1 single serial output
Slow control	SPI

Table 1. FIT ASIC specification

Another challenging aspect of the project is the high level of integration required. The digitization and the digital back-end must be integrated in the chip with a high number of channels (64 or 128 ch per chip). After zero-suppression all the channels must be multiplexed in a single output. With a single line output per ASIC, the FIT deadtime is determined by the serial readout element of the highest occupancy. Of the serial readout element has 64 channels, then the deadtime for a full occupancy event reading at 1MHz will be 64x13x1us = 831us, within the 1kHz trigger rate limit. It should be studied to use extra handshake signal and an independent clock line for the readout.

Digital circuitry will be protected against Single Event Errors (SEEs) and techniques to avoid Single Event Latchup (SEL) will be also adopted. Since this chip will be used in space, it must be radiation tolerant (at least at 80 Gray). A possible technology to develop this ASIC and to achieve these specifications can be the TSMC 130nm which is already qualified for higher radiation levels at CERN and it is used for the PACIFIC chip.

Figure 5 shows the preliminary block diagram of the HERD's FIT ASIC. The ASIC reads *n* (64 or 128, to be studied) channels of the SiPM array. A preamplifier is followed by a tuneable shaper. The preamplifier will probably be based on a dynamic gain switching architecture to cover the full dynamic range with a single path and thus to minimize power consumption. The shaper will be tuneable to compensate for potential signal shape variation due to radiation damage in the sensors or the fibres. After shaping, a Sample and Hold (S&H) or Peak Detector and Hold (PDH) circuit will sample the signal. A bank of n_{adc} ADCs (with $n<n_{adc}$) will digitize the signal. The size n_{adc} of the bank will be determined based on the analysis of the occupancy and the event rate of the system. Finally, the digital back-end will comprehend: the slow control interface, the state machine to control the conversion based on trigger signalling, the event buffer, the zero-suppression and the serialization to generate a single output data signal. Internal trigger should be validated with an external trigger signal. The chip only digitizes what is validated with external trigger. The internal trigger should be provided as open collector (o.c.) signal.

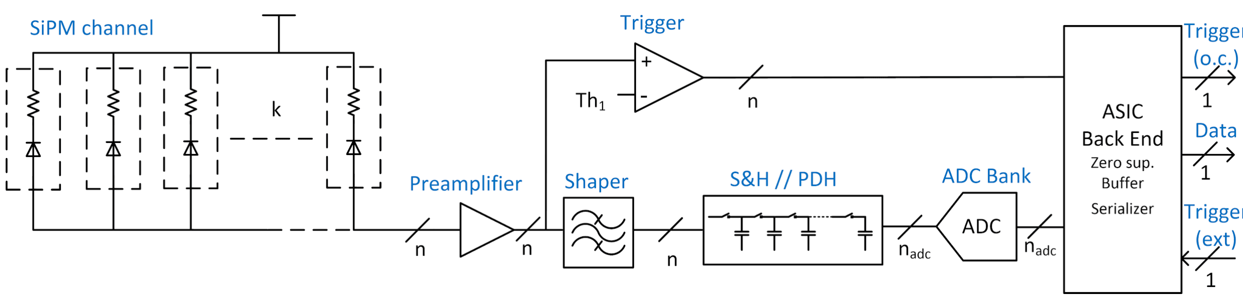

Figure 5. Preliminary block diagram of the HERD's FIT ASIC.

The traditional approach in tracking detectors is to use naked ASICs because of space limitation and wire-bonding them in house. This approach has been followed by UNIGE for previous space projects (AMS and DAMPE trackers). An alternative approach with even higher density would be to study new Chip Scale Package (CSP) or Flip-Chip solutions with even higher density than wire bonding.

2.1. Silicon Photomultiplier Array

The sensor baseline solution is the use of Silicon Photomultiplier Arrays, that can stand the temperature, mechanical stress and radiation levels. The initial solution is based on the SciFi detector ones. The already designed device for particle tracking is enough for single MIP measurements, but does not cope with the needed dynamic range and number of cells for high signal measurement and needed energy resolution. For this reason R&D is focusing on a version of the array with reduced cells size that should increase the current number of cells (104) to around 1750 (15x15µm) or 4000 (10x10µm) cells. This number of cells should be enough to cope with the full range as described in section 2.2.

2.1.1. SiPM model

In order to develop the HERD-**β** front end ASIC, an accurate model of the SiPM is needed. An overview is given in Figure 6. This model was chosen because of its simplicity and the possibility of inclusion in an analog circuit simulator (SPICE).

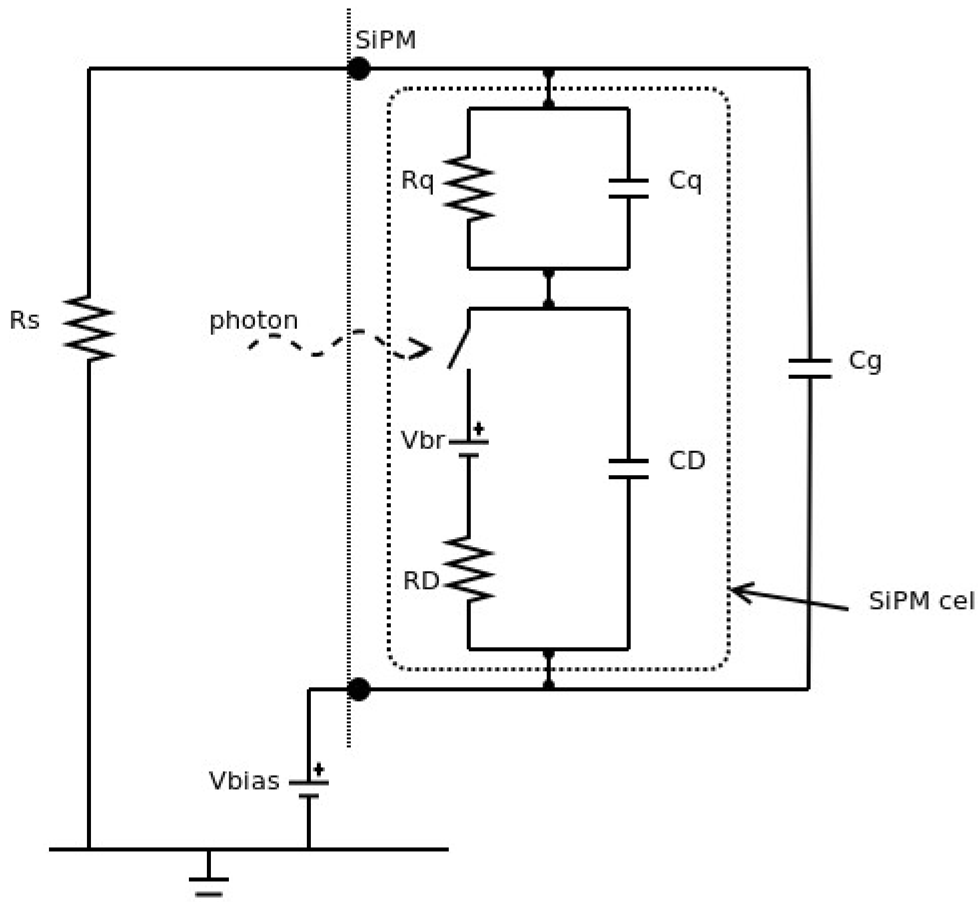

Figure 6. SiPM model used for simulation of incoming signal.

In this model *Cg* is the parasitic capacitance of the detector, *Cd* the capacitance of the reverse-biased diode, *Rd* is the resistance of the micro-plasma in avalanche, *Rq* the quanch resistor and *Cq* its associated stray capacitor. The equation that models the slow time constant of the SiPM can be obtained using the previous parameters as follows:

$$T_{SiPMslow} = Rq\ x\ (Cq + Cd)$$

On the other hand, the equation that models the fast time constant is:

$$T_{SiPMfast} = R_S\ x\ C_{tot} = R_S\ x\ ((C_d + C_q)\ x\ N\ +\ C_g)$$

where *N* is the number of SiPM cells. The value of *Rq, Cq, Vbr, Rd, Cd* and *Cg* can be extracted from experimental results and datasheet parameters. The switch on the model is closed when a photon is converted and opened when the value of the current which comes through drops below a defined current (I_q). V_{ov} corresponds to the voltage over breakdown voltage (V_{br}), thus V_{bias} is the sum of V_{br} and V_{ov}.

For the design of the ASIC the model parameters used are as summarized in table 2.

Parameter	**SciFi 2016HQR**	**HERD 10x10 µm**	**HERD 15x15 µm3749**
N	104	3749	1750
Cd	115fF	5.9fF	14.4fF
Cq	18fF	2.1fF	3.2fF
Rq	470kΩ	700kΩ	700kΩ
Cg	1pF	1.5pF	1.5pF
Vov	4V	5V	4V
Rd*	2kΩ	2kΩ	2kΩ
Iq*	25 µA	25 µA	25 µA

*Parameters used internally for the model control of the avalanche.

Table 2. SiPM model parameters

Using those parameters the devices can be simulated and compared to real measurements as seen in figure 7.

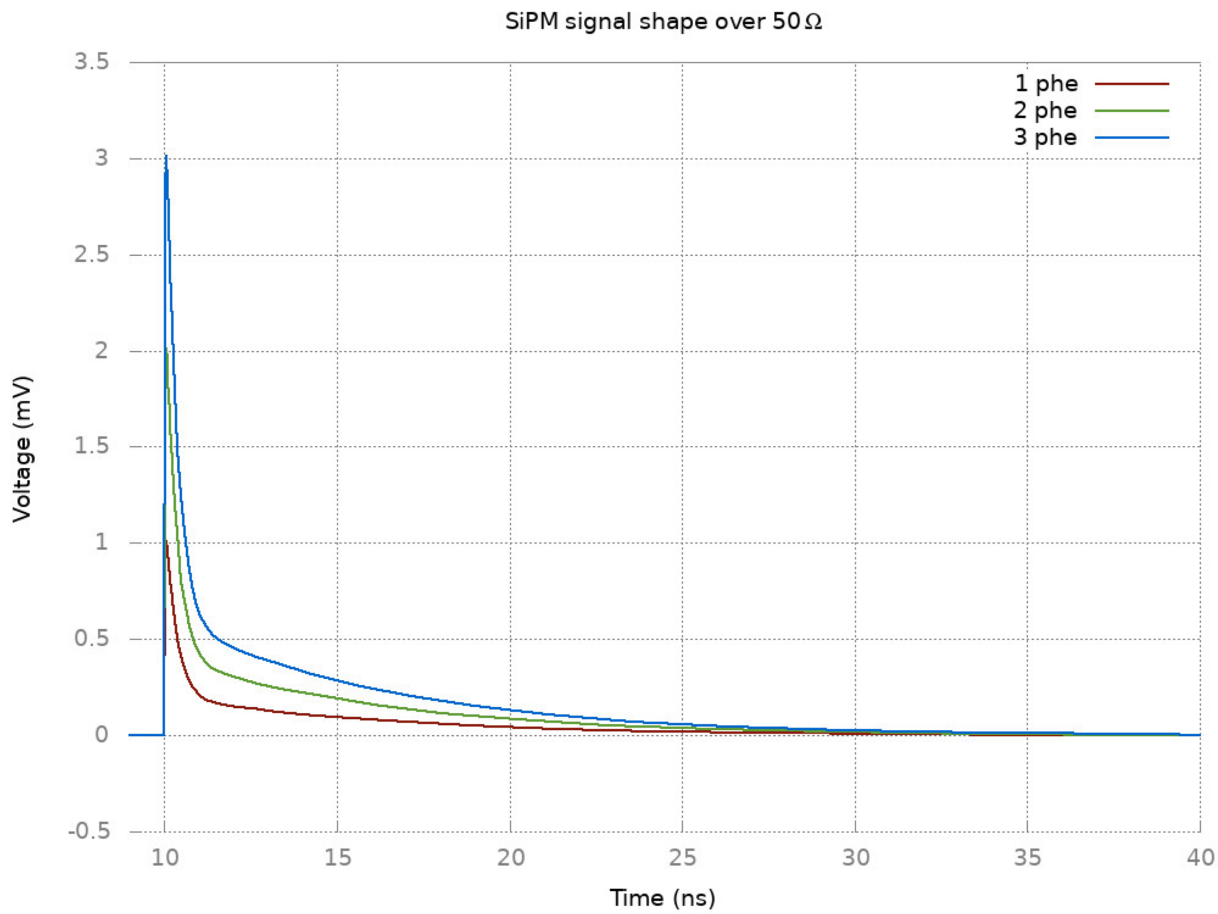

Figure 7. SiPM 1,2,3 cell simulation at 4V overvoltage

2.1.2. Measurements with SiPM S13552-10

With this SiPM it has been measured:

- An Average (Np*ε) of 12 phe for MIP proton clusters, vertical entrance, and Vov = 6.5V.
- 8 phe for MIP proton peak channel, vertical entrance.
- DCR: DCR_1pe/_2phe/_3phe = 60kHz/180Hz/0.6Hz at room temperature.

2.2. Dynamic range

SiPM offer a linear output depending on incident light in certain range of input photons. According to [13] the response of a SiPM can be extracted with the following equation, where *m* is the total number of cells of the device and ε is the photon detection efficiency (including geometrical factors).

$$N_{cellsfired} = m\,x\,\left(1 - e^{-\frac{N_{phe}\,x\,\varepsilon}{m}}\right)$$

In figure 8 there is a summary of the response of the SiPM depending on the incoming number of photons. The data for the 10x10μm cells version is extrapolated from the commercial S14160-1310PS device (with ε=18% only) and the 15x15μm cells device ((with ε=32%) from the S14160-1315PS device from Hamamatsu.

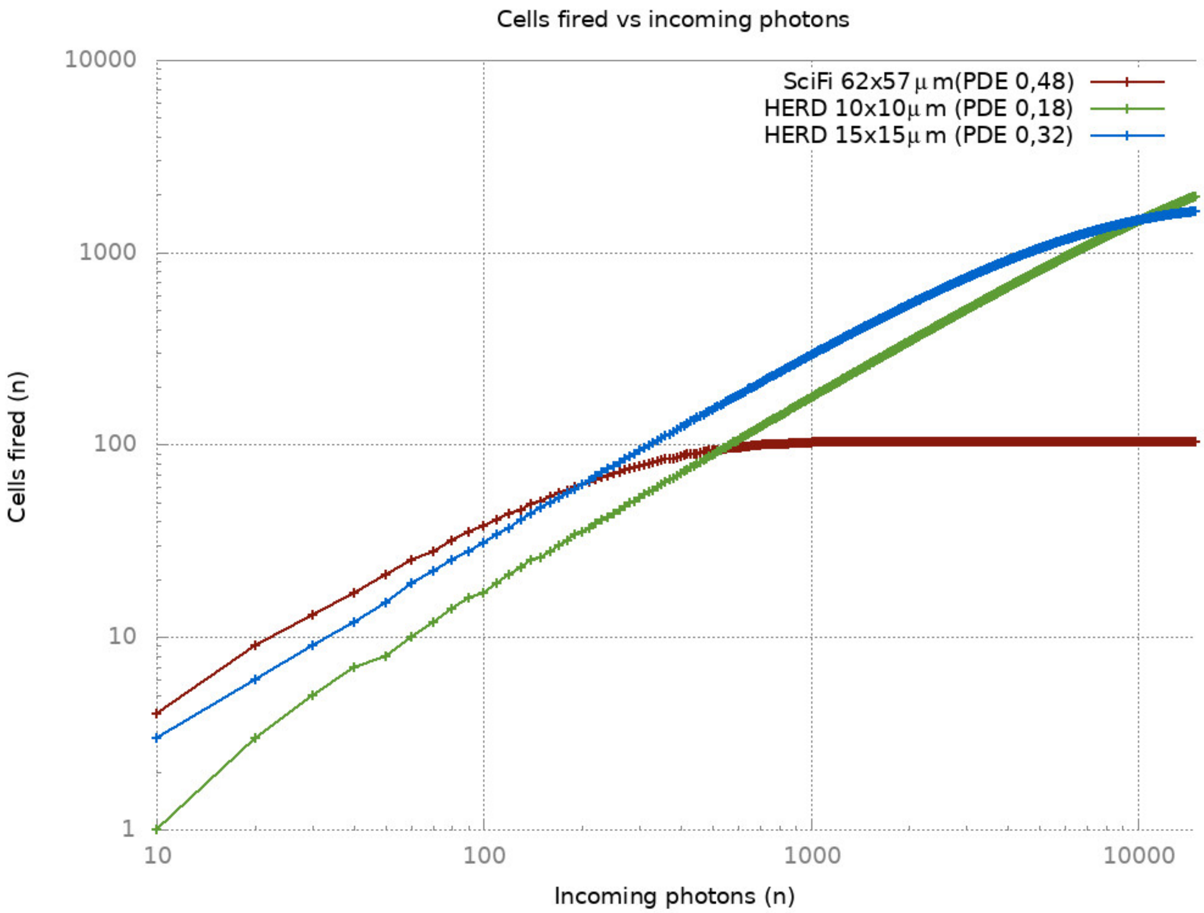

Figure 8. SiPM saturation depending on PDE and number of cells.

Assuming an (Np*ε) of 8 phe/MIP, simple scaling by Z^2 gives (NpFe*ε) =5408 (Z=26), but there are effects that will move the actual saturation point up and down:

- (Np*ε) = 8 phe/MIP is at vertical entrance, at 45º entrance (Np*ε) ~ 11 phe/MIP.
- The dE7dx distribution has a Gaussian distribution with a width proportional to Z. Assuming a 3 sigma width of fraction of event will have a NpFe*ε up to 30% higher, leading to 7030.
- The quenching effect of high Z will reduce the NpFe*ε to NpFe*ε*q (q = 0.6 for DAMPE PSD -> NpFe*ε*q = 4218).

- The photons from one fiber may leak out to neighboring fibers and the coupling of the SiPM will lead to leaks to neighboring channels (optical crosstalk effect).

Assuming all the effects above gives NpFe*ε = 5000 then:

$$N_{cellsfired} = 3749\ x\ \left(1 - e^{-\frac{5000}{3749}}\right) = 2761$$

Which is already about 74% of N, close to the saturation of the SiPM. Therefore 10 um SiPM should be the baseline solution.

The total dynamic of the electronics will be determined by the signal to noise ratio (SNR) and the total number of SiPM cells:

$$DR\ =\ SNR\ *\ N_{cells}$$

The SNR is defined as the signal of 1 firing cell divided by the total integrated noise. SNR for calibration is required to be > 10, whereas for operation > 5 (to set 3.5 threshold).
The input range of the electronics must accept the maximum SiPM signal (all cells firing). In case of 10 um, it corresponds to N_{cells}=3749. This leads to a dynamic range of 5*3749 = 18745.

2.3. Preamplifier

The preamplifier to be used in this design should have as small power consumption as possible. It is also desired that it has low input impedance to avoid modification on the signal shape. As a convention 50Ω should be desirable since it may be coupled to the transmission line impedance in the printed circuit boards. Different low power Charge Sampling Amplifiers (CSA) or even just a termination resistor of higher value should be studied to obtain the desired noise performance.

The bandwidth requirement for the preamplifier should be quite low since the shaper will be quite slow, but also the overall power consumption with less than 100μW.

2.3.1. SiPM voltage adjustment

The SiPM overvoltage should be tunable channel by channel to cope with manufacturing variations. Even if this is expected to be a second order effect on data output, the option should be possible in the electronics. A desirable range of at least 1V variation in the DC level at the SiPM connection should be foreseen. Input voltage control range 500 mV should be ok but 1 V may be need to control temp variations (several SiPMs controlled by the same power supply).

2.3.2. Dynamic gain change

To cope with the different ranges needed for the electronics (1 MIP signal for calibration and 700 MIP) a dual gain input stage will be designed. During normal operation of the device the gain change should be carried out dynamically without user intervention, but in special (calibration or debug) modes this gain may be fixed by slow control. The shared signal path (shaper, T&H and peak detector) should reduce the power consumption of the overall signal path.

2.4. Shaper

The main purpose of the shaper is to provide a slow stable signal with reduced noise to the ADC. For this reason a configurable slow shaper (around ~10µs peaking time, 1-20) should be designed. The DCR increase due to the radiation damage will limit the shaping time to avoid crossing the 2 pe threshold. As in the preamplifier the most challenging constrain will be the reduced power consumption (less than 100µW). The GBW of the designed OTA would be 500kHz to 100kHz. A pedestal feedback circuit should be used to have a stable pedestal between channels.

2.5. Rates: random and trigger

Typical external trigger is below 1 KHz. External trigger validates internal trigger and determines the conversion rate in normal operation.
However, it is important to take into account random internal trigger rate, fixed by the dark current rate and correlated noise of the sensor. Two factors should be considered:

1. The maximum shaping will be limited by the maximum channel internal trigger rate.
2. For calibration, a special trigger mode based on internal trigger might be useful. In this scenario the conversion rate might be not higher than 1 KHz.
3. In normal operation, the internal trigger threshold will be set around 3.5 cells. However, *if calibration down to single cell (finger plot) is performed much higher rates would be required.*

2.6. ADC

ADC will be included in less granularity than the number of channels. The main goal is to reduce the power consumption by adjusting the number of ADCs needed for the expected occupancy of the detector. Low power Successive Approximation (SAR) switched capacitor ADC is the baseline implementation due to its speed and low power.

Using a 12 bit resolution ADC, at high gain, assuming an LSB of 0.1 pe, and 10 ADC for 1 pe, the effective dynamic range would be (4096 - PED)/10 = 400 which can cover up to Z = 5. The large abundance of Z=4 allows for cross calibration between high gain and low gain. At low gain, it would be useful to see the separate Z-peaks from Z=1 on. Assuming 1 LSB is 0.25MIP, i.e. 2 pe, a 12 bit ADC allows a dynamic range of 4096x2 = 8192 pe. The readout channel will have 13 bits: 12 for ADC and 1 for range.

Since signal is expected to be shared amongst neighbour channels; a starting point should be to have three (3) DACs for every channels block of 16.

If possible, the ADC will be used to digitize the signal of external temp sensors (1 per ASIC).

2.7. Digital

2.7.1. Slow control

The slow control interface will be based on an SPI serial control running at a maximum speed of 100kHz. Due to the small power consumption requirements single ended communication is preferred. The distance between devices should be reduced to the maximum to avoid transmission errors. The different devices could be daisy chained with independent CS signals to reduce the number of signals.

Several programmable parameters and debug control signals will be managed by the slow control. In order to avoid unexpected behaviour during data taking, all static values (configuration parameters) will be protected by hamming encoding memories. The signal data path will not be protected against bit flips (single event upsets), since data can probably be used still even if one bit flip exists and the probability is assumed to be low enough at the system working frequency.

2.7.2. System clock

In order to reduce the switching power consumption of the standard cells blocks the clock speed of the device must be as reduced as possible. Moreover the ADC conversion time will be directly proportional to the clock period. For this reason an initial value will be **1MHz**.

2.7.3. Data output

The data delivered by the ADC will need to be validated by an external trigger enable signal. For debugging the option to mask this external signal should also be included. Data will only be transmitted after zero suppression (with a programmable level). Again single ended output is preferred against differential data transmission due to the reduced power consumption. For this reason the system clock used for data transmission must be kept at low frequency.

2.8. Floorplan

The final readout ASIC should be as much as possible fitting a square box to provide easier bonding to the printed circuit board. This means the input channels must be provided from both sides of the die (left and right), keeping the other two sides for data and control input output and power supplies.

The device will be based on a 16 channel structure including all the needed elements and **a number of ADCs to be defined** shared amongst this group of channels.

All common signals for biasing and common control of the channels will be routed crossing the channels from one side to the other and minimizing distance. All those signals should provide voltage references (not current) to avoid voltage drop with large paths. A general view of the design organization is depicted in figure 9.

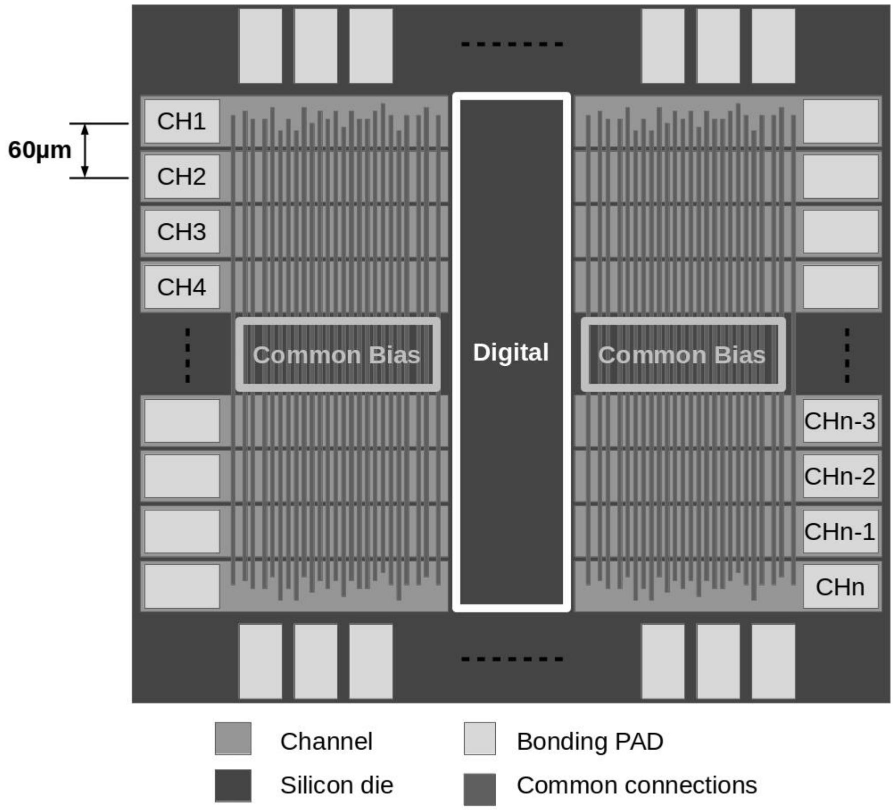

Figure 9. Temptative die organization for final ASIC.

2.8.1. Channel pitch

The main constraint to define the final die size and channel aspect ratio is the pitch between channels. This pitch is mainly driven by the wire bonding capabilities and is assumed to be **60µm** as a conservative and standard distance.

This pitch restricts the final device size, just counting the channels needed width the estimations on a rectangular design die are summarized in table 3. Those estimations assume the channel analog processing can be fitted in the width two times (in bigger prototypes) and also the ADCs and digital processing in the middle area.

	16 channels	**64 channels**	**128 channels**
Top - Bottom height	~ 300µm	~ 300µm	~ 300µm
Channels height	16x60µm = 960µm	32x60µm = 1920µm	64x60µm = 3840µm
Common Bias height	Side of channels	4x60µm = 240µm	4x60µm = 240µm
TOTAL size (square)	1300x1300µm	2500x2500µm	4400x4400µm

Table 3. Estimated design size for different number of channels prototypes.

3. References

[1] AMS Collaboration, Phys. Rev. Lett. 113, 121101 (2014), Phys. Rev. Lett. 114, 171103 (2015) and Phys. Rev. Lett. 115, 211101 (2015).

[2] DAMPE Collaboration, Direct detection of a TeV break in the cosmic ray e− + e+ spectrum, Nature, 552, 63-66 (2017).

[3] ARGO-YBJ Collaboration, LHAASO Collaboration, Phys. Rev. D. 92, 092005 (2015).

[4] The Joint Working Team for the HERD collaboration, "HERD proposal", https://indico.ihep.ac.cn/event/8164/material/1/0.pdf (2018)

[5] S. N. Zhang, O. Adriani, S. Albergo, et al. The High Energy cosmic-Radiation Detection (HERD) facility onboard China's Space Station. In Proc. SPIE, Space Telescopes and Instrumentation 2014: Ultraviolet to Gamma Ray, volume 9144, page 91440X, (2014).

[6] Gascon, D., Chanal, H., Comerma, A., Gomez, S., Han, X.., Mazorra, J., Mauricio, J., Pillet, N., Yengui, F., Vandaele, R., "PACIFIC: A 64-channel ASIC for scintillating fiber tracking in LHCb upgrade", Journal of Instrumentation, vol. 10, (2015).

[7] Gascon, D., Sanuy, A., Paredes, J.M., Ribó, M., Sieiro, J., "Wideband (500 MHz) 16 Bit Dynamic Range Current Mode Input Stage for Photodetector Readout", IEEE Nuclear Science Symposium and Medical Imaging Conference, Valencia, (2011).

[8] Gascon, D. et al., "Wideband pulse amplifier with 8 GHz GBW product in a 0.35 μm CMOS technology for the integrated camera of the Cherenkov Telescope Array", Journal of Instrumentation, vol. 5, (2010).

[9] A. Comerma, D. Gascon et al., "FlexToT - Current mode ASIC for readout of common cathode SiPM arrays," IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Seoul, pp. 1-2, (2013).

[10] J. Castilla, D. Gascon et al., "Evaluation of the FlexToT ASIC on the readout of SiPM matrices and scintillators for PET," IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Seoul, pp. 1-4, (2013).

[11] J. Trenado, D. Gascon et alt., "Performance of FlexToT Time Based PET Readout ASIC for Depth of Interaction Measurements", Proceedings of the 3rd International Conference on Technology and Instrumentation in Particle Physics (TIPP) (2014).

[12] S. Gomez, D. Gascon et alt. "MUSIC: An 8 channel readout ASIC for SiPM arrays", Proc. SPIE 9899, Optical Sensing and Detection IV, 98990G (2016).

[13] D. Dolgoshein, "Silicon Photomultipliers in particle physics: possibilities and limitations", Proc. of the 42nd Workshop of the INFN ELOISATRON Project (2003)