Silicon based sensors for Time-Of-Flight measurement

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Outline

- Introduction
- Classification of silicon detectors for timing
- Sensors with gain
- Integrated sensors without gain
- Work in progress and future perspectives
- Conclusion

Sensor timing resolution

Fundamental limit

Non saturated velocity and non-uniform weighting field

Can be made **negligible**

$$\sigma_{\mathrm{t}}^2 = \sigma_{\mathrm{Time\ Walk}}^2 + \sigma_{\mathrm{Landau\ Noise}}^2 + \sigma_{\mathrm{Distortion}}^2 + \sigma_{\mathrm{Jitter}}^2 + \sigma_{\mathrm{TDC}}^2$$

Can be **corrected** (e.g. with Constant Fraction Discriminator, CFD)

$$\sigma_{Jitter} \propto \frac{\sigma_V}{\frac{dV}{dt}}$$

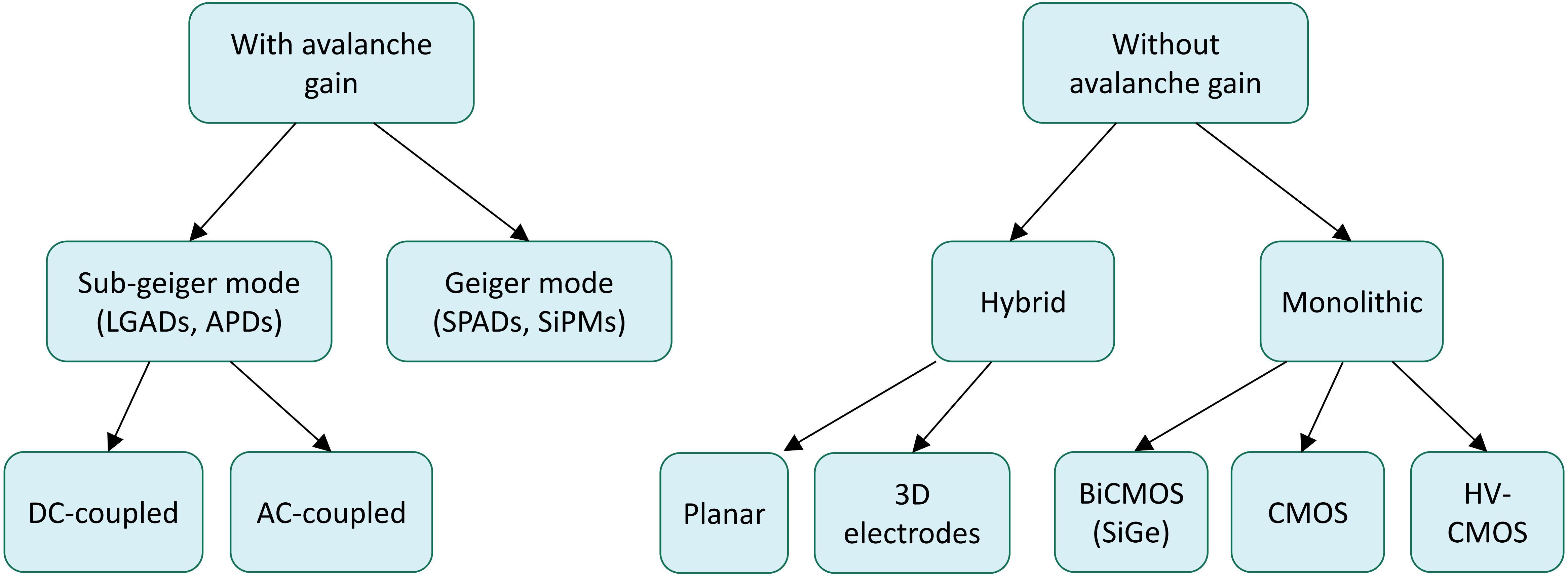
Low input capacitance,
High preamp. transconductance

Large signal (gain)

Short signal rise time

H. F.-W. Sadrozinski et al 2018 Rep. Prog. Phys. 81 026101

Detectors for ps timing: overview



With avalanche gain

Sub-geiger mode (LGADs, APDs)

DC-coupled

AC-coupled

Geiger mode (SPADs, SiPMs)

Without avalanche gain

Hybrid

Planar

3D electrodes

Monolithic

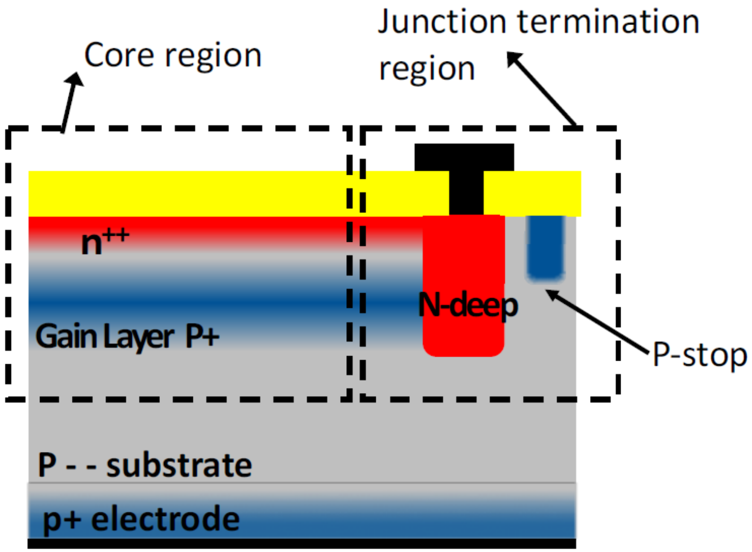
BiCMOS (SiGe)

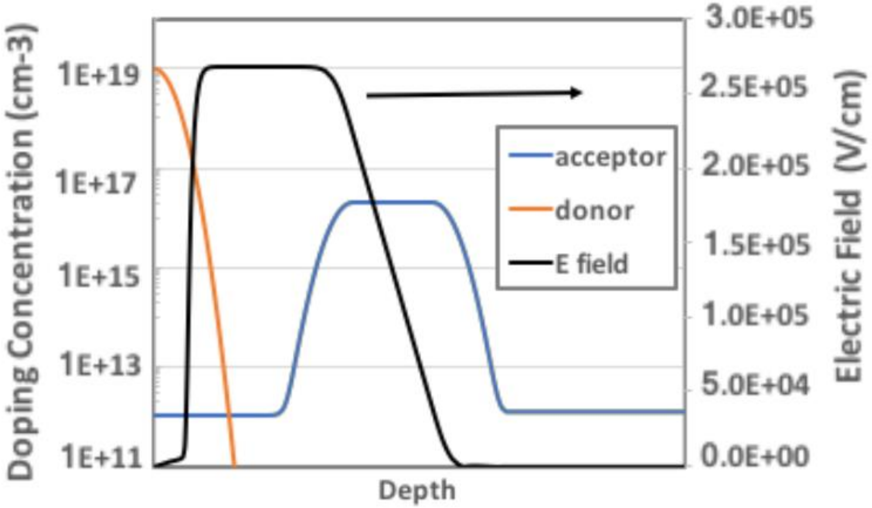
CMOS

HV-CMOS

LGADs: operation

- Avalanche multiplication: linear-mode (sub-Geiger) operation
- Separate absorption-multiplication region:
  - Fully depleted HR substrate or epitaxial layer
  - P+ gain layer: high electric field
- Gain area termination needed: dead (no gain) region between the pixels





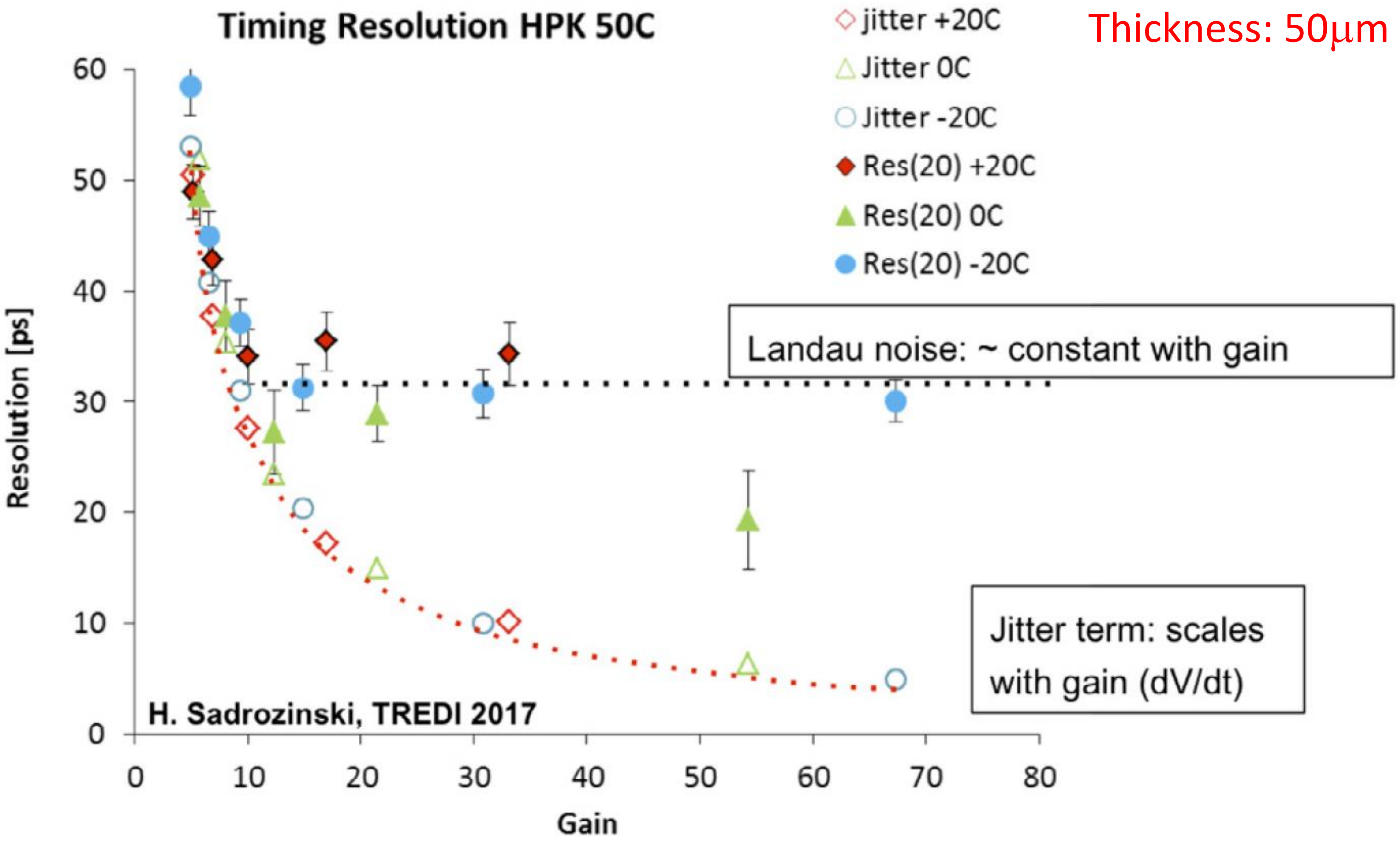
G. Paternoster et al., J. Instrum., vol. 12, no. 2, 2017, Art. no. C02077

LGADs: timing resolution

- Uniform electric field in a large area (~ mm^2): $\sigma_{\text{distortion}}$ is negligible

- The effect of electronics noise on timing resolution (σ_{jitter}) can be reduced by increasing the gain

- Fundamental limitation: **Landau noise**, due to fluctuations in the released charge



Thickness: 50μm

Landau noise: ~ constant with gain

Jitter term: scales with gain (dV/dt)

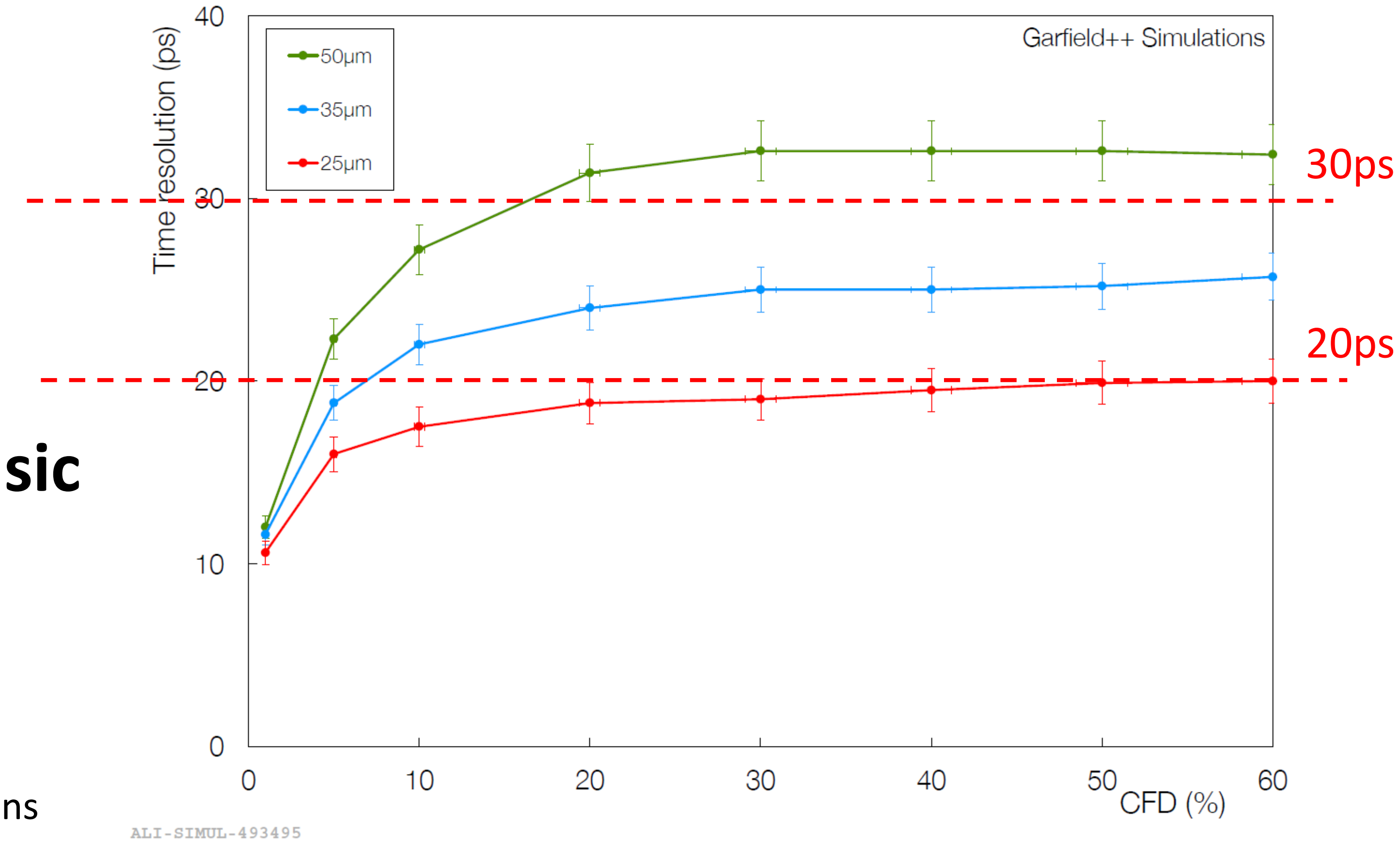
N. Cartiglia et al., NIM A 924 (2019) 350-354

How to go below 30ps with LGADs?

- Low threshold → practical limits in an array due to electronic noise, pixel non-uniformity and electrical cross-talk

- **Sensor thickness < 50µm**

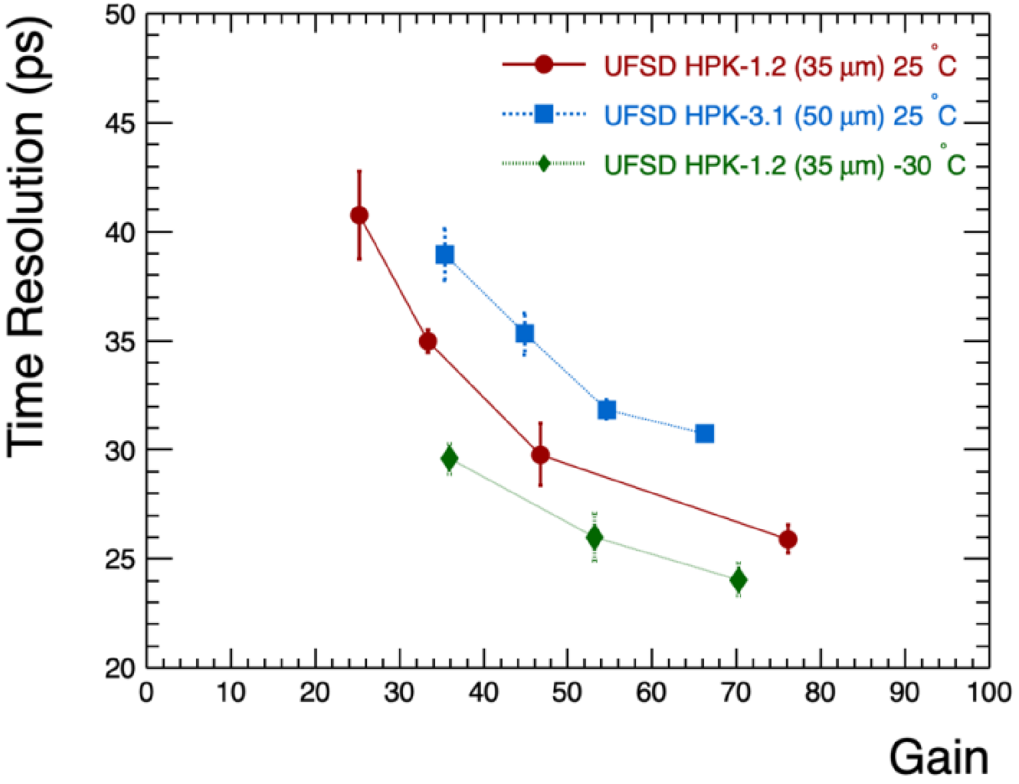
- Landau fluctuations: with 25um thickness the **intrinsic time resolution** for MIPs is ~20ps

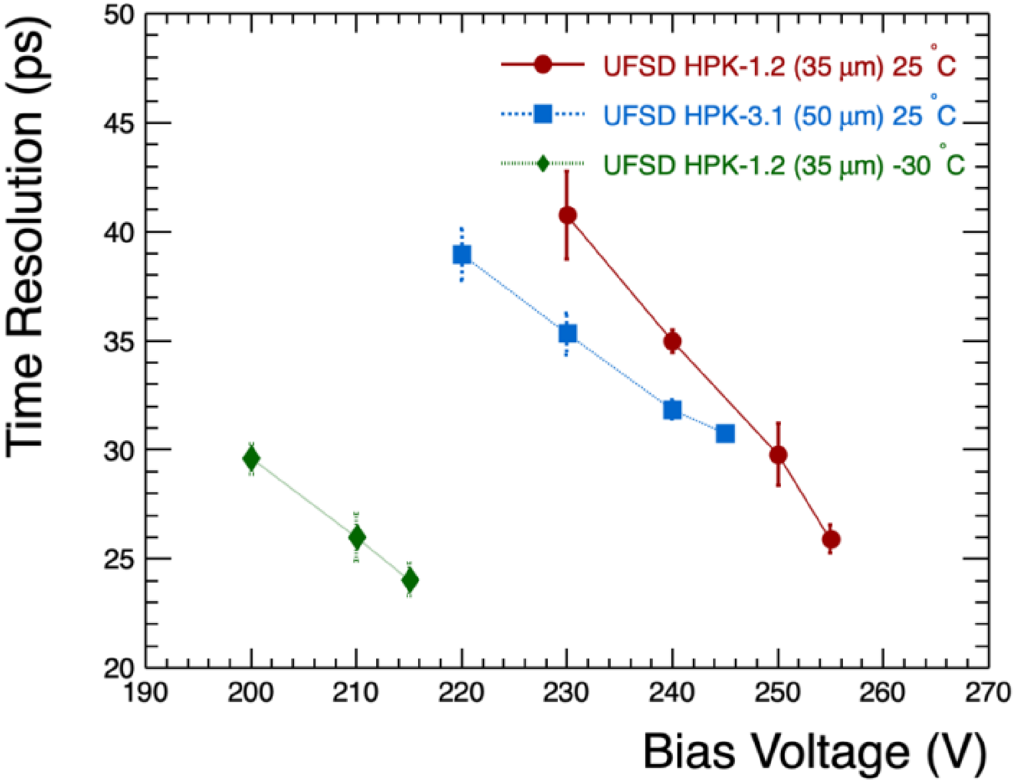


F. Carnesecchi – ALICE simulations
Landau noise for MIPs in LGADs

Thin LGADs – beam test

- Measurements on thin LGADs (35um thickness) confirm the predicted time resolution
- Thin LGADs produced by several manufacturers are available

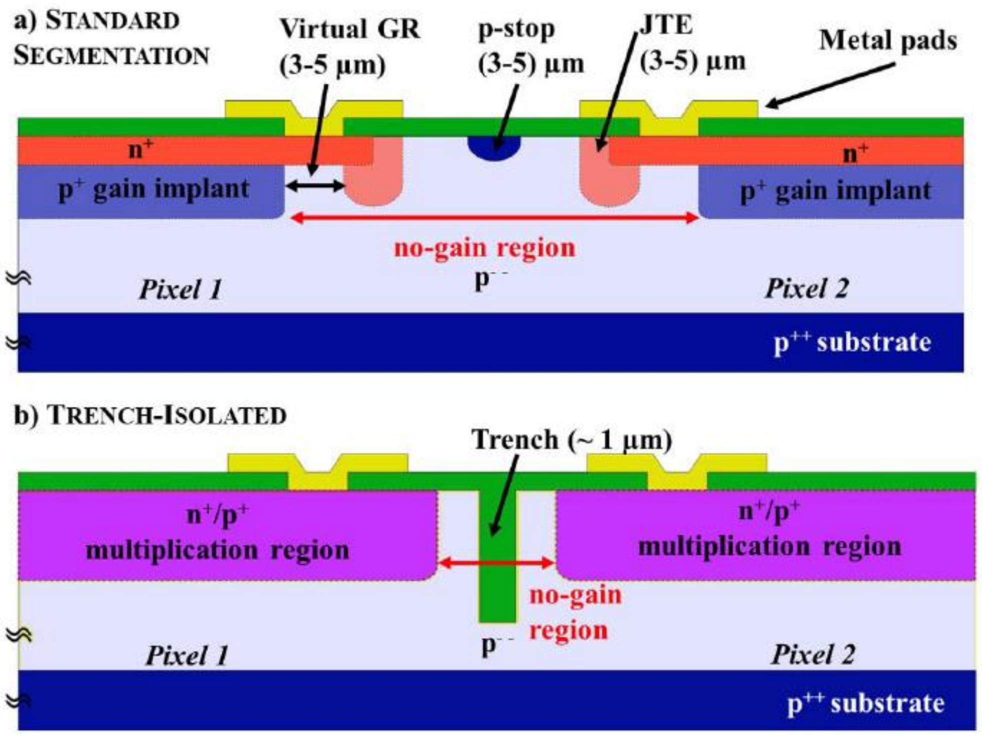




M. Jadhav et al 2021 JINST 16 P06008

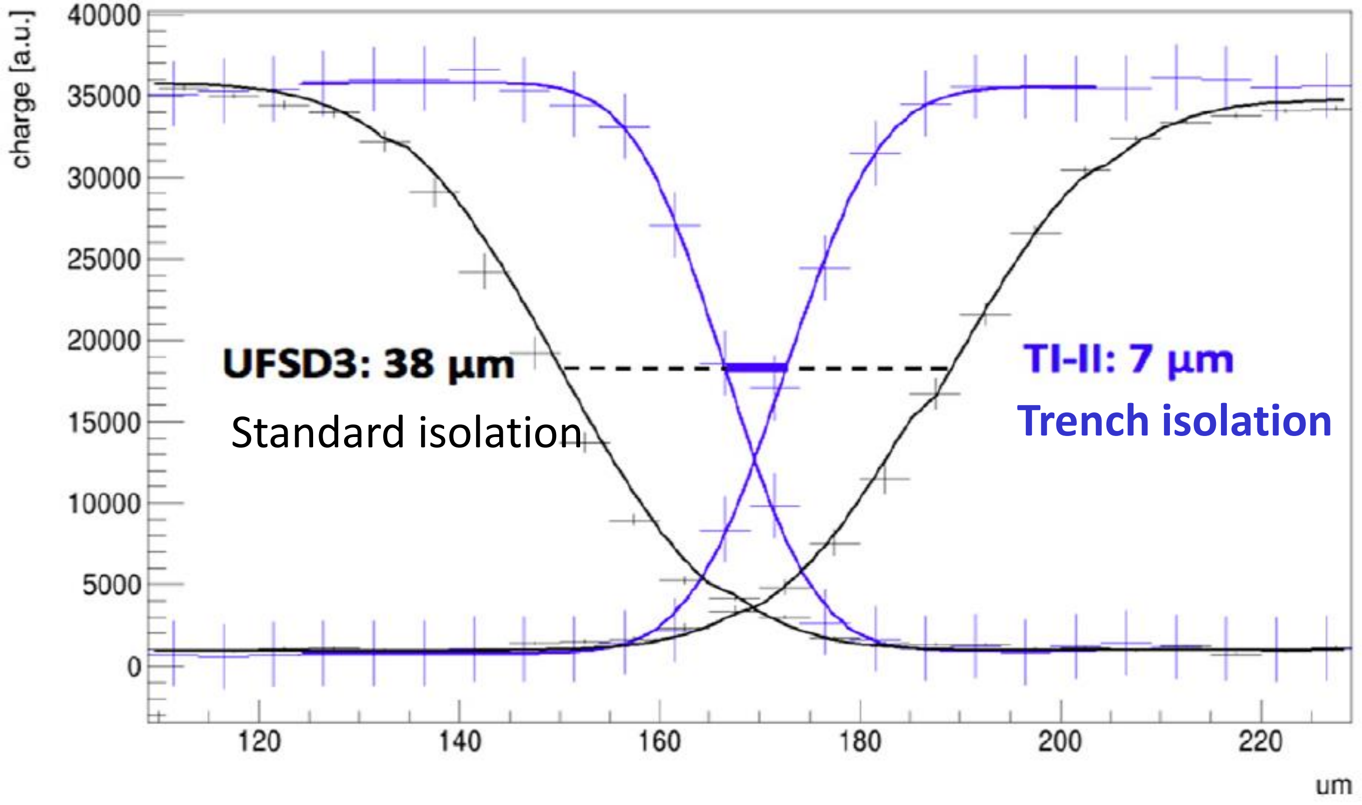
Reducing the dead area in LGADs: Trench Isolation

N-deep ring replaced with a trench: the no-gain area is reduced



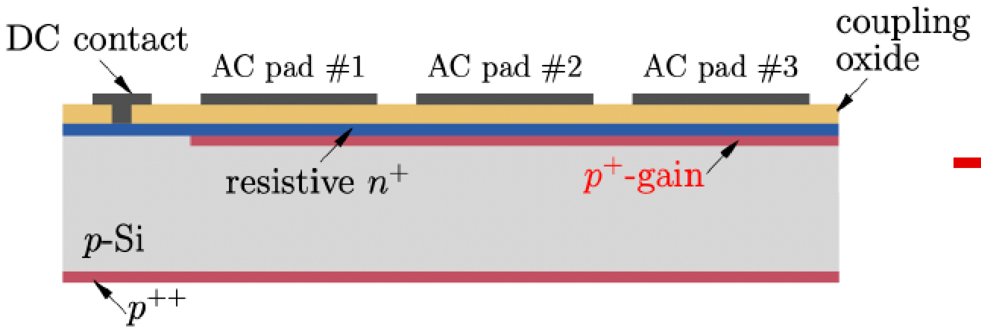
G. Paternoster et al., IEEE Electron Dev. Lett., Vol. 41, No. 6, June 2020

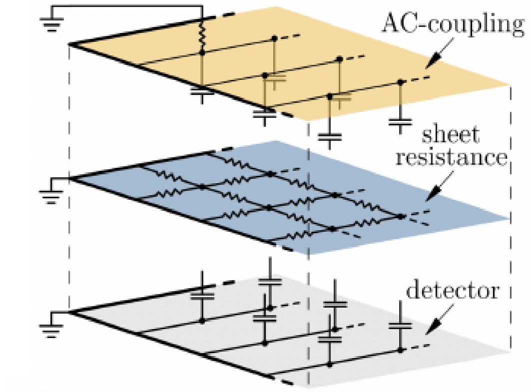
Signal amplitude with pulsed laser – top side illumination

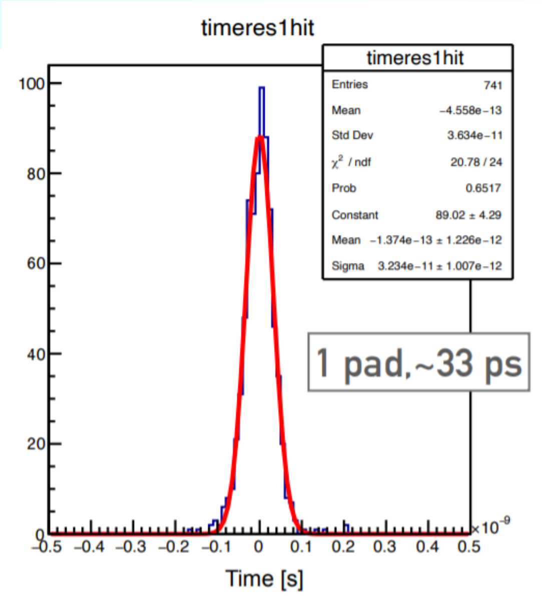


R. Arcidiacono et al., NIMA 978 (2020) 164375

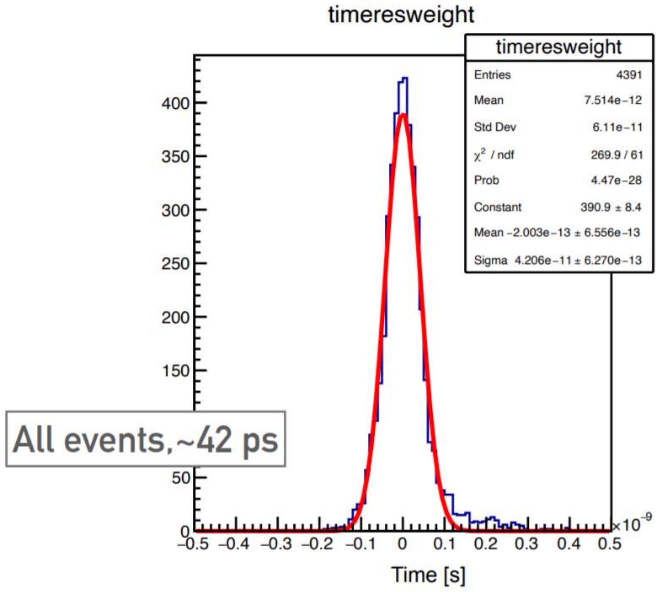
AC coupled LGADs







1 pad,~33 ps



All events,~42 ps

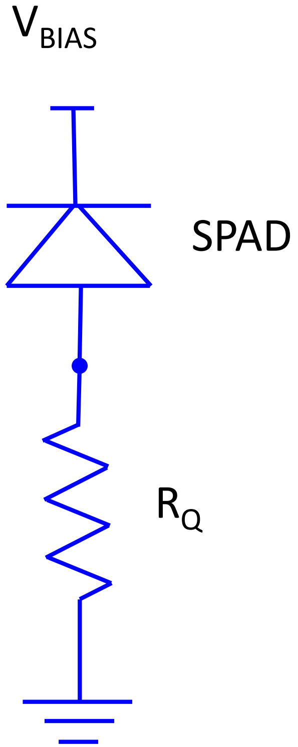
- 100% fill factor
- First promising results on timing and spatial resolution with 50µm FBK sensors
- Samples produced by FBK, BNL, HPK

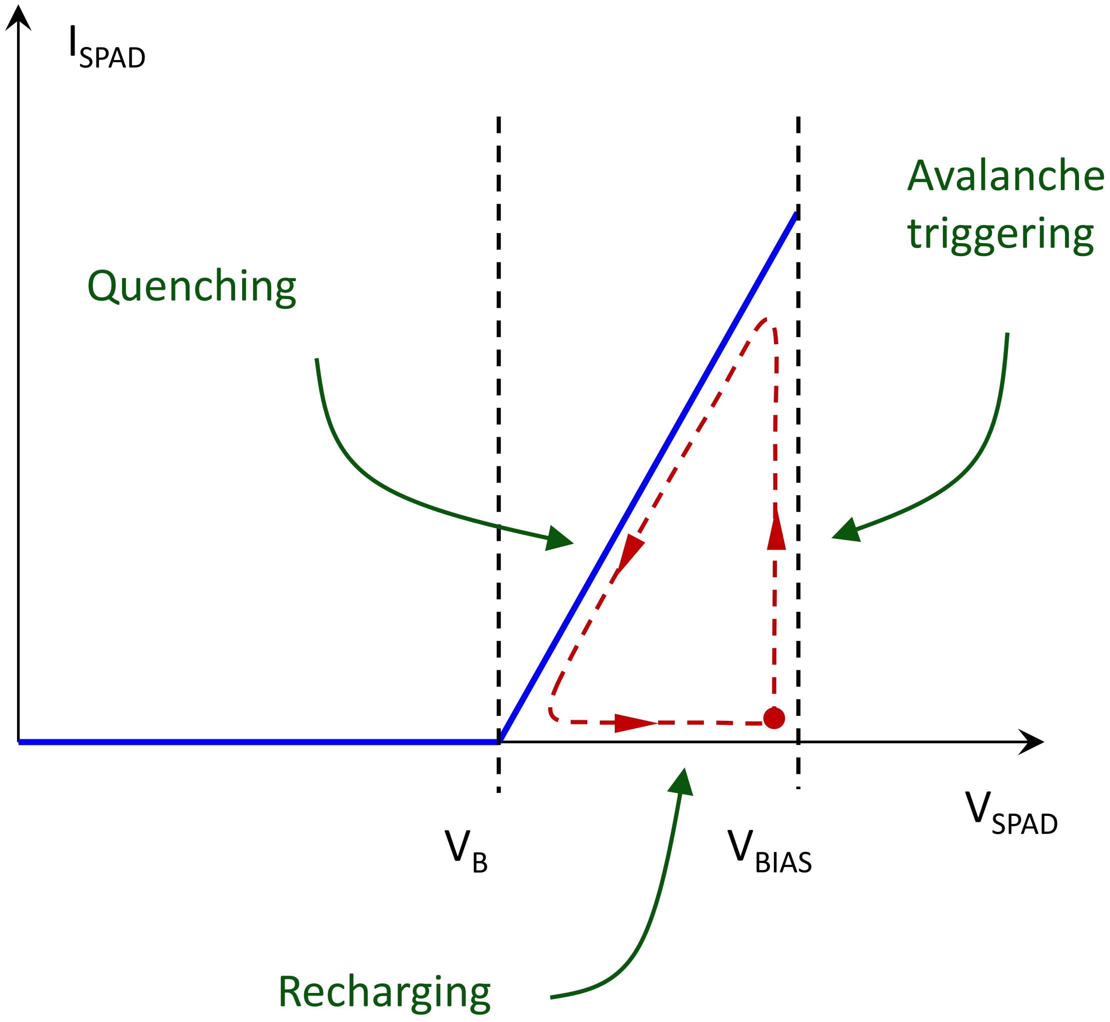
M. Mandurrino et al., arXiv:2003.04838 (2020)

M. Tornago et al., 36th RD50 Workshop

Single-Photon Avalanche Diodes (SPADs) and SiPMs: operation

- Triggered (Geiger-mode) operation
- Available devices designed for photon counting and timing
- The best devices have a photon timing resolution $\sigma_t < 20$ps
- Dead time ~10 - 100ns
- High dark count rate: 20 - 200 kHz/mm^2 at room temperature

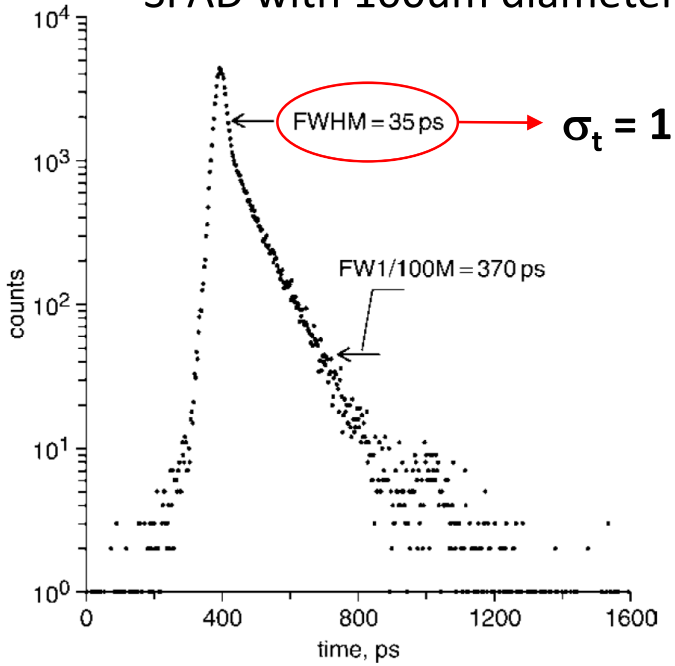




Large Si SPADs: SoA photon timing resolution

- **Thin active region (a few µm)**, saturated drift velocity, response free from diffusion tails → Dedicated fabrication process
- Homogeneous electric field: circular area
- Low threshold: resolution independent from size

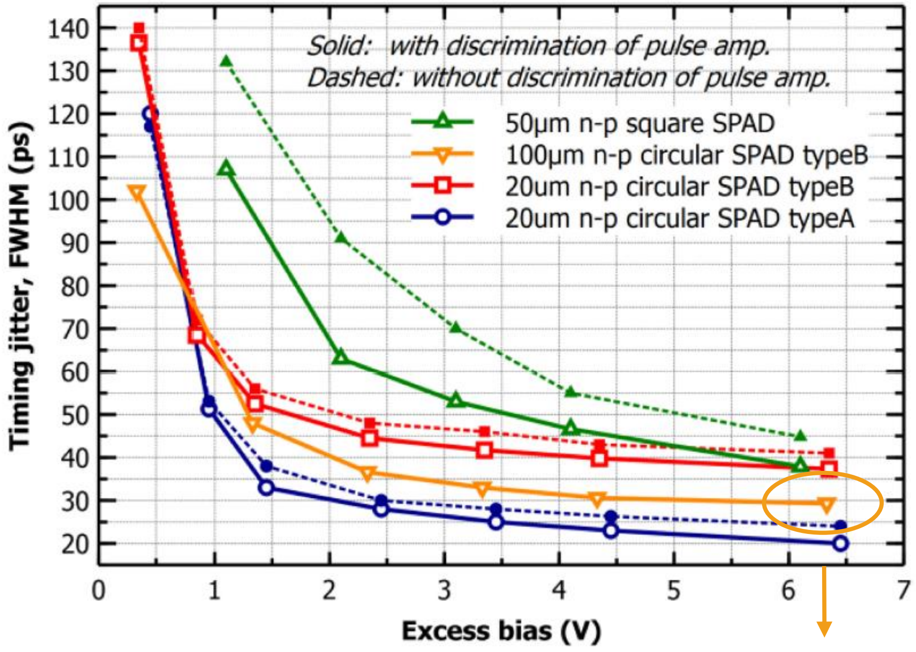
SPAD with 100um diameter at PoliMI



σ_t = 15ps

A. Gulinatti et al., Electronics Letters, Vol. 41 No. 5, 2005

SPAD with 100um diameter produced at FBK

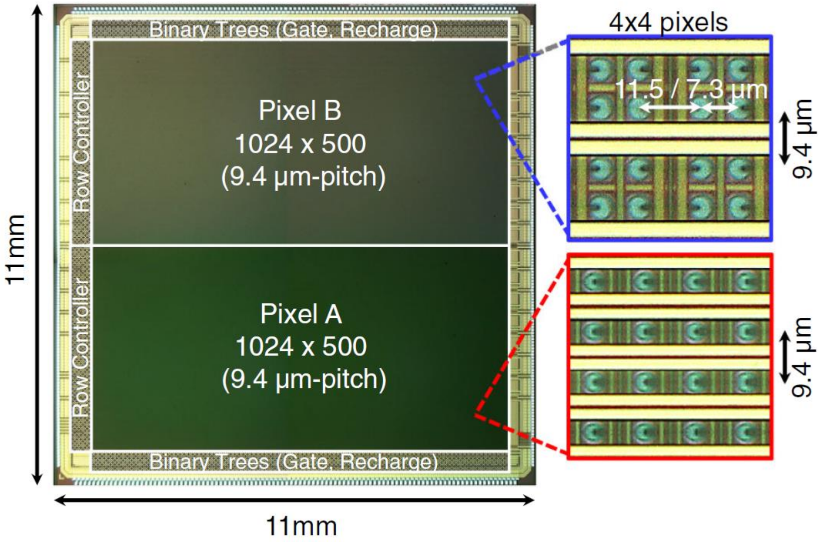


F. Acerbi et al., IEEE J. Selected Topics Quantum Electron., Vol. 20, No. 6, 2014

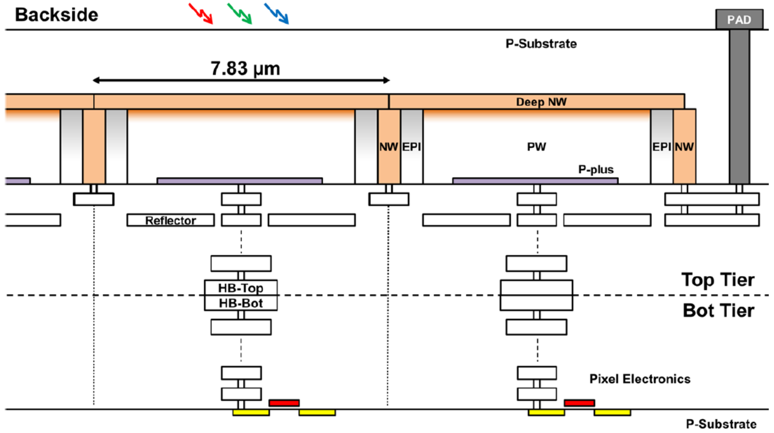
σ_t = 12.8ps

Monolithic and hybrid SPAD arrays

- Many designs demonstrated, up to 1Mpixel (Canon)
- Granularity: down to a few um
- Fill Factor: limited by device guard-ring and electronics. Typically 20 – 50%
- SPAD arrays with 3D-stacked electronics demonstrated (STM)
- A few proof of concept designs for particle counting and tracking presented so far, but no timing results with particles
- Weakness: radiation resistance.
  DCR increases considerably at fluences $> 10^{10}$- 10^{11} $1MeVn_{eq}/cm^2$

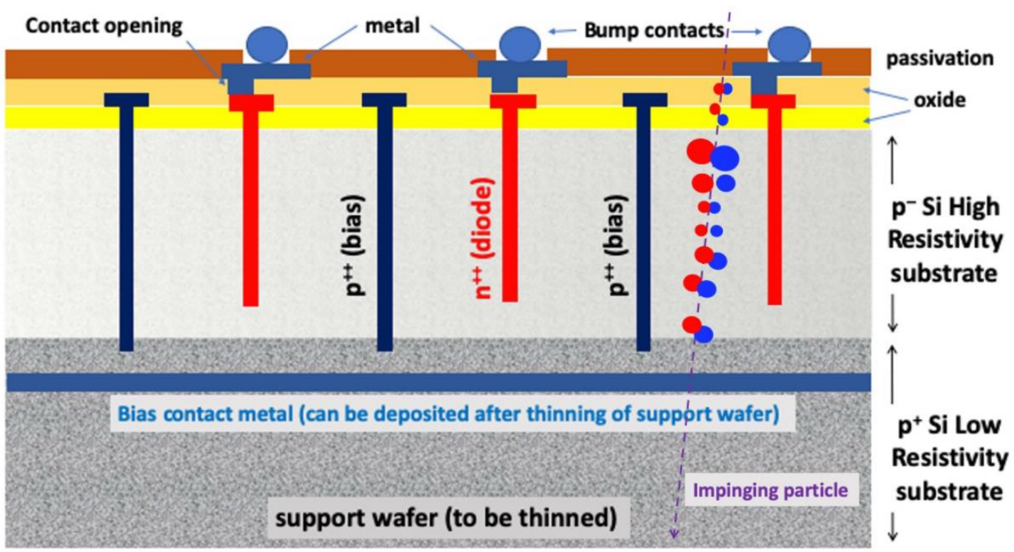


K. Morimoto et al., Optica, 7, 4, 346-354 (2020);

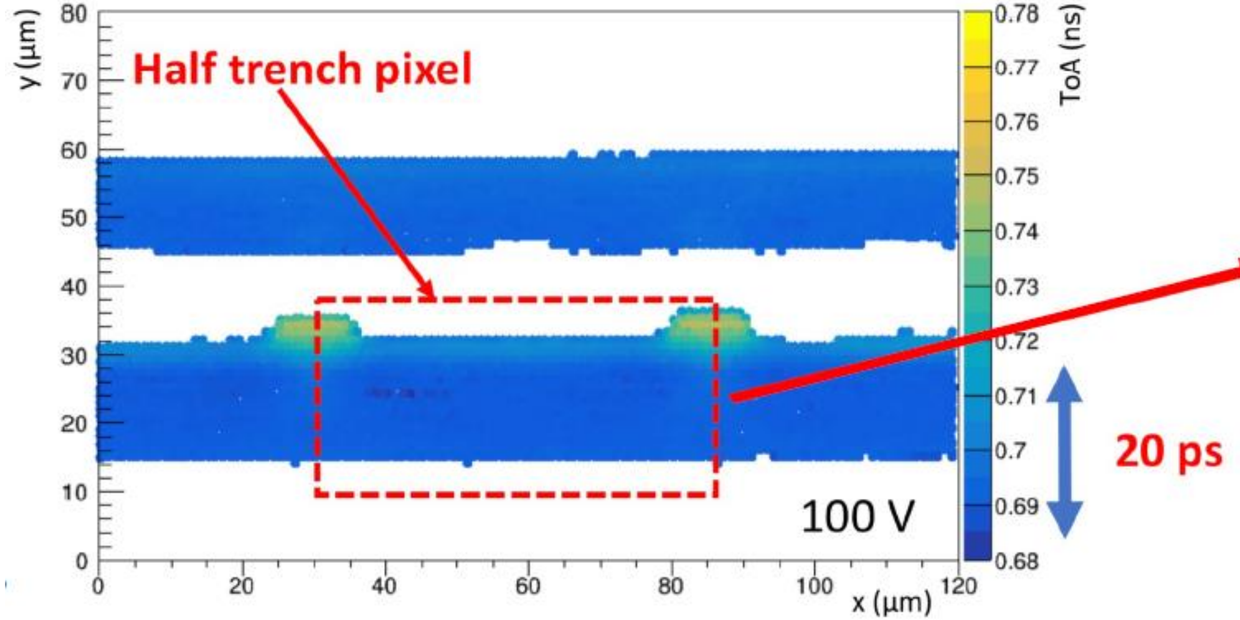


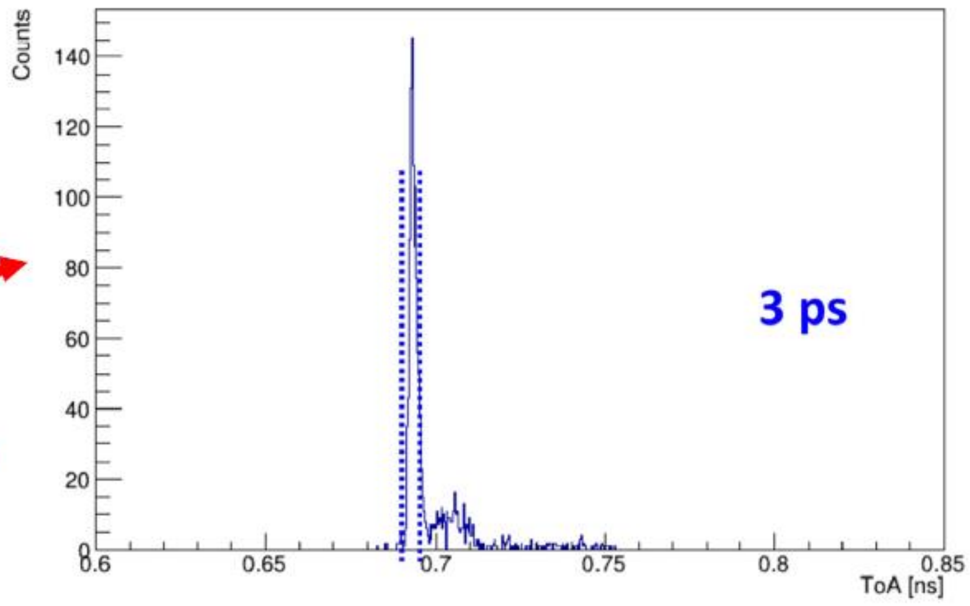
T. Al Abbas et al., IEEE IEDM 2016

Timing with 3D detectors: TimeSPOT



- **Thick active volume** but short drift length: combines large signal and large slope
- Trench geometry (**uniform electric field**): very narrow Time of Arrival distribution

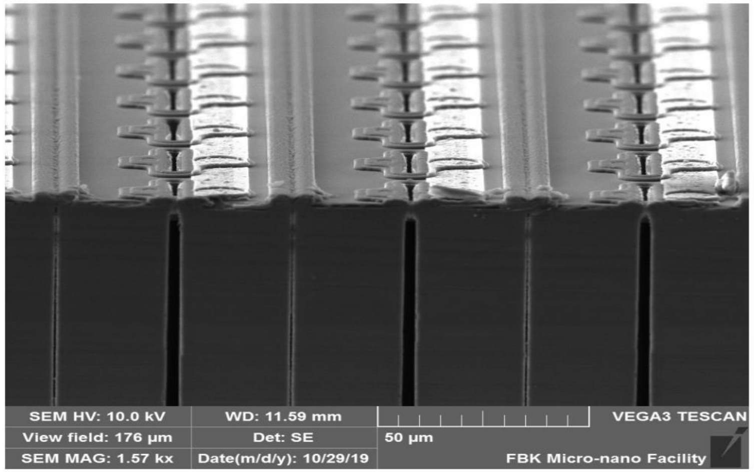


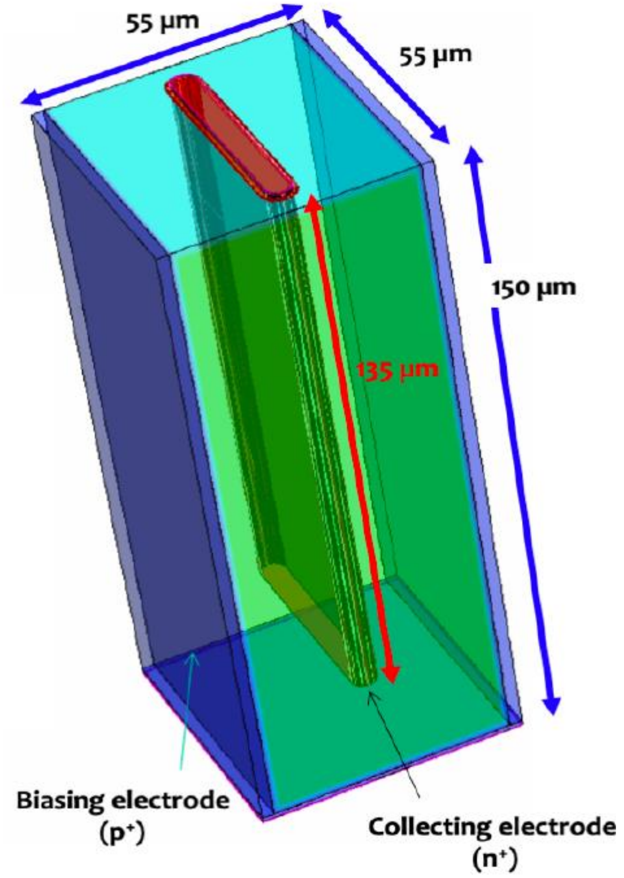


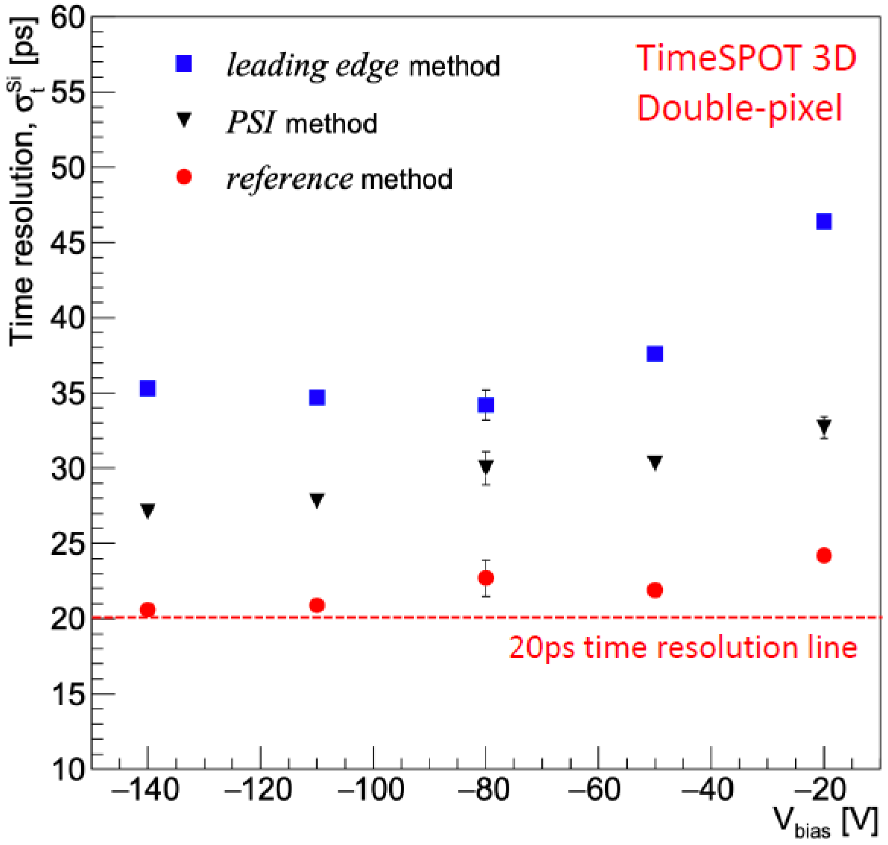
A. Lai, Vertex 2021

Timing with 3D detectors

- Trench distance: ~20μm
  saturated velocity v_{sat} :
  $t_{coll} = D/v_{sat} \sim 200$ps
- Weakness:
  complex fabrication process, mechanical stability of wafers (yield)







L. Anderlini et al, arXiv:2004.10881v2 [physics.ins-det] 29 Jul 2020

Timing with monolithic sensors: challenges and opportunities

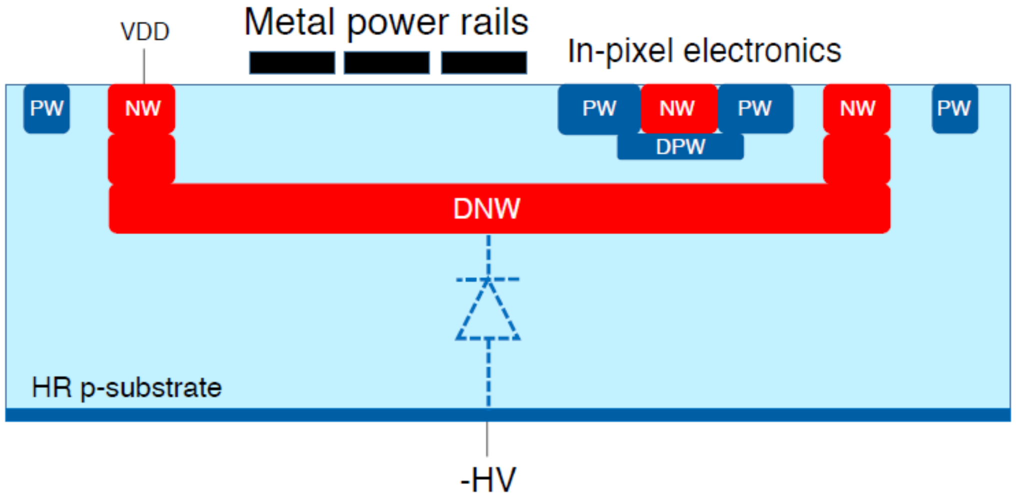
- **Advantages:**
  - Potentially **100% efficiency**
  - Excellent **radiation hardness** demonstrated for several processes
  - **Cost**-effectiveness

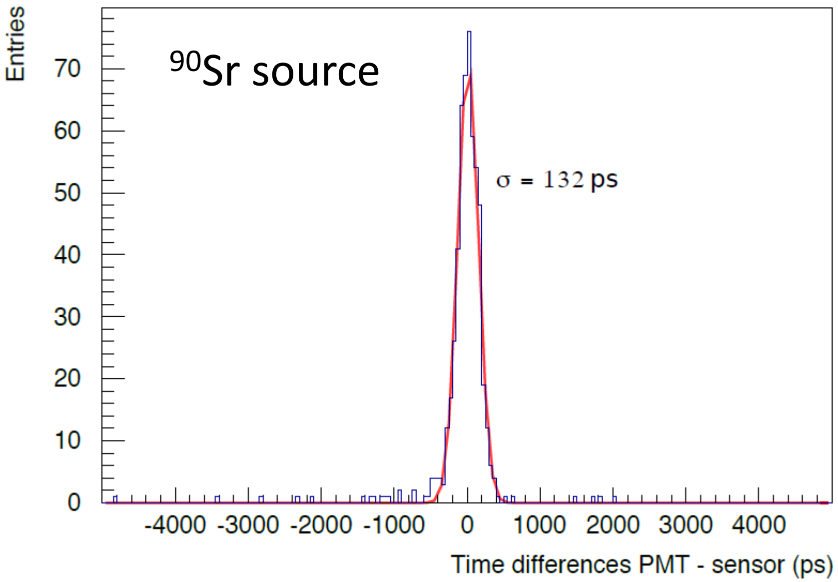
- **Challenges:**
  - Fast collection (100s of ps) and low capacitance at the same time
  - Pixel **non-uniformity** correction needed
  - Jitter is more critical than for LGADs. In most monolithic devices demonstrated so far the timing resolution is > 100ps
  - Low **jitter** with acceptable **power** consumption

HV-CMOS approach: CACTUS

- Deep nwell collection diode
- FE electronics inside the pixel
- Fast and uniform charge collection
- Substrate thickness: 200um
- Pixel size: 0.5 – 1 mm^2
- Pixel capacitance: 1 – 1.5 pF

- Noise can be reduced by moving the readout electronics outside the pixels: capacitance reduction

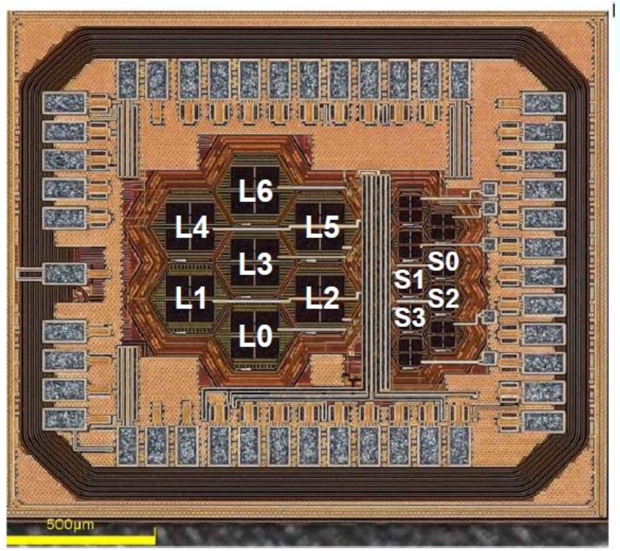


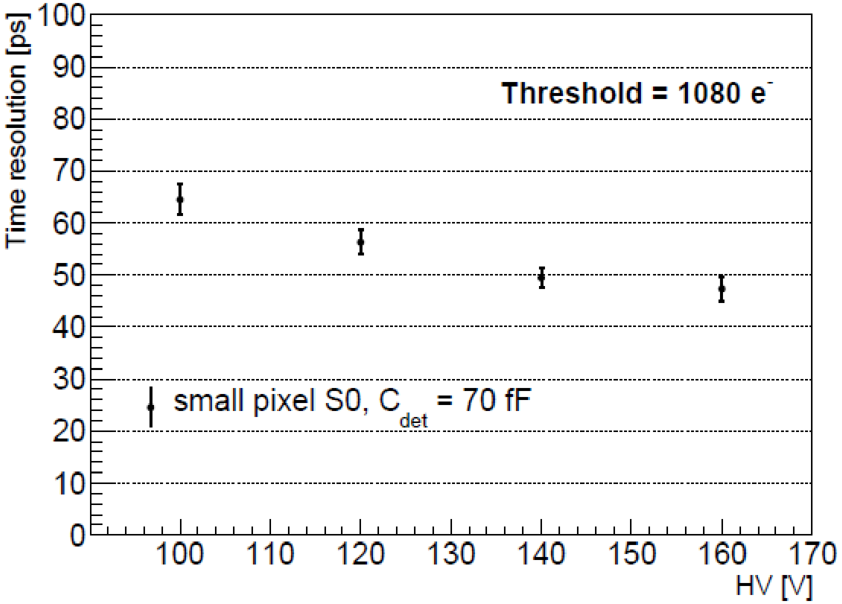


Y. Degerli et al., 2020 JINST 15 P06011

SiGe approach

- SiGe process modified (HR substrate) for the integration of planar silicon detector
- High speed – low noise on-chip SiGe preamplifiers placed outside the pixels
- Hexagonal pixels with 130 and 75 um side
- Depletion depth: 26um at -140V
- Large detector capacitance (70 - 220 fF)
- Nearly 100% collection efficiency
- ~ 50ps timing resolution demonstrated with ^{90}Sr source

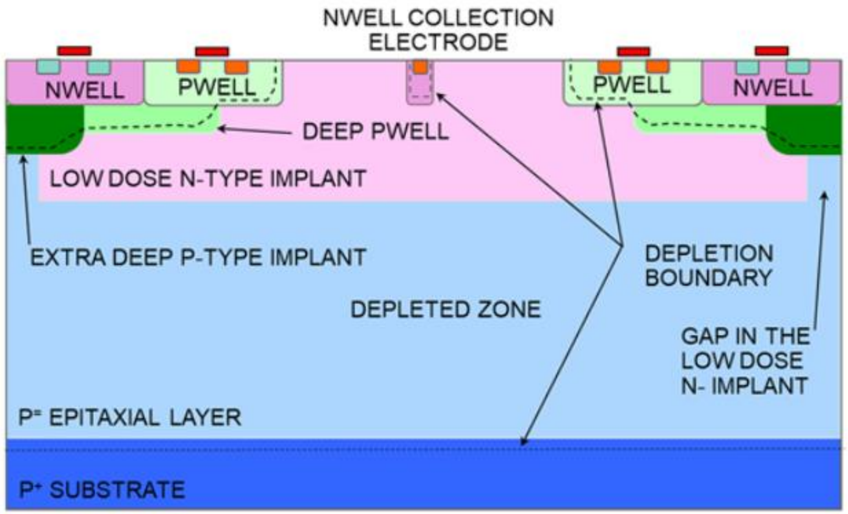


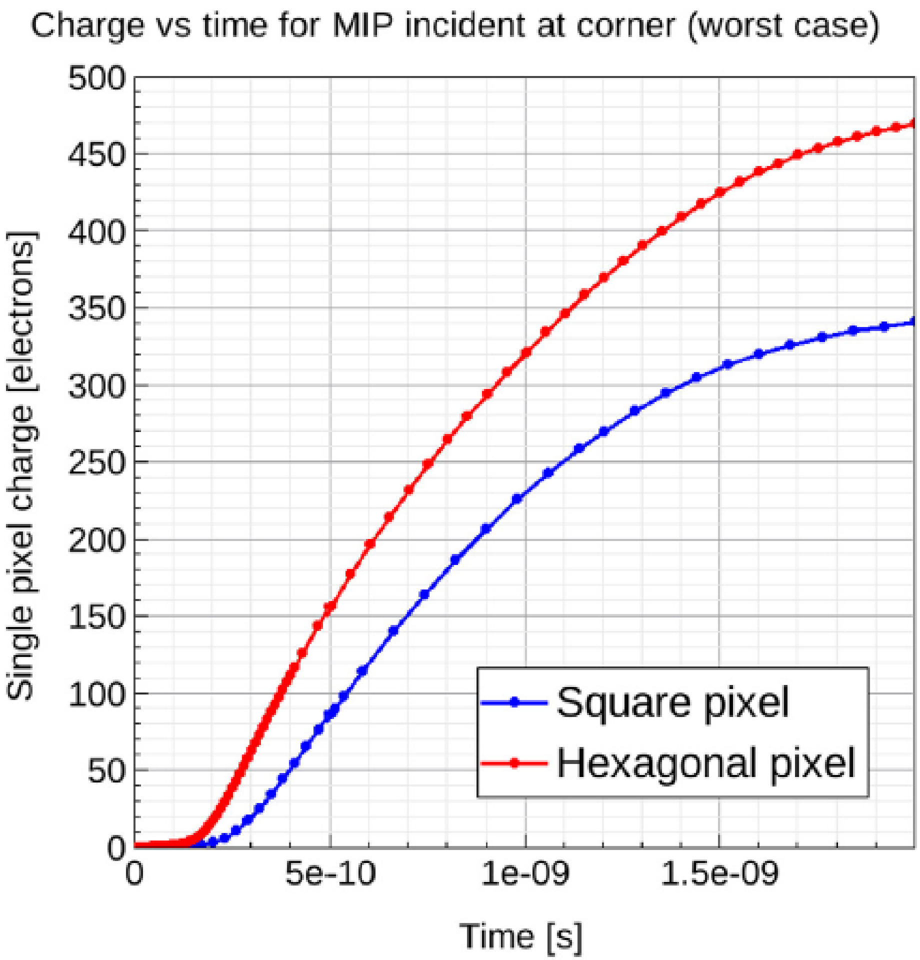


G. Iacobucci et al., 2019 JINST 14 P11008

Fastpix

- Evolution of the MAPS developed for the ALICE tracker: full depletion + speeding up the electron lateral drift
- Test chip with small pixel pitches (10 - 20 μm)
- Very low electrode capacitance (< 1fF)
- Expected jitter (electronics): 20ps @ Q_{in} =1000 e^-

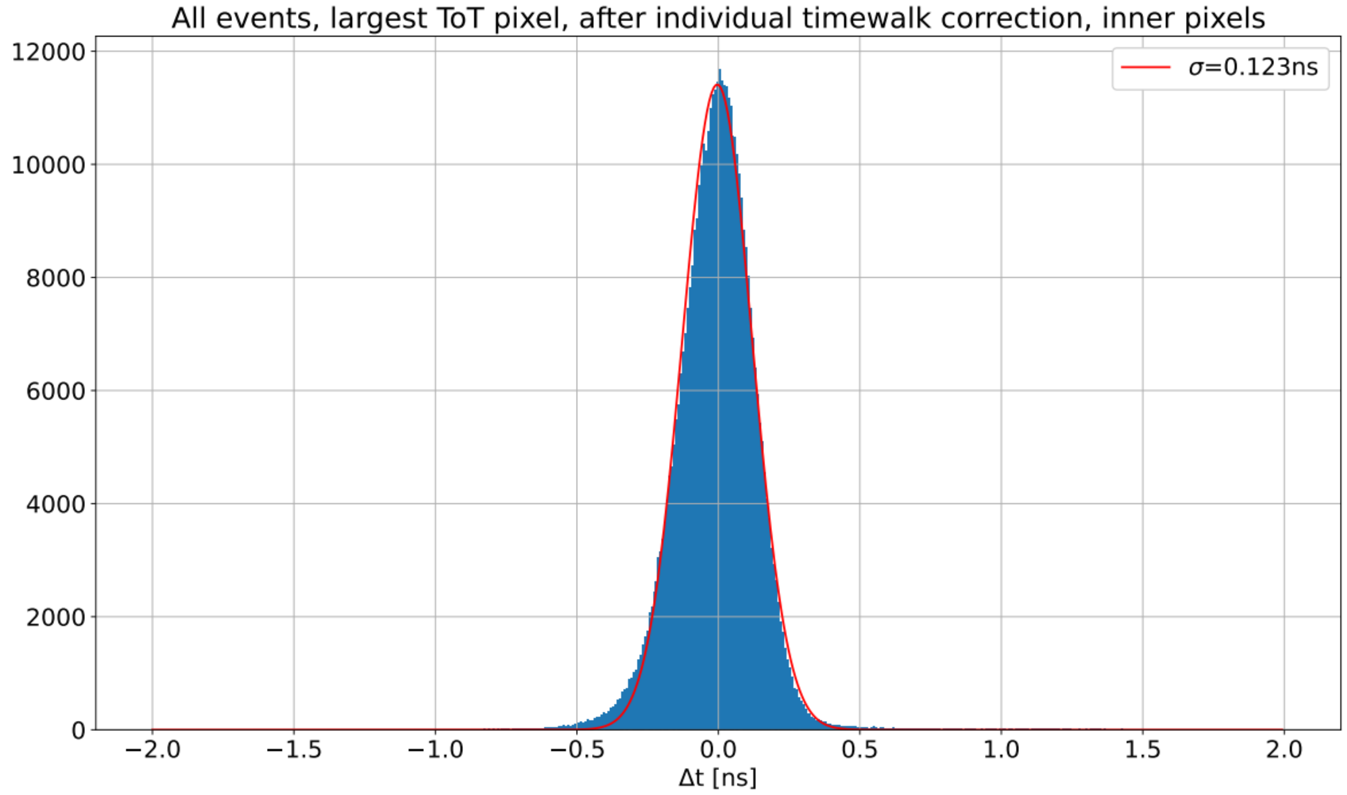




T. Kugathasan et al., Nucl. Inst. Meth. A Vol. 979, Nov. 2020

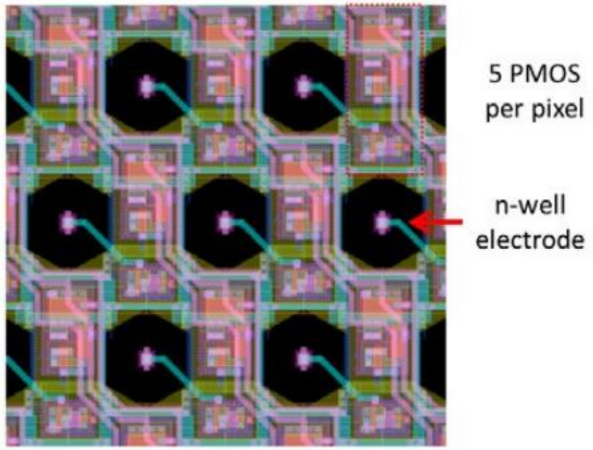
Fastpix – test beam results

- Time walk correction
- Pixel-by-pixel correction for best results
- 70e- threshold for 20um and 50e- threshold for 10um pixels



E. Buschmann et al., 2021

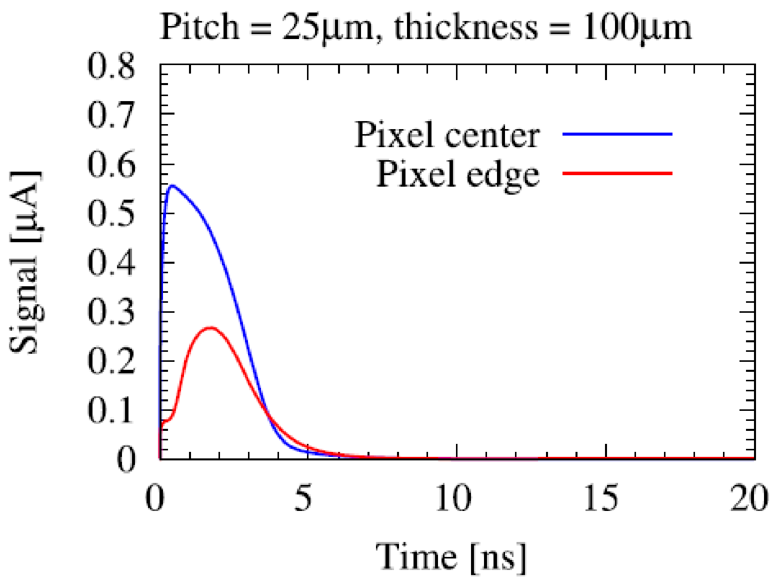
Pixel in the matrix

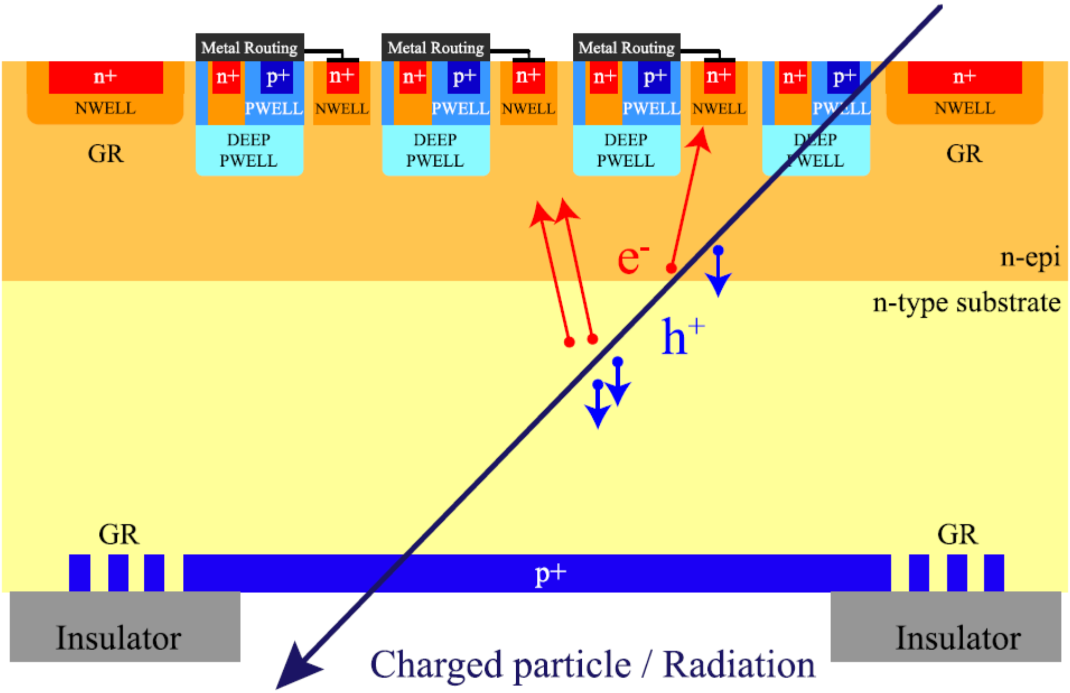


Test beam: timing resolution < 140 ps for both 10 and 20um pitch

ARCADIA – on going activity on timing sensors

- Fully depleted substrate: charge collection by drift
- Process validated on 50 – 300µm thick substrates, 25 and 50µm pixel pitch
- Complete charge collection in few ns for optimized pixel geometry

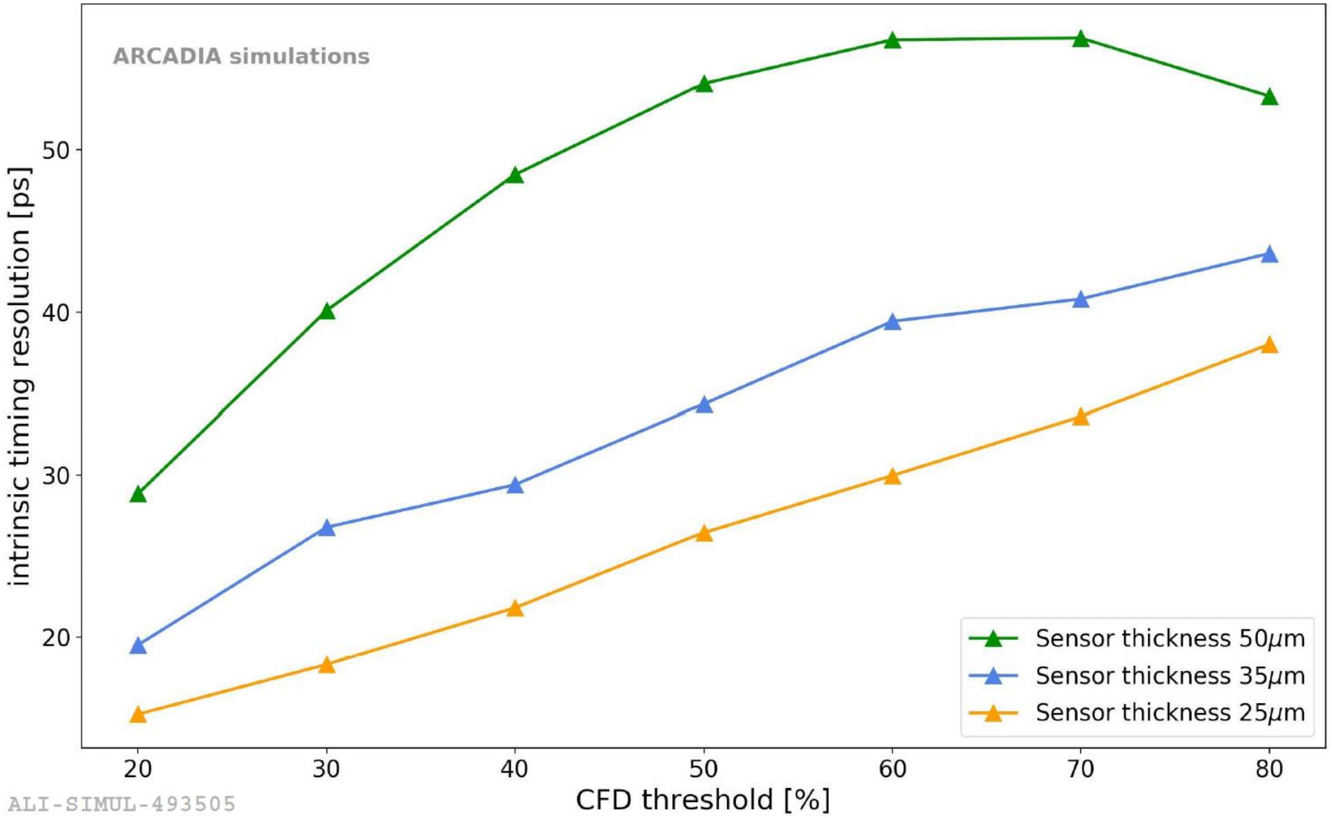




L. Pancheri et al., IEEE Tran. Electron Dev., Vol. 67, No. 6, June 2020

Intrinsic timing resolution: 50 µm pitch pixels

Intrinsic timing resolution: $\sigma_{\text{distortion}}$ and $\sigma_{\text{Landau noise}}$



L. De Cilladi

- Capacitance: 30 – 35fF
- Thin substrates: better intrinsic resolution (as observed for LGADs)
- N.B.: **Electronics noise (σ_{jitter})** not considered in this simulation. Tradeoff between jitter and power consumption

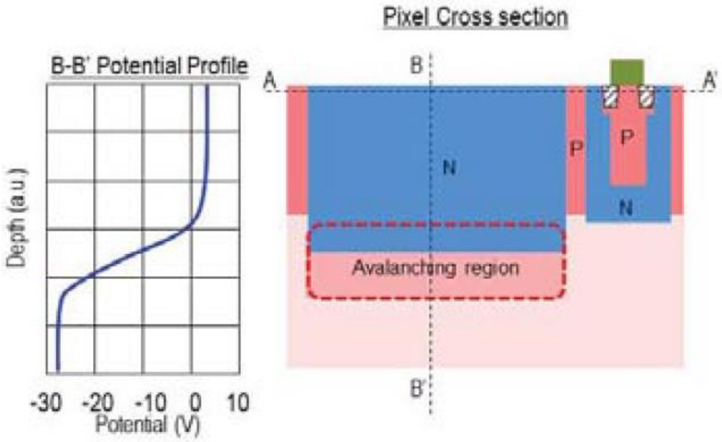
Test pixels with 50µm thickness and integrated amplifier are in production

Monolithic avalanche detectors

Several recent examples of **avalanche gain integrated in CMOS** sensors:

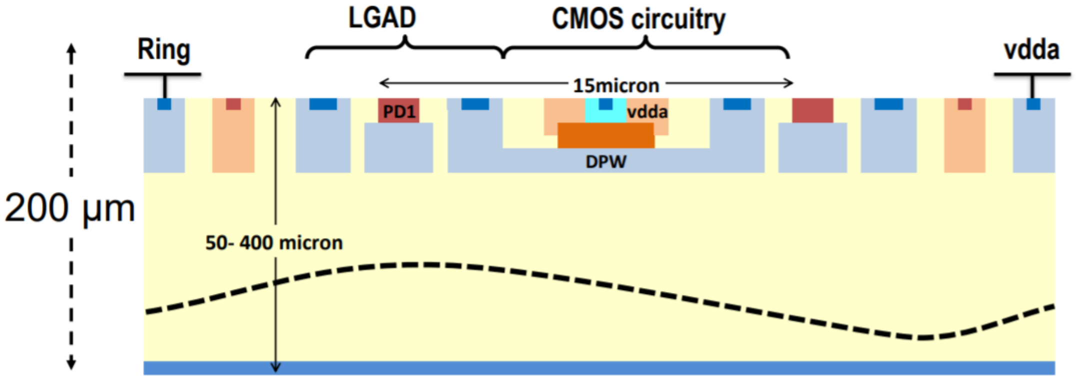
- The feasibility of structures designed for **photonics applications** can be verified for particle detection
- Foundries may be available to implement simple **process modifications**, needed to add gain to CMOS sensors

Fine-pitch avalanche pixels with 6um pitch (Panasonic)



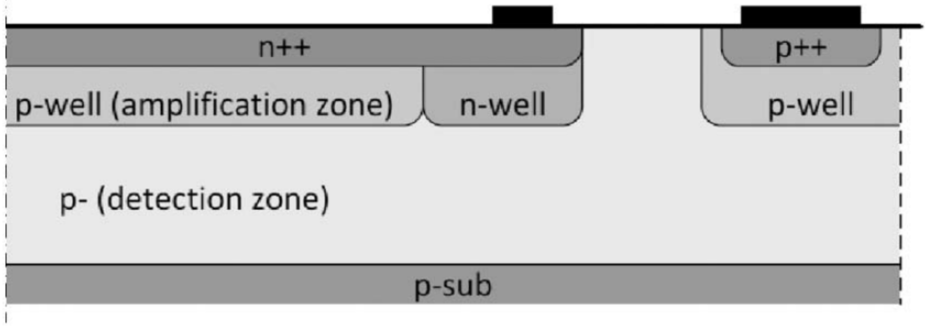
Y. Hirose et al., IEEE ISSCC 2019

LGADs on thick fully depleted substrates (Sensor Creations Inc.)



S. Lauxtermann et al., Pixel 2018, Taiwan

CMOS-integrated APDs with > 1GHz bandwidth (University of Vienna)



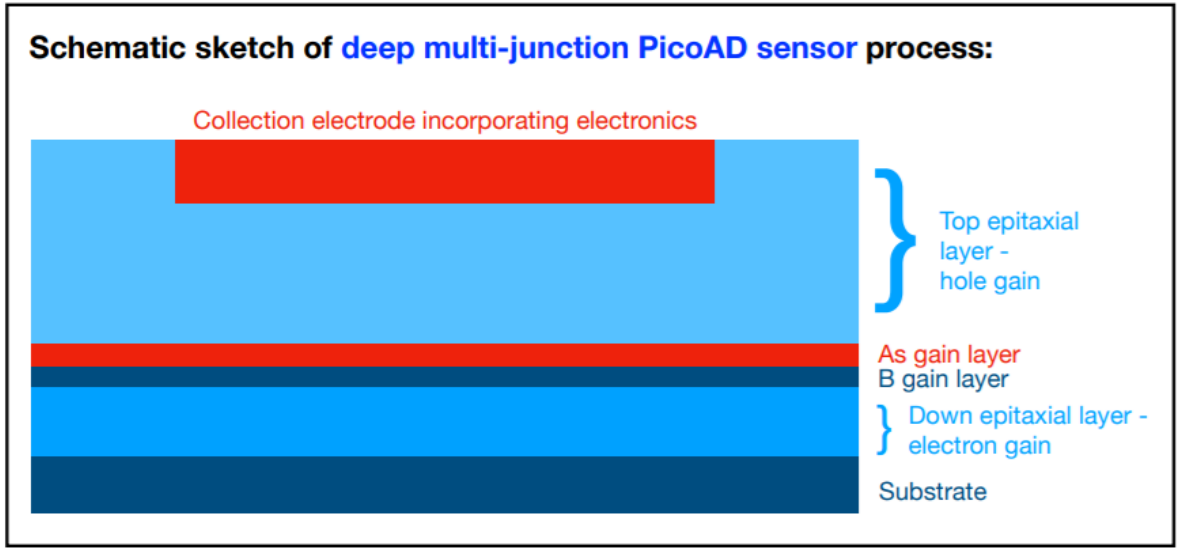
W. Gaberl et al., Opt. Lett., Vol. 39, No. 3, 2014

Monolithic sensors with gain @ University of Geneva

Avalanche gain in monolithic CMOS sensors: may be the key for **combining very high resolution and acceptable power consumption**

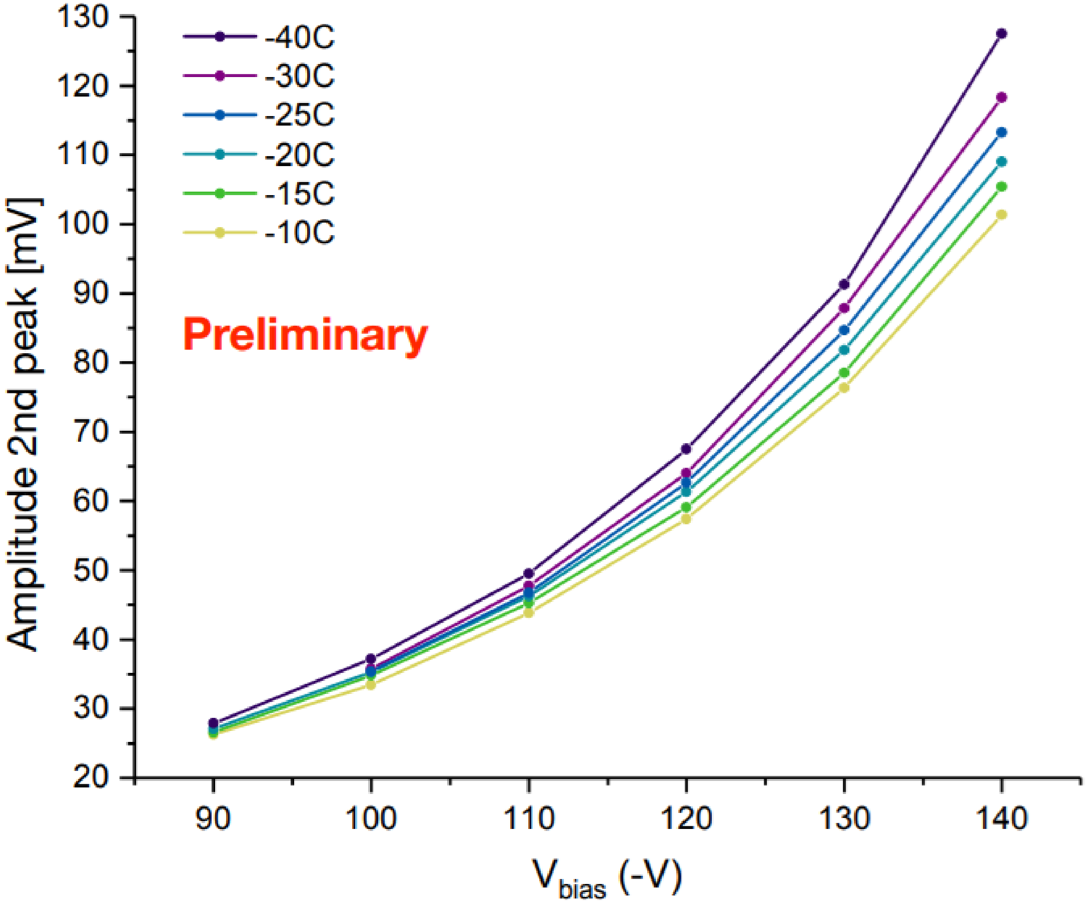
Work in progress … more updates to come soon

Picosecond Avalanche Detector (PicoAD): EU Patent EP18207008.6



Schematic sketch of deep multi-junction PicoAD sensor process:

Measurements of sensor gain using 55-iron source in climate chamber:



M. Munker et al., Vertex, September 2021

Conclusion

- Timing layers based on LGADs with 30 – 40 ps resolutionare realistic (CMS and ATLAS)
- Layers with 20ps timing resolution based on thin LGADs seems within reach in a few years (ALICE)

Several **alternative possibilities** are under investigation:

- Advanced (TI or AC-coupled) LGADs with hybrid readout
- Monolithic or hybrid SPADs/SiPMs
- Hybrid sensors with 3D electrodes
- Low noise Monolithic sensors
- Monolithic sensors with gain

A solution requires tight interaction between sensor designers, circuit designers, silicon manufacturers, packaging service providers

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- S. Lauxtermann et al., Pixel 2018, Taiwan, https://indico.cern.ch/event/669866/contributions/3234993/attachments/1767987/2871451/1100-Sensor_Creations_Pixel_2018_Mono_DD_CMOS_or_MIP_Detection_and_X_Rays.pdf
- Y. Hirose et al., IEEE ISSCC 2019, https://doi.org/10.1109/ISSCC.2019.8662405
- W. Gaberl et al., Opt. Lett., Vol. 39, No. 3, 2014, https://doi.org/10.1364/OL.39.000586
- M. Munker et al., “Monolith – pico-second time-stamping in fully monolithic highly-granular pixel sensors,” Vertex, September 2021, https://indico.cern.ch/event/1047531/contributions/4520798

Thank you

Backup slides

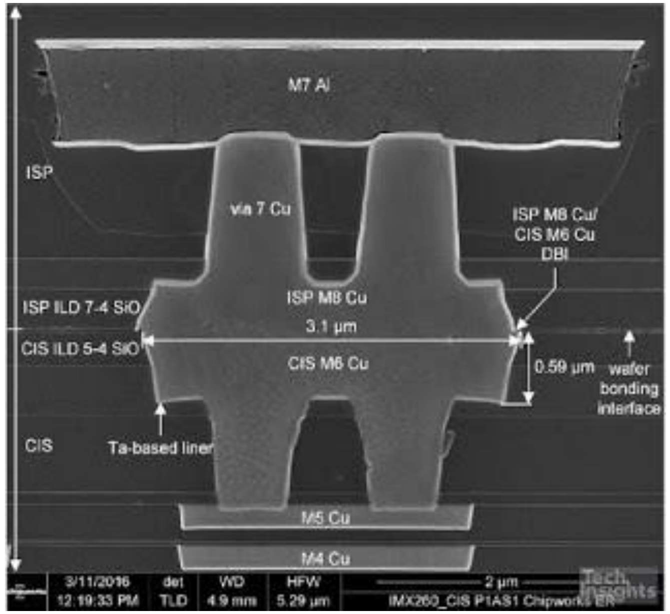
Timing with silicon detectors – a system perspective

The **detector** is just one part of the game:

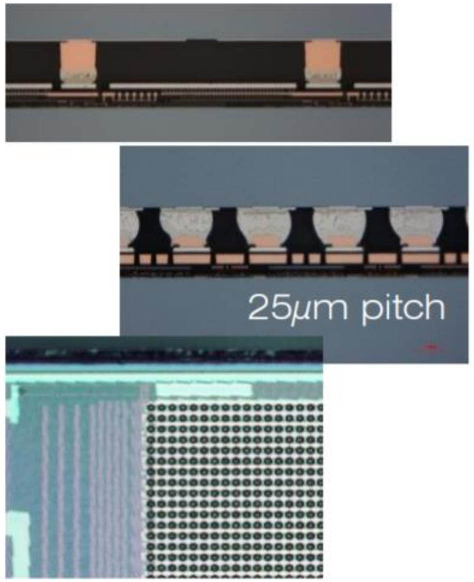
- Performance (**bandwidth, noise and size**) of available **readout electronics** related to:
  - available process technology (cost)
  - available power (cabling and cooling)
  - pixel area (granularity)
- **Pacakging (3D stacking):**
  - **in hybrid detectors** affects the parasitic capacitance (noise)
  - In **monolithic detectors** can be used to integrate advanced (fast and low-power) digital circuits in-pixel

Perspectives for hybrid integration: low-capacitance 3D interconnections

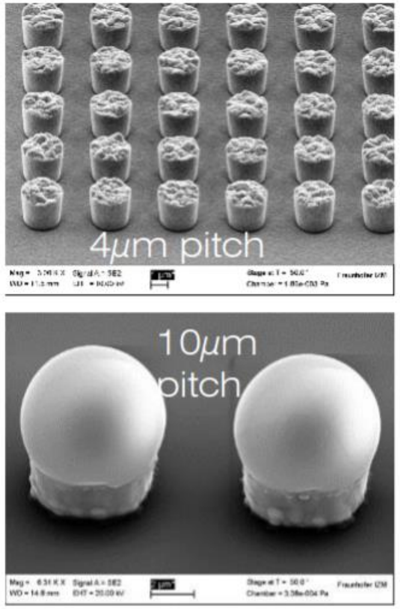
- Hybrid integration development at Sony, STM, TSMC, Samsung, IMEC …
- IZM Fraunhofer fine pitch interconnections
- Today more processes are available, which ones are accessible and cost-effective for research?



Cross section of Sony IMX260 stacked sensor
https://www.techinsights.com/



μ-bumping:
Pitch 50…20μm
Bump size: 25…12μm
Material: Solder bumps, pillar bumps with solder cap



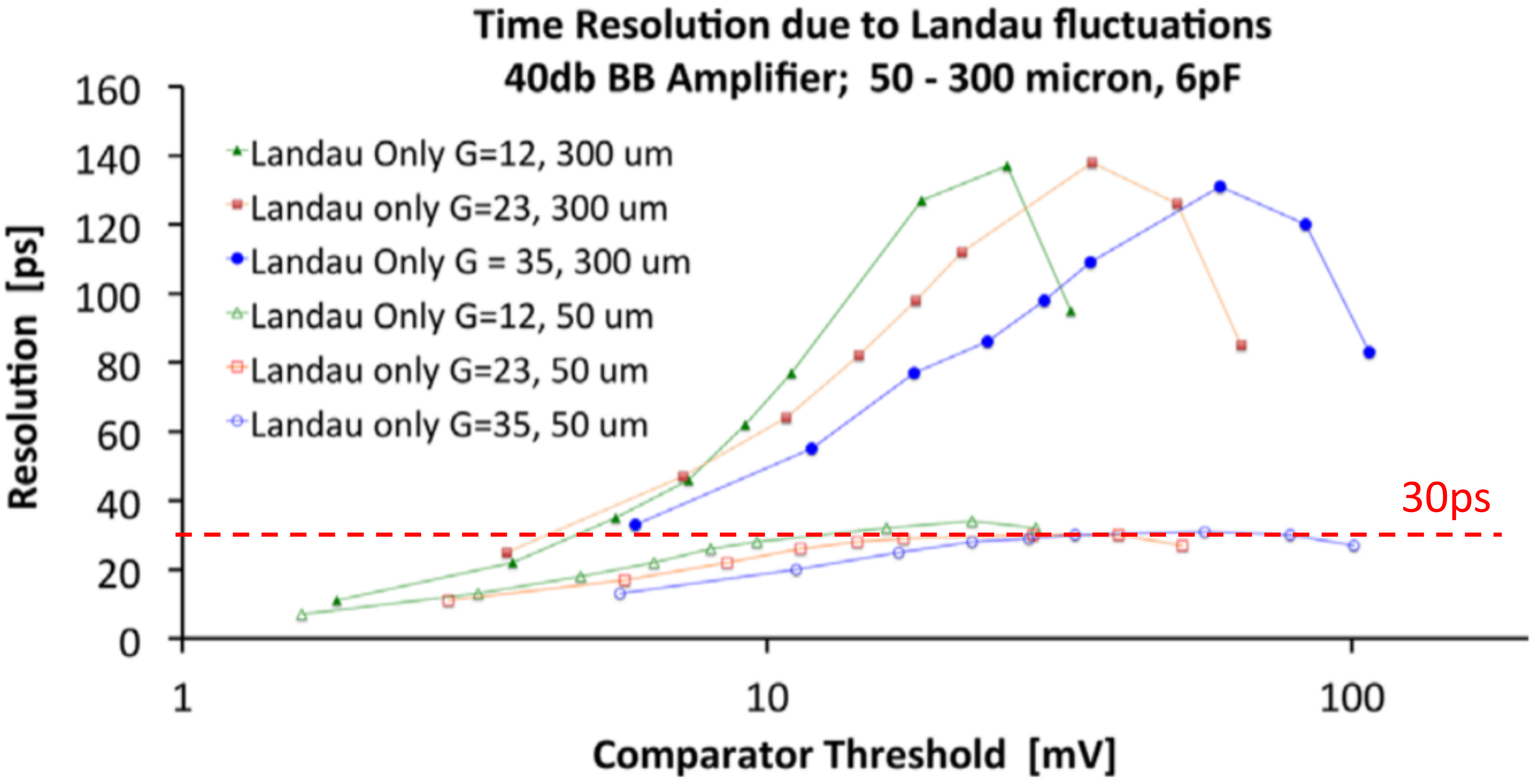
Sub-10μ-pitch:
Pitch 10…2 μm
Bump size: 6…1μm
Material: pillar bumps with solder cap, pillars, pads

T. Fritzsch, et al. AIDA2020 Topical Workshop on Future of Tracking Oxford, United Kingdom, 1-2 April 2019

How to go below 30ps with LGADs?

- Low threshold → practical limits in an array due to jitter, uniformity and electrical cross-talk

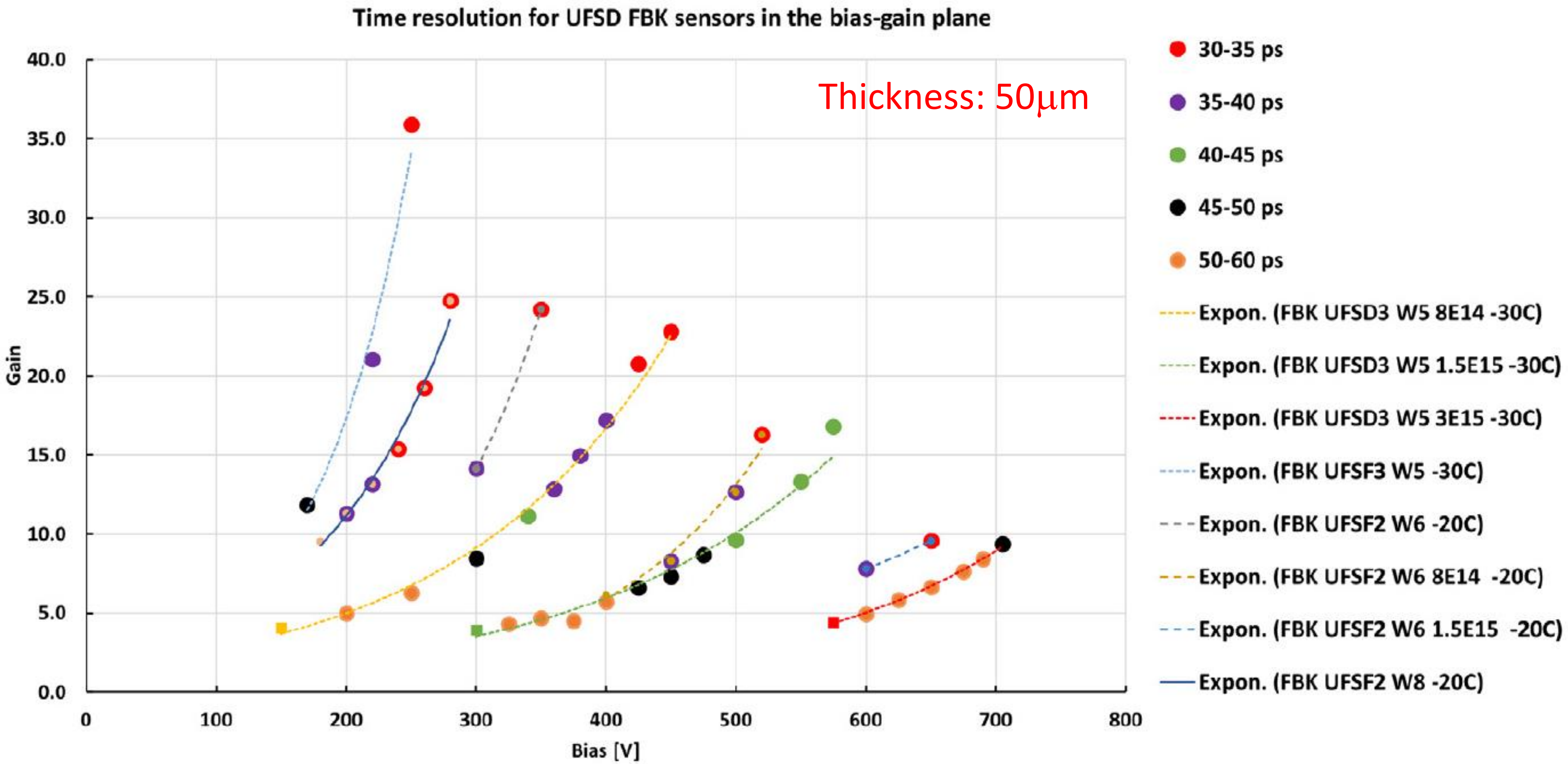
- **Thinner sensors (< 50μm)**



N. Cartiglia et al.,
NIMA 845 (2017) 47–51

LGADs: radiation hardness

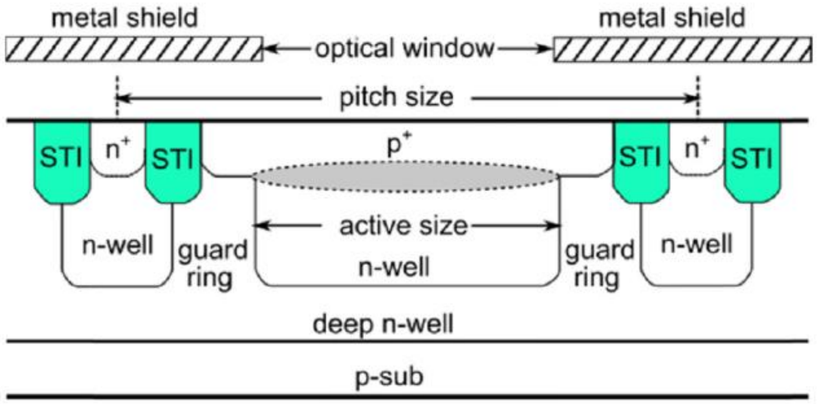
Rad-hard operation and 30ps timing demonstrated up to a fluence > 10^{15} $1MeVn_{eq}/cm^2$

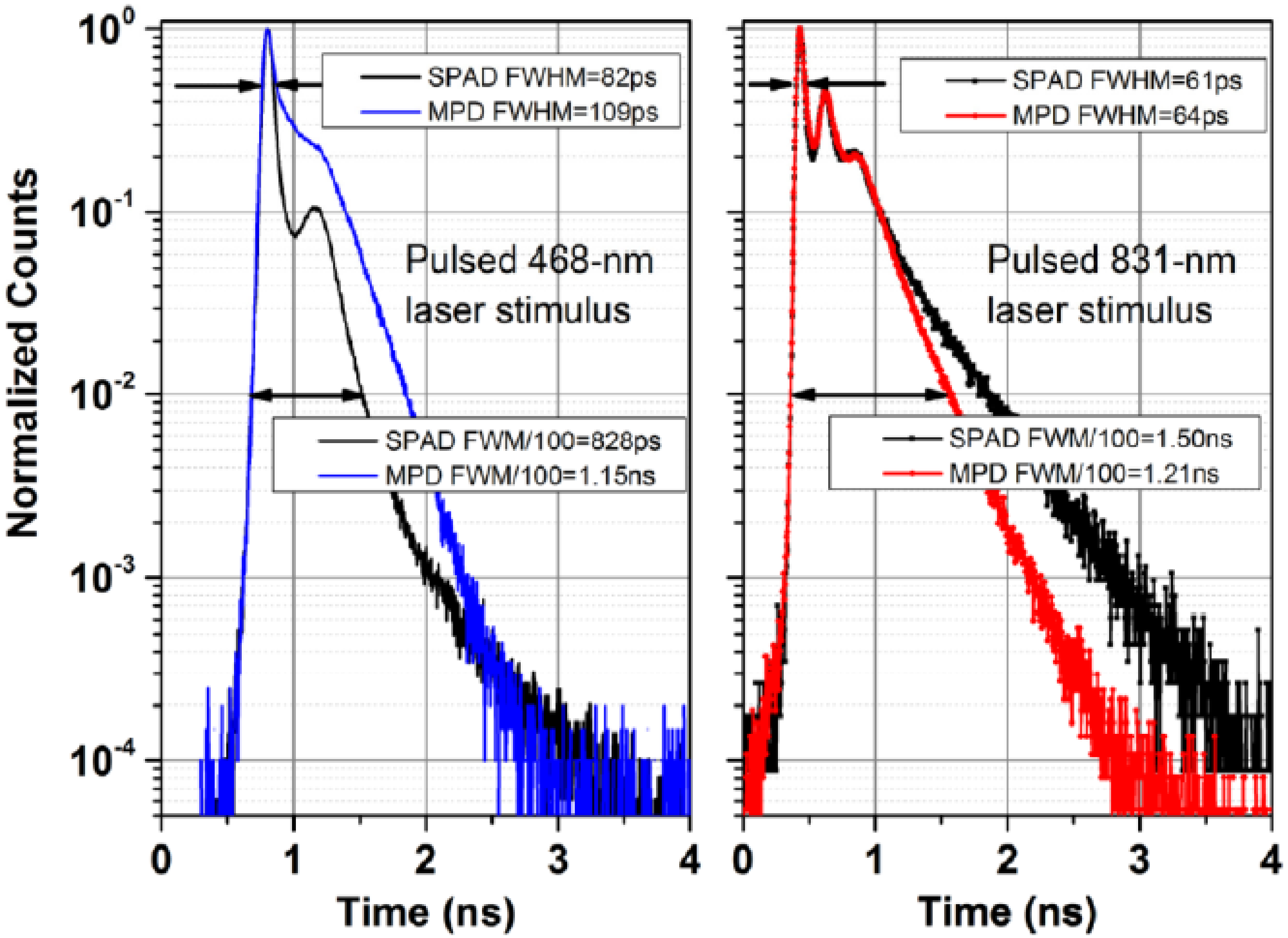


R. Arcidiacono et al., NIMA 978 (2020) 164375

CMOS SPADs

- Fully compatible with standard CMOS
- Higher Dark Count Rate than dedicated processes
- Active region thickness: ~ 1um
- Timing resolution with IR light $\sigma_t < 26$ps



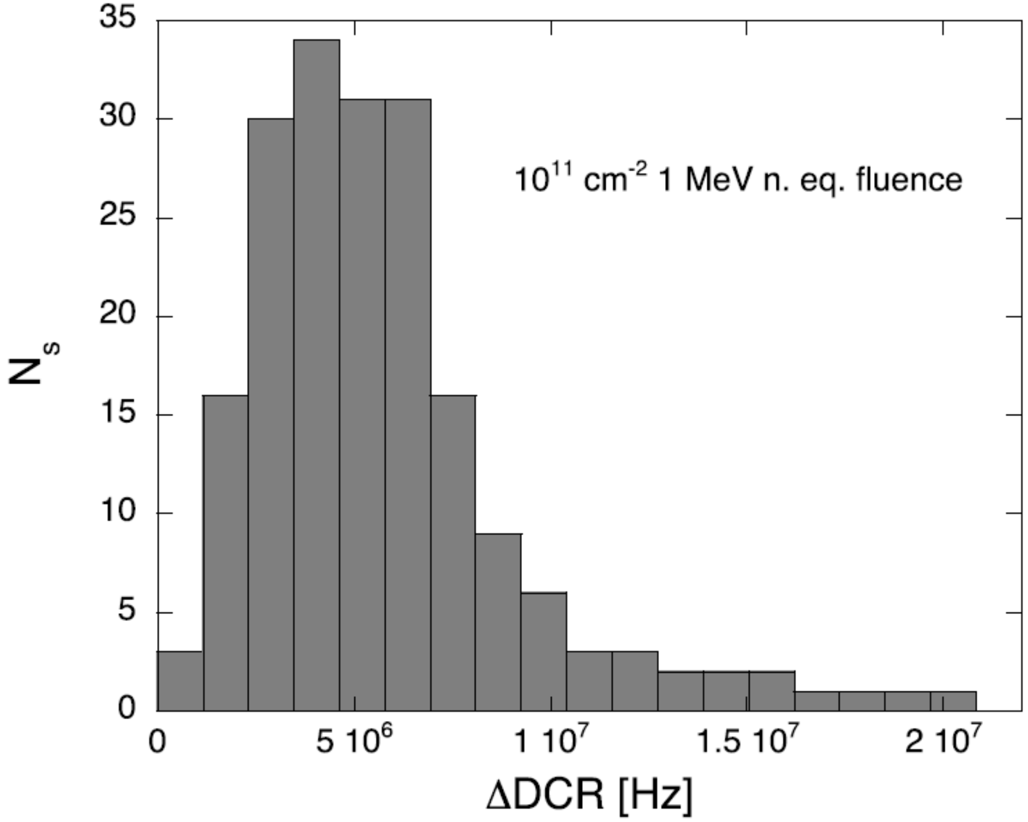


H. Xu et al., Opt. Express 12765 Vol. 25, No. 11, 29 May 2017

SPADs: efficiency for charged particles and radiation hardness

- **Efficiency**: same or slightly larger than the Fill Factor
- Large **increase of DCR** at fluences of 10^{11} $1MeVn_{eq}/cm^2$
- Radiation hardness can be improved by:
    - Reducing the cell size (like in HD-SiPM), but there is a trade-off with Fill Factor (Trench Isolation might be useful)
    - Cooling

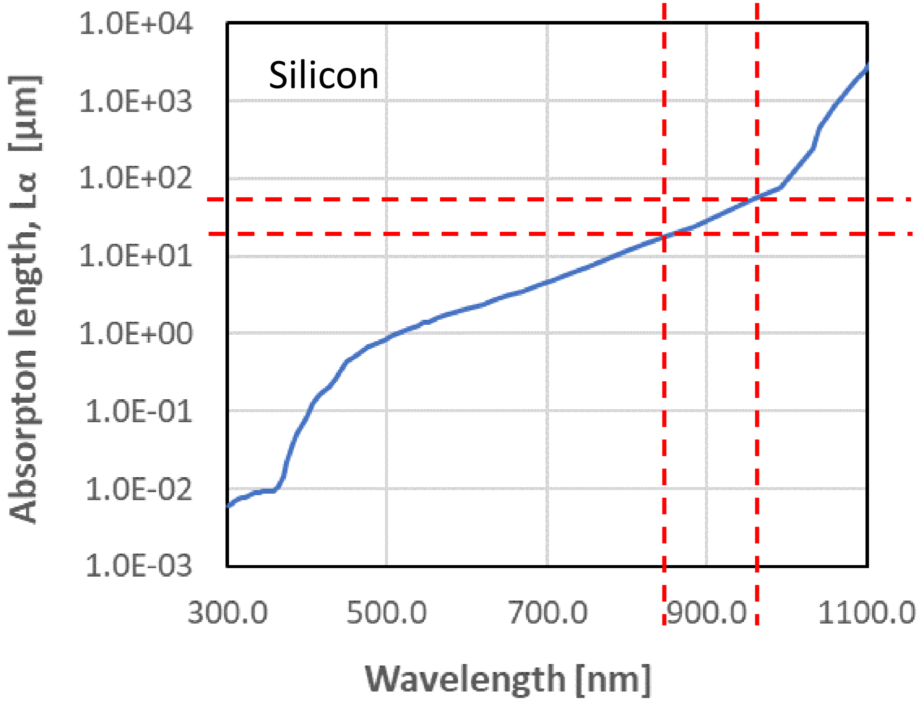
Dark Count Rate (DCR) increase in CMOS SPADs with 43 x 45 um^2 active area

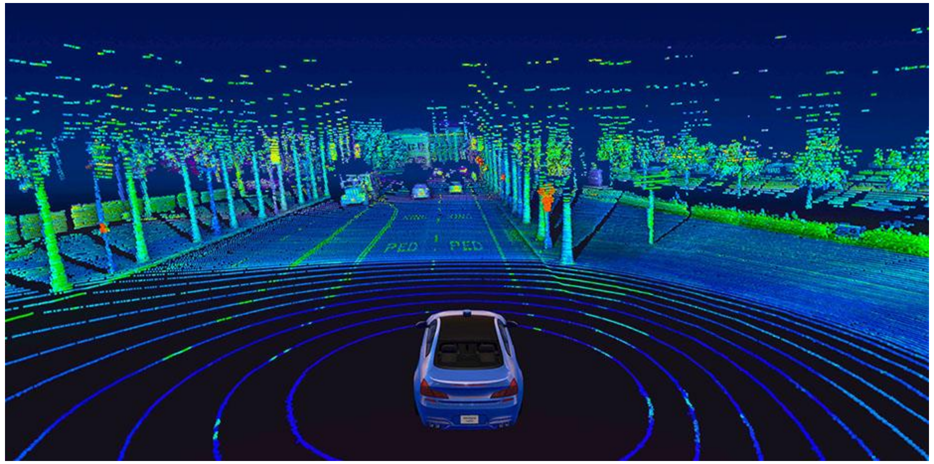


L. Ratti et al., IEEE Tran. Electron Dev., Vol. 66, No. 12, Dec. 2019

Looking at industrial developments: LIDAR

- LIDAR requirements and approaches: synergy with time-resolved particle detection
- IR wavelengths: 850-940nm: requires 20 – 50um active silicon substrate for efficient detection: thick epitaxial layers
- Time of Flight: 66 ps time resolution = 1cm distance resolution
- Several CMOS foundries introduced process modifications to obtain fast charge collection by drift





https://velodynelidar.com/