Subsystem	Target	Equipment
Detector 6hr 15min	▪ LYRA new production batch; ▪ ASIC Functionalities; ▪ SDD Performances; ▪ GAGG Performances;	○ Test Equipment (ARTY) and test pulser; ○ Custom interface for TE; ○ HV and LV lab. generator; ○ SW for Quick Look/data analysis; ○ Radioactive sources (241Am, 137Cs); ○ HERMES breadboards (1&2);

The Integration/Verification on DETECTOR sub-system is operated on the integrated HERMES detector, including FEE PCB, LYRA-FE and LYRA-BE ASICs, SDDs matrix and GAGG crystals, assembled together. The Detector will be connected to the TE through custom interface (to be realized).

Test Set-up (15 min):
FEE PCB connection with:
- HV and LV lab. Generator;
- TE;
- Pulser for test;
- Oscilloscope;
- Acquisition system;

At this stage all the components listed above represent the Detector-EGSE.

LYRA new production batch (1 hr):
- Integration of packaged LYRA-BE on breadboard #1;
- Power-on Detector-EGSE;
- Check LYRA-BE general configuration for:
- Check LYRA-BE low Main Threshold with test pulse;
- Integration of naked LYRA-BE and LYRA-FE on breadboard #2;
- Proceed with next steps;

ASIC functionalities (1 hr):
- Power-on Detector-EGSE;
- Check LYRA – FE:
    - Power consumption on 2V line;
    - Power consumption on 3V3 lines;
- Check proper LYRA-BE configuration for:
    - Shaping time according to LYRA-FE shaping hardware configuration;
    - Baseline DC value according to the selectable voltage;
    - Shaper out;
    - Stretcher out;
    - Main Threshold;
    - Fine Threshold (few channel);
    - DAC Reset (low, nominal, high);
    - Single trigger configuration;

    - OR-Trigger configuration;
    - …
- Check ASIC performance
    - Amplitude of a test signal (i.e: 17000 el. equivalent to the 60 keV of 241Am)
    - Check the gain and linearity with two-pulse signal on C_{test}

SDD Performances (2 hr):

- Power-on Detector-EGSE;
- Configure LYRA-BE in OR-trigger with proper Main threshold;
- Place 241Am (TBD how) on the top of the P/L;
- Stop acquisition after TBD events acquired;
- Analyse data to verify performances;

GAGG Performances (2 hr):

- Power-on Detector-EGSE;
- Configure LYRA-BE in OR-trigger with proper Main threshold;
- Place 137Cs (TBD how) on the top of the P/L;
- Stop acquisition after TBD events acquired;
- Analyse data to verify performances;

Subsystem	Target	Equipment
BEE 4hr 15min	▪ TC interpretation; ▪ HK generation; ▪ TM generation; ▪ Single Event Time Tagging; ▪ ….	○ Detector Emulator (breadboard); ○ iOCB Emulator; ○ LV lab. Generator; ○ PPS Emulator; ○ SW for Quick Look/data analysis;

The Integration/Verification on BEE sub-system is operated on the integrated HERMES BEE, including FPGA, ADC, AtomicClock, … and custom firmware assembled together. The BEE will be connected to the TE through custom interface (to be realized).
At this stage to verify functionalities of BEE

Test Set-up (15 min):
BEE PCB connection with:
- LV lab. Generator;
- Pulser for PPS Emulator;
- Test Pulse for electrical calibration;
- Oscilloscope;
- Acquisition system as PDHU Emulator;
- …

At this stage all the components listed above represent the BEE-EGSE.

TC interpretation (1 hr):
- Power-on BEE-EGSE;
- Verify proper automatic start-up at BEE power-on (e.g. HK generation);
- Send on I2C interface the TC for:
    - ASIC configuration (check TBD – "serial in" line monitoring);
    - Power-Safe Operative-Mode (check monitor power absorption);
    - Test Operative-Mode (check TBD);
    - Observation Operative Mode (check TBD);
    - …

HK generation (1 hr):
- Power-on BEE-EGSE;
- Verify proper automatic start-up at BEE power-on (check TBD – power absorption?);
- Check on :
    - HK type 1 generation;
    - HK type 2 generation;
    - HK type 3 generation;
    - …
- Verify HK values are consistent with real data;

TM generation (1 hr):
- Power-on BEE-EGSE;

- Verify proper automatic start-up at BEE power-on (check TBD – power absorption?);
- Check on:
    - HK type 1 generation;
    - HK type 2 generation;
    - HK type 3 generation;
    - …
- Check on TBD interface:
    - TM packet generation for HK type 1;
    - TM packet generation for HK type 2;
    - TM packet generation for HK type 3;
    - …

- Verify TM data packet is consistent with real data;

Single Event Time Tagging (1 hr):

- Power-on BEE-EGSE;
- Verify proper automatic start-up at BEE power-on (check TBD – power absorption?);
- Simulate LYRA-BE trigger output with external Pulser using simple and complex (multiple) sequence;
- Verify (TBD how) that the Single Event Time Tagging is consistent with real data;

Subsystem	Target	Equipment
PSU 3hr 15min	▪ LV Power on-off verification; ▪ HV Ramp-up/down verification; ▪ Complete procedure for detector switch on/off verification (TBV); ▪ Latch-up circuit verification;	○ LV lab. Generator; ○ Latch-up "stimulus"/simulator; ○ Artificial FEE load simulator;

The Integration/Verification on PSU sub-system is operated on the integrated HERMES BEE, including LV regulators for 2V and 3V3 filtered lines, HV (i.e. 150V) generator, latch-up circuitry, … The PSU will be connected to the necessary equipment through custom interface (to be realized).

Test Set-up (15 min):
PSU connection with:

- LV lab. Generator to simulate S/C power lines for 5V and 12V (others?);
- Latch-up "stimulus"/simulator;
- Artificial resistor capacitor/resistor load simulating the FEE connected;
- …

At this stage all the components listed above represent the PSU-EGSE.

LV Power on-off verification (1hr):

- Power-on PSU-EGSE;
- Connect the artificial FEE load (resistor/capacitor) simulator on 2V and 3V3 lines;
- Connect the artificial BEE load (resistor/capacitor) simulator on 3V3 and XXX lines;
- Verify that the FEE 2V (both input and output) power consumption and stability (?) is as expected;
- Verify that the FEE 3V3 (both input and output) power consumption and stability (?) is as expected;
- Verify that the BEE 3V3 (both input and output) power consumption and stability (?) is as expected;
- Verify that the BEE XXX (both input and output) power consumption and stability (?) is as expected;
- …

HV Ramp-up/down verification (1hr):

- Power-on PSU-EGSE;
- Connect the artificial HV load (resistor/capacitor) simulator;
- Verify that the HV (both input and output) power consumption and stability (?) is as expected at the nominal value (i.e 120V);
- Verify that the HV ramp-up and ramp-down duration is as expected with nominal load;
- Verify that the HV ramp-up and ramp-down duration is as expected with lower load simulating to loose some SDD matrix interconnection;

Latch-up circuit verification (1hr):

- Power-on PSU-EGSE;
- Connect the artificial LV FEE load (resistor/capacitor) simulator;
- Power-on FEE lines;
- Simulate artificial latch-up event using Latch-up simulator;
- Verify that the reaction time of the latch-up circuit is as expected on different lines;
- Verify that Alert for Latch-up event is properly generated (?);

Subsystem	Target	Equipment
PDHU 9hr 15min + TBD hr for scientific SW	▪ TC interpretation; ▪ PSU commanding; ▪ BEE commanding; ▪ Operative modes; ▪ Alert procedures; ▪ TM packets generation; ▪ Scientific on-board SW ▪ Scientific data handling	○ LV lab. Generator; ○ P/L & S/C simulator ; ○ Desktop/labtop computer with ISIS-SDK ○ Cables and connectors. ○ Computer display ○ Optional: Osciloscope.

The Integration/Verification on PDHU sub-system is operated on the iOBC board. The main preparation activity on HERMES PDHU concern the daughter board and the development of the on board SW. Custom interfaces have to be realized.

Test Set-up (15 min):
PDHU connection with:
- LV lab. Generator;
- P/L & S/C simulator.
- Running the ISIS-Software Development Kit(SDK).

At this stage all the components listed above represent the PDHU-EGSE.

TC interpretation (1hr):
- Power-on PDHU-EGSE;
- Tx of TC from the PDHU-EGSE;
- Acknowledge response from the PDHU;
- CRC calculations;
- Repeat for all TCs;

PSU commanding (1hr):
- Power-on PDHU-EGSE;
- Toggle on/off the voltage switches for the PSU;
- Confirmation of the on/off status from the PDHU-EGSE;
- Monitoring the switches lines with the oscilloscope;
- Repeat for all voltage switches;

BEE commanding(2hr):
- Power-on PDHU-EGSE;
- Tx of commands to PDHU-EGSE;
- Rx of PDHU-EGSE responses;
- Display of Rx response on the debug interface (PC);

Operative modes (2hr):
- Power-on PDHU-EGSE;
- Tx of mode change TC from PDHU-EGSE;
- Acknowledge response from the PDHU;
- Repeat for all modes (specific responses should be tailored for each mode);

Alert procedures (1hr):

- Power-on PDHU-EGSE;
- PDHU-EGSE emulates an alert signal;
- PDHU acknowledges the alert and reports it to user;

TM packets generation (2hr):

- Power-on PDHU-EGSE;
- PDHU-EGSE sends a simulated HK and telemetry data via the SPI;
- PDHU processes it and generates the TM packet including the analog readings;
- PDHU shows the contents of the TM packet to the user;

Scientific on-board SW (X hr):

- PDHU-EGSE sends simulated events via the SPI.
- PDHU receives and processes the events.
- Statistics and burst search algorithms run on simulated packets.
- Scientific data saved to SD-Card.

Scientific-data handling (Y hr):

- Power-on PDHU-EGSE;
- Send a simulated “Transmit scientific data” command;
- PDHU responds sending mock-up scientific data saved to the SD-card via the SPI;