Single Subsystem integration/verification
READY
TO BE PROCURED

Subsystem	Target	Equipment
Detector 6hr 15min	▪ LYRA new production batch; ▪ ASIC Functionalities; ▪ SDD Performances; ▪ GAGG Performances;	○ Test Equipment (ARTY) and test pulser; ○ Custom interface for TE; ○ HV and LV lab. generator; ○ SW for Quick Look/data analysis; ○ Radioactive sources (241Am, 137Cs); ○ HERMES breadboards (1&2);
BEE 4hr 15min	▪ TC interpretation; ▪ HK generation; ▪ TM generation; ▪ Single Event Time Tagging; ▪ ….	○ Detector Emulator (breadboards); ○ iOCB Emulator; ○ LV lab. Generator; ○ PPS Emulator; ○ SW for Quick Look/data analysis;
PSU 3hr 15min	▪ LV Power on-off verification; ▪ HV Ramp-up/down verification; ▪ Complete procedure for detector switch on/off verification (TBV); ▪ Latch-up circuit verification;	○ LV lab. Generator; ○ Latch-up “stimulus”/simulator; ○ Artificial FEE load simulator;
PDHU 9hr 15min + TBD for SW	▪ TC interpretation; ▪ PSU commanding; ▪ BEE commanding; ▪ Operative modes; ▪ Alert procedures; ▪ TM packets generation; ▪ Scientific on-board SW; ▪ Scientific data handling	○ LV lab. Generator; ○ P/L & S/C simulator; ○ Desktop/labtop computer with ISIS-SDK; ○ Cables and connectors; ○ Computer display; ○ Optional: Osciloscope;

In this phase the main functionalities of single sub-systems (Detector, BEE, PSU, PDHU) will be verified. This activity is preliminary to the following one-by-one sub-system integration/verification (see next pages).
The current table, mostly incomplete, shall be filled including all main functionalities that need to be verified, including the necessary equipment necessary to carry out tests.
The use of breadboards and/or simulators is strongly recommended.
Please, an indication on the estimated time for each single functionality check is warmly required.

One-by-one Subsystem integration/verification
READY
TO BE PROCURED

Subsystem	Target	Material
BEE PSU TBD time	▪ BEE proper PSU commanding; ▪ Complete procedure for Detector switch on/off verification; ▪ Complete Latch-up procedure verification (Safe-Mode);	○ LV lab. generator; ○ SW for Quick Look/data analysis; ○ Latch-up "stimulus"/simulator;
BEE FEE TBD time	▪ FEE configuration; ▪ Detector operation; ▪ SDD Performance; ▪ Monitoring and HK generation; ▪ Single Event Time Tagging; ▪ Data Package generation (e.g. HK, event list);	○ LV lab. Generator; ○ PPS Emulator; ○ SW for Quick Look/data analysis;
PDHU BEE TBD time	▪ TM/TC generation; ▪ Alert generation; ▪ Operative modes; ▪ BEE operation; ▪ …	○ LV lab. Generator; ○ Latch-up "stimulus"/simulator; ○ SW for Quick Look/data analysis;
PDHU PSU TBD time	▪ Toggle voltages switches ▪ Reading of voltages status	○ LV lab. Generator; ○ Latch-up "stimulus"/simulator(?); ○ ….

In this phase, after the subsystem stand-alone verification phase, the focus is on the one-by-one interconnection. The main topic is to check the correct configuration and the proper operation of each pair of interconnected sub-systems.
For what concerns the integration of the demonstration module, i.e. the first integrated system, a development phase during integration activity could be taken into account. For this reason BEE-PSU and BEE-FEE are kept separated at this stage and could be simplified for PFM and FM models.
The current table, mostly incomplete, shall be filled including all main functionalities that need to be verified, including the necessary equipment necessary to carry out tests.
The use of breadboards and/or simulators is strongly recommended.
Please, an indication on the estimated time for each single functionality check is warmly required.

Multiple Subsystem integration/verification

READY

TO BE PROCURED

Subsystem	Target	Material
PDHU BEE PSU TBD time	▪ Operative modes (power safe); ▪ Emergency procedures; ▪ …	○ Detector Emulator (breadboards); ○ LV lab. Generator; ○ PPS Emulator; ○ SW for Quick Look/data analysis; ○ Latch-up “stimulus”/simulator;
BEE PSU FEE TBD time	▪ FEE operation; ▪ SDD performances; ▪ …	○ LV lab. generator; ○ PPS Emulator; ○ SW for Quick Look/data analysis; ○ Latch-up “stimulus”/simulator;

READY

TO BE PROCURED

Subsystem	Target	Material
PDHU BEE PSU FEE (i.e. whole payload module) TBD time	▪ Operative modes; ▪ SDD performances; ▪ …	○ Detector Emulator (breadboards); ○ LV lab. Generator; ○ PPS Emulator; ○ SW for Quick Look/data analysis; ○ Latch-up “stimulus”/simulator;