PHOS4BRAIN:
Design and operation of Silicon Photonics optical links, as enabling technology for quantum communications

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Outline

- Introduction
- SiPh devices
- Radiation effects on SiPh devices
- High-speed electronic driver design
- Whole systems tests
- Ongoing activities

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Introduction

- Photonic Integrated Circuits (PIC) are one of the most promising platforms for Quantum computing (e.g. QKD) comprising several optical elements such as – among others – Mach-Zehnder Interferometers (MZI) and Ring Resonators (RR).

- PHOS4BRAIN (PHOtonic Systems for Broad Rad HArd INterconnect), is a project funded by INFN CSN5, with partnership from Department of Information Engineering of University of Pisa, Scuola Superiore S. Anna of Pisa and CERN, to design and operate PIC for high-speed radiation tolerant links. Key to the exploitation of this technology is the ability to drive MZI and RR with suitable electronic circuits.

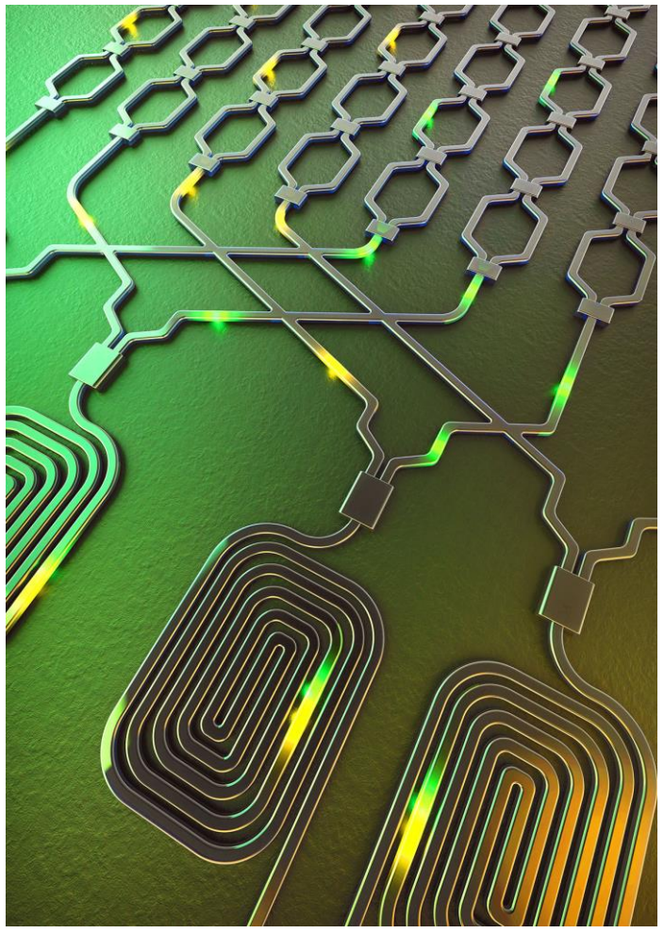

Image: Xiaogang Qiang
University of Bristol

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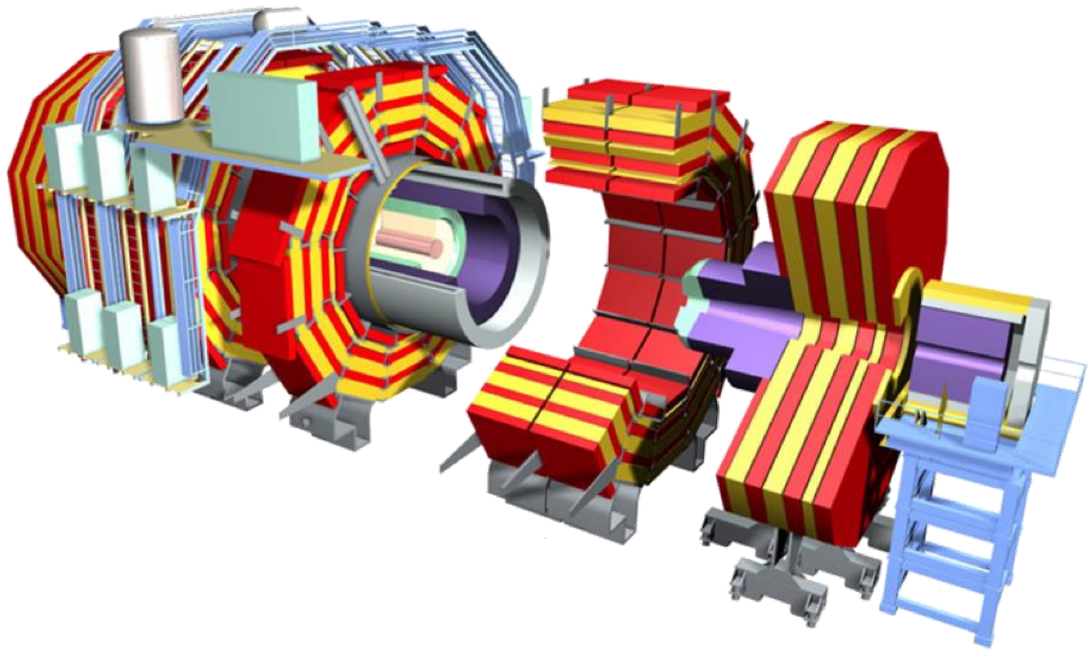
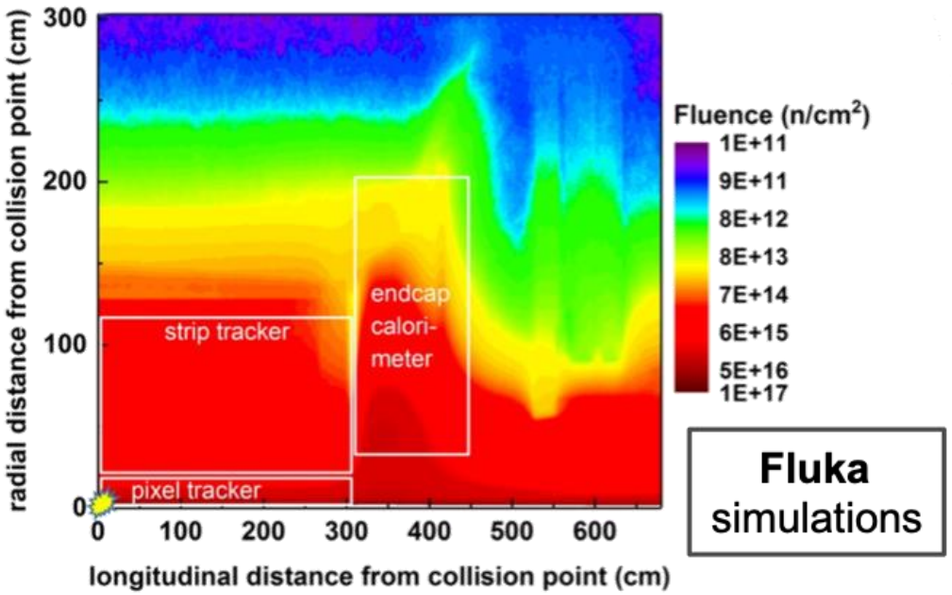
Next generation HEP detectors

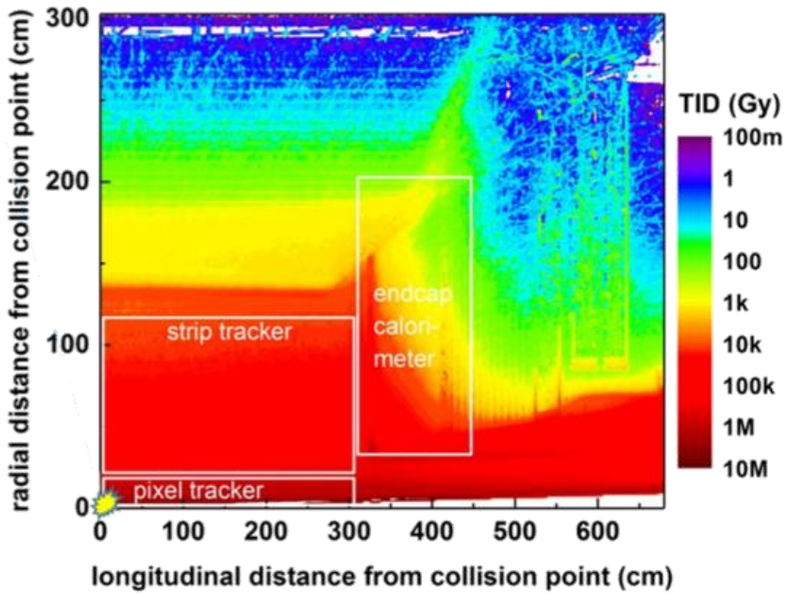
Future colliders (HL-LHC, FCC)

- Increment of radiation levels
- Inner detector rates
  - Few tens of Gb/s

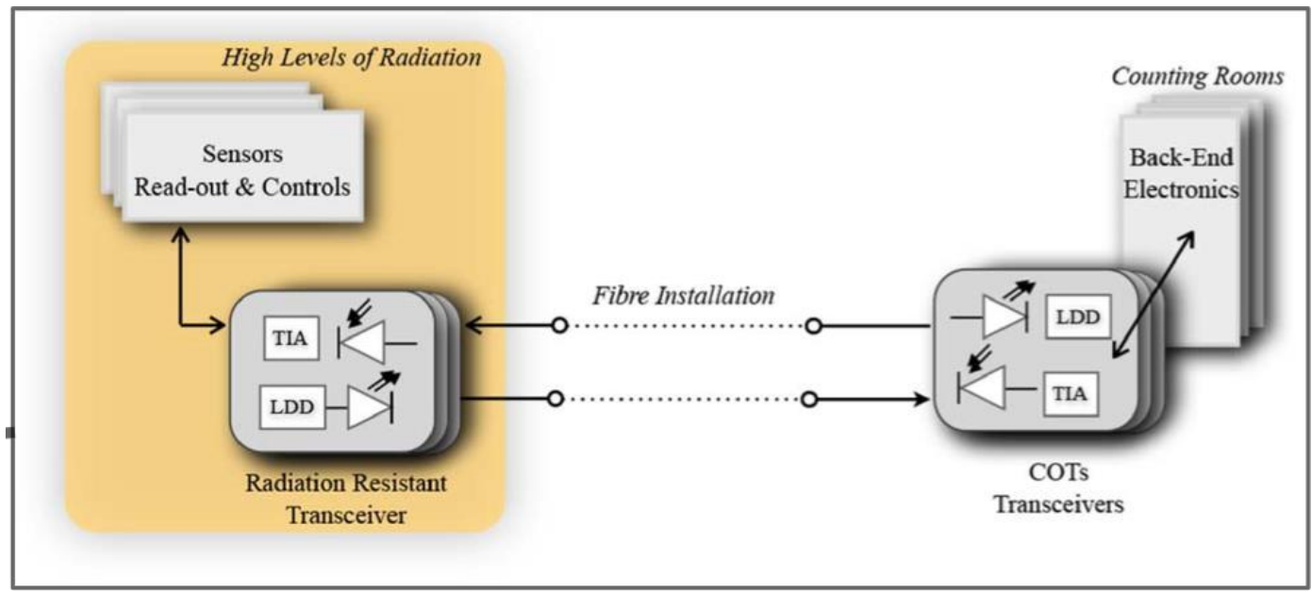




Fluka simulations



Silicon Photonics Rad Hard data links

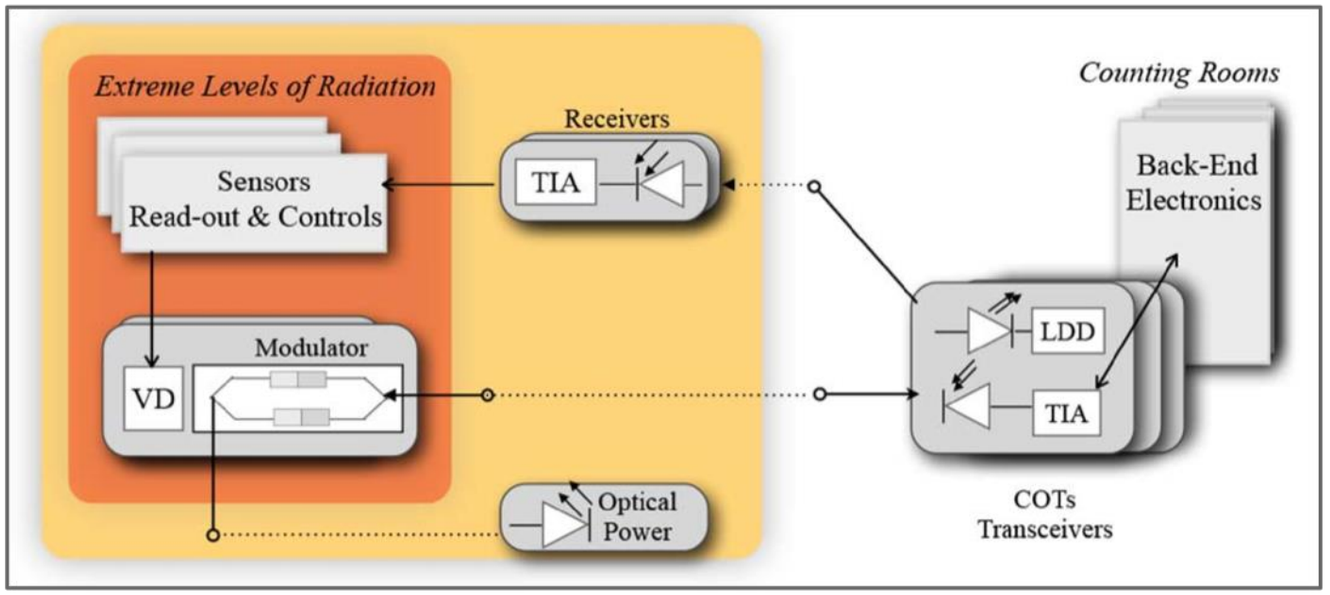


Current (LHC) links

- Based on lasers (VCSEL) inside the radiation zone.
- VCSEL suffer from displacement damage.

Silicon Photonics links

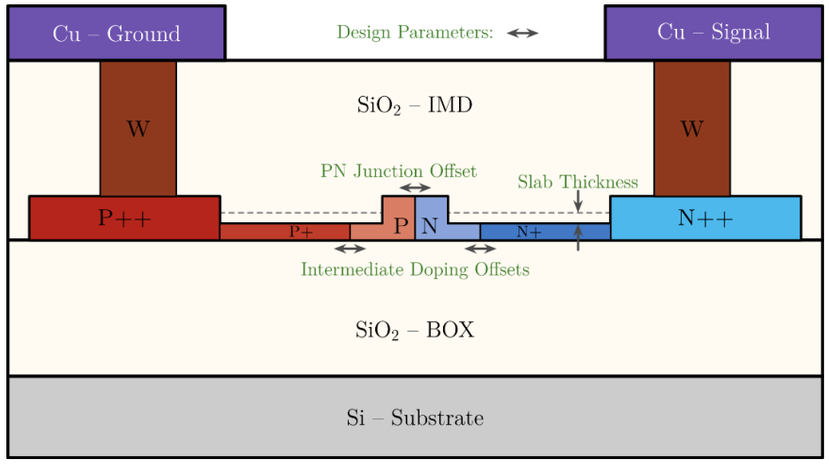
- Based on Modulators (Mach-Zehnder or Ring Resonators), electrically modulated by the front-end.
- Laser light brought in through fibres (generated outside the harshest radiation regions).
- SiPh devices are intrinsically resistant to displacement damage.



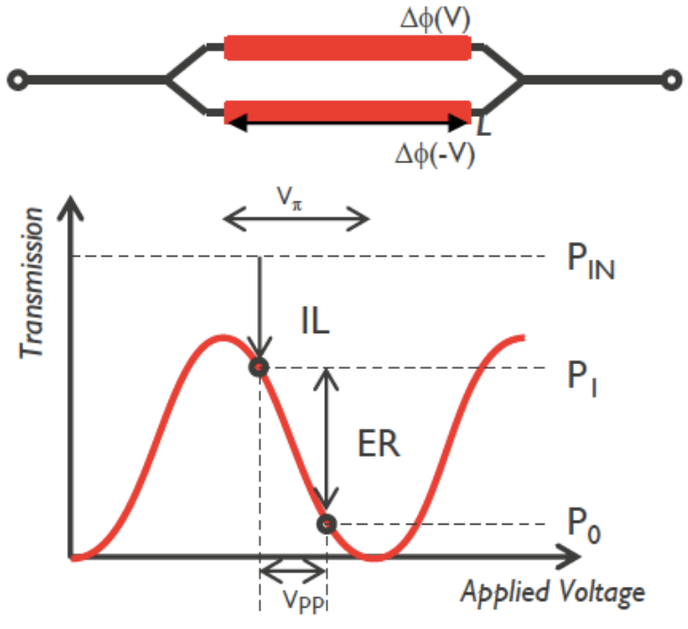
[from S. Seif El Nasr-Storey, et al. «Modeling TID Effects in MZI Silicon Modulators for HL-LHC» IEEE Transactions (2015)]

Silicon Photonics devices

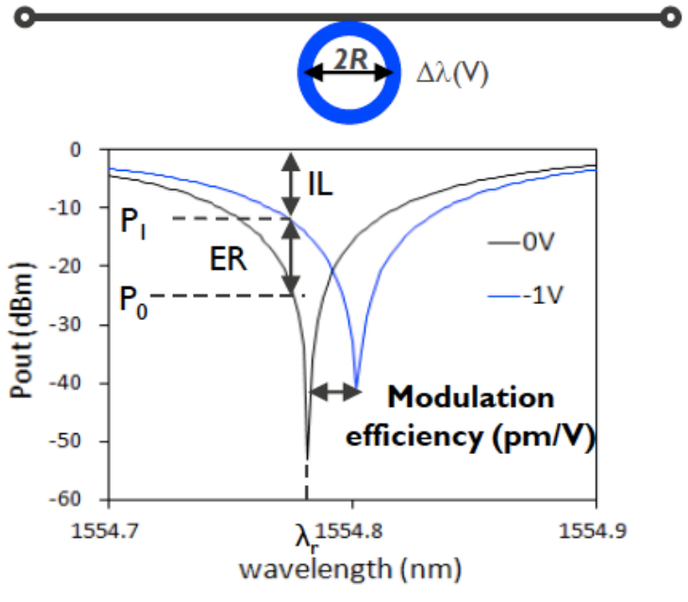
- Free carriers determine local refractive index variations (plasma dispersion effect).
- **Reverse-biased PN junction** embedded in a mono-modal rib waveguide enables to change the **overlap** between charge carriers and propagating optical mode: **voltage-dependent phase shift**



Si Mach-Zehnder Modulator



Si Ring Modulator



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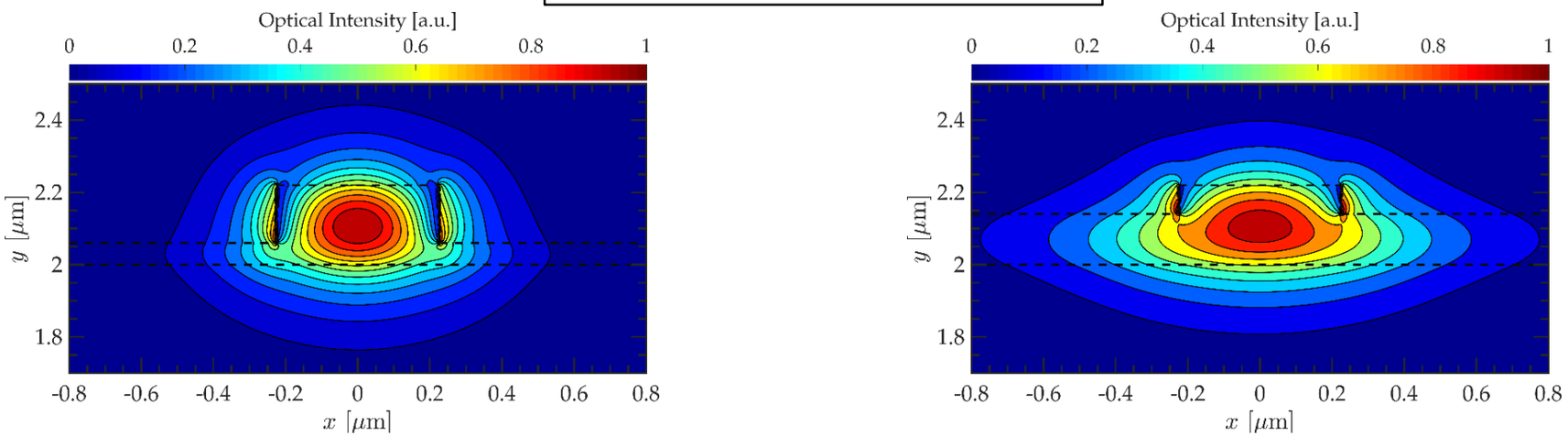
PN junction as base element

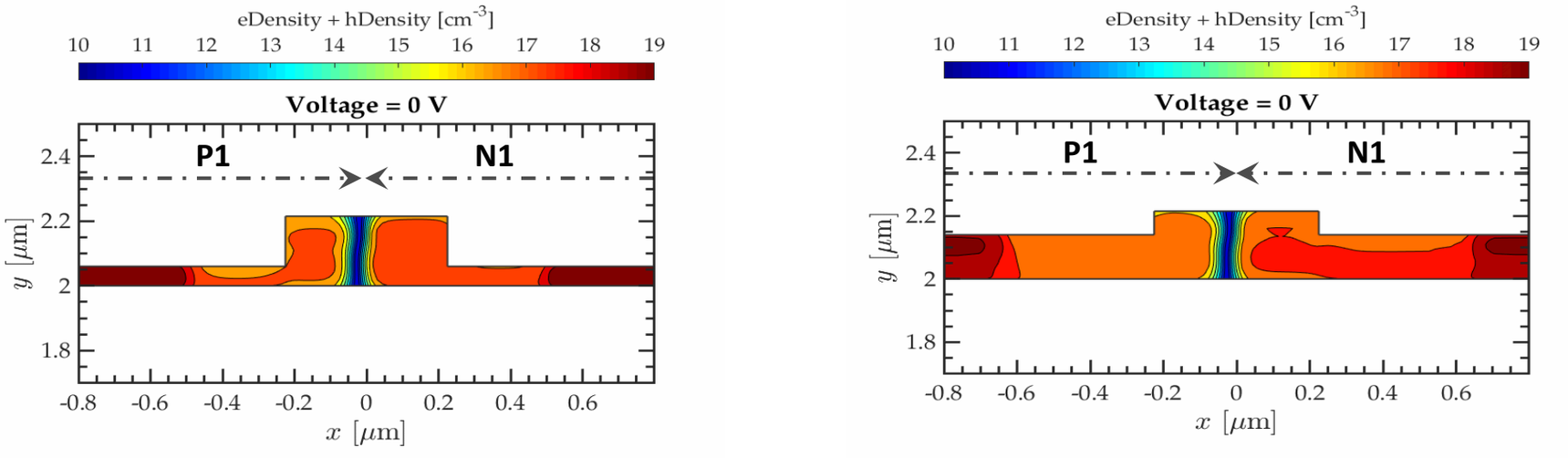
Classic Deep-etched slab

New Shallow-etched slab

Optical mode (λ_0 = 1550 nm)



Free carrier concentrations



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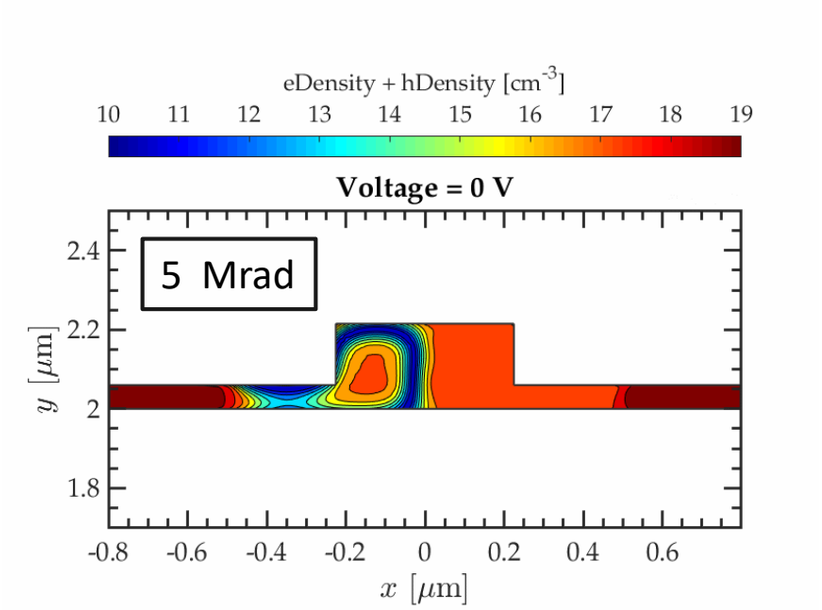
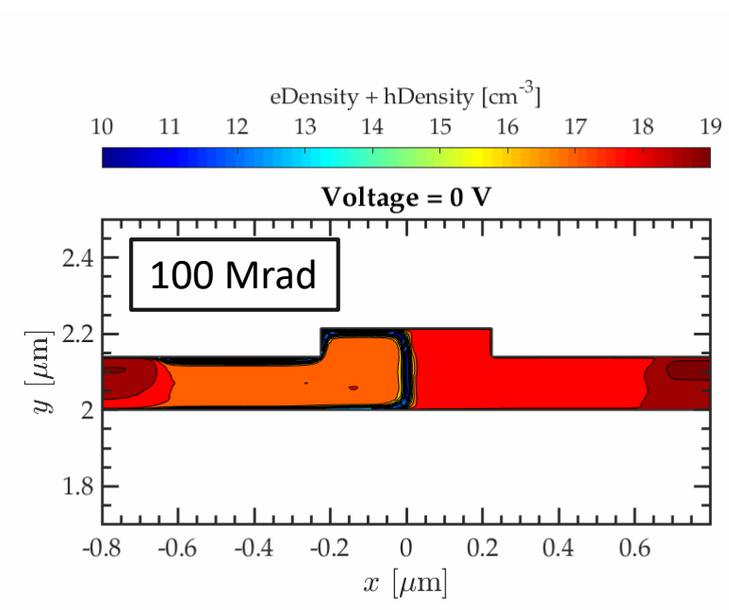
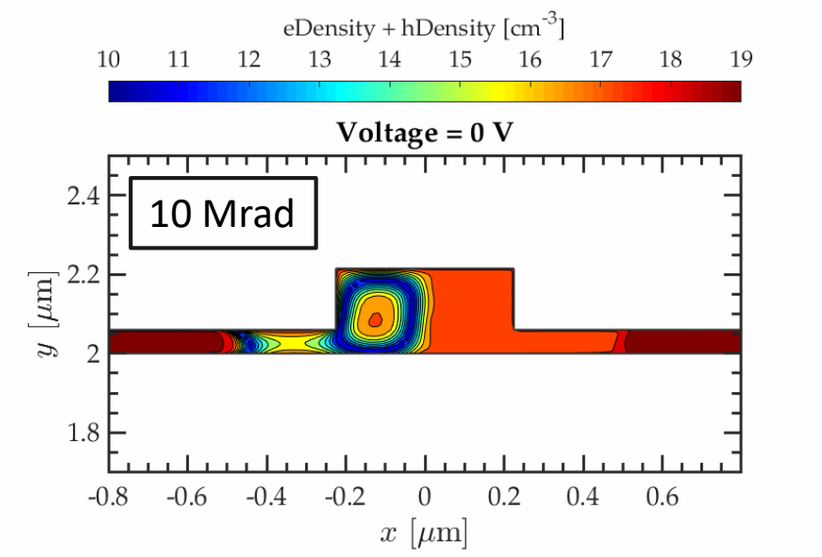
Radiation effects on different structures

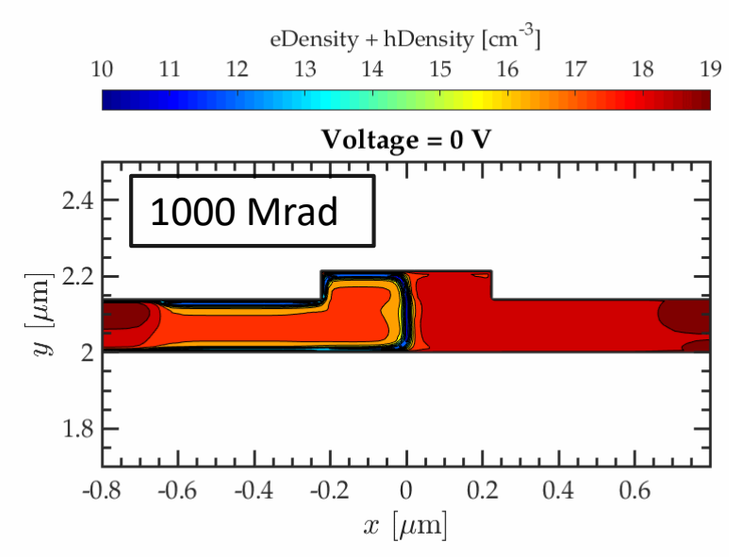
Classic Low-doped Deep-etched device

New High-doped Shallow-etched device









- Ionizing radiation-induced holes remain trapped in deep oxide traps near the Si/SiO2 interface
- The positive charge buildup influences the electrical behavior and determines the pinch-off of the p-doped slab

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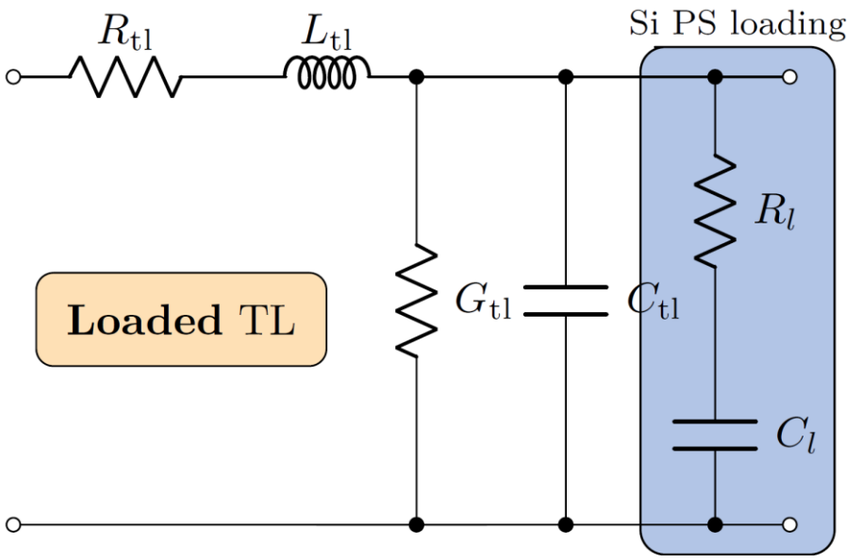
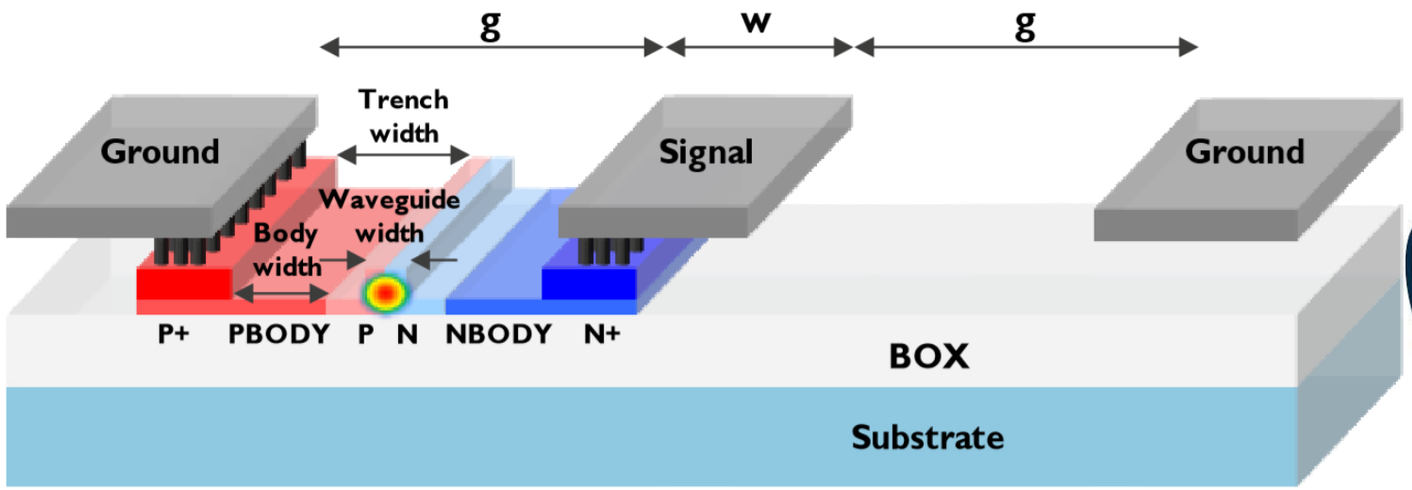
Transmission Line Design

Transmission line model



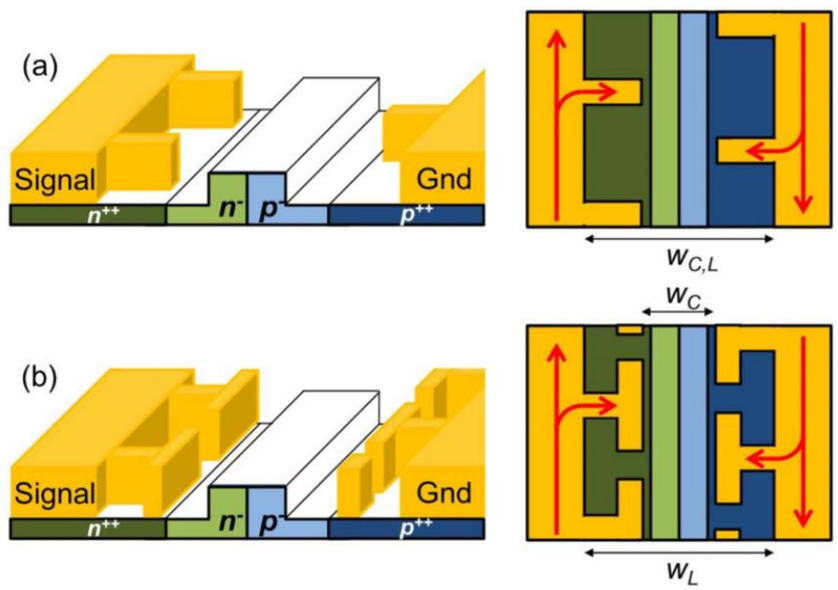


[from M. Rakowski, «Silicon Photonics Platform for 50G Optical Interconnects» (2017)]

Electro-optical modulation bandwidth is limited by:

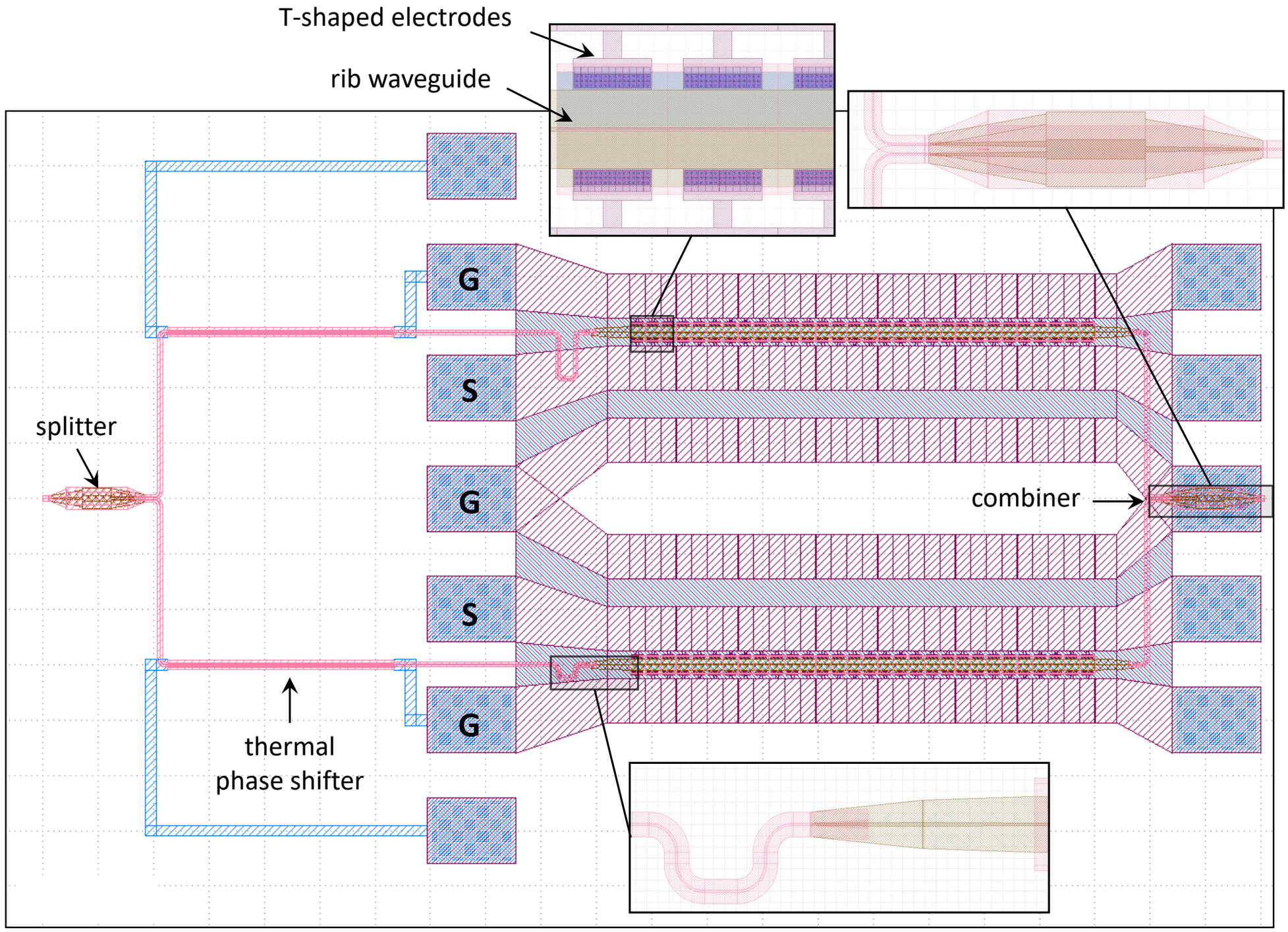
- Microwave attenuation
- Phase matching between optical and RF wave envelopes
- Impedance matching at driver and termination sides

Careful RF design of coplanar metal electrodes is needed



[from J. Witzens, «High-Speed Silicon Photonics Modulators» (2018)]

MZM Layout



- Unbalanced MZM with thermal phase shifters (quadrature tuning).
- Linear metal tapers to adapt phase shifter TLs to pads pitch (100 um).

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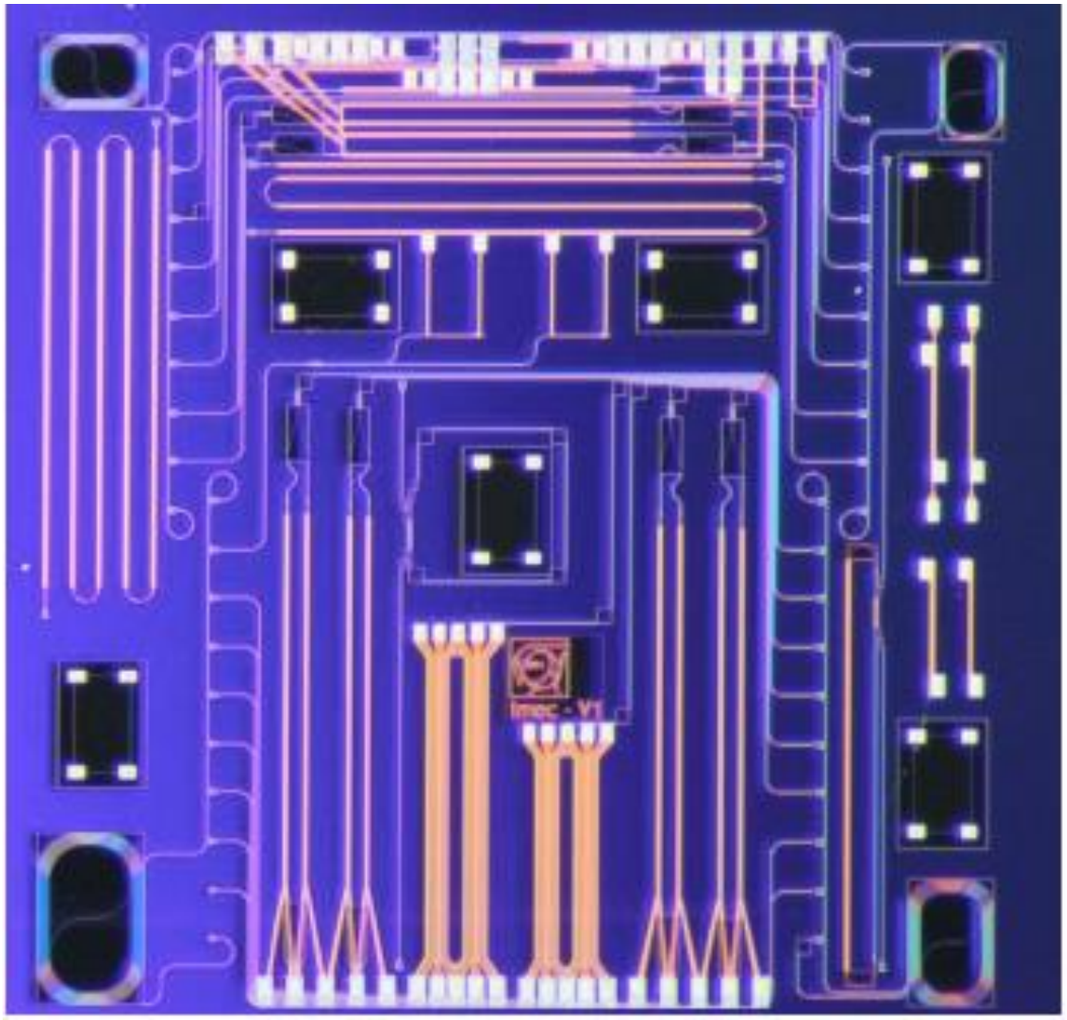
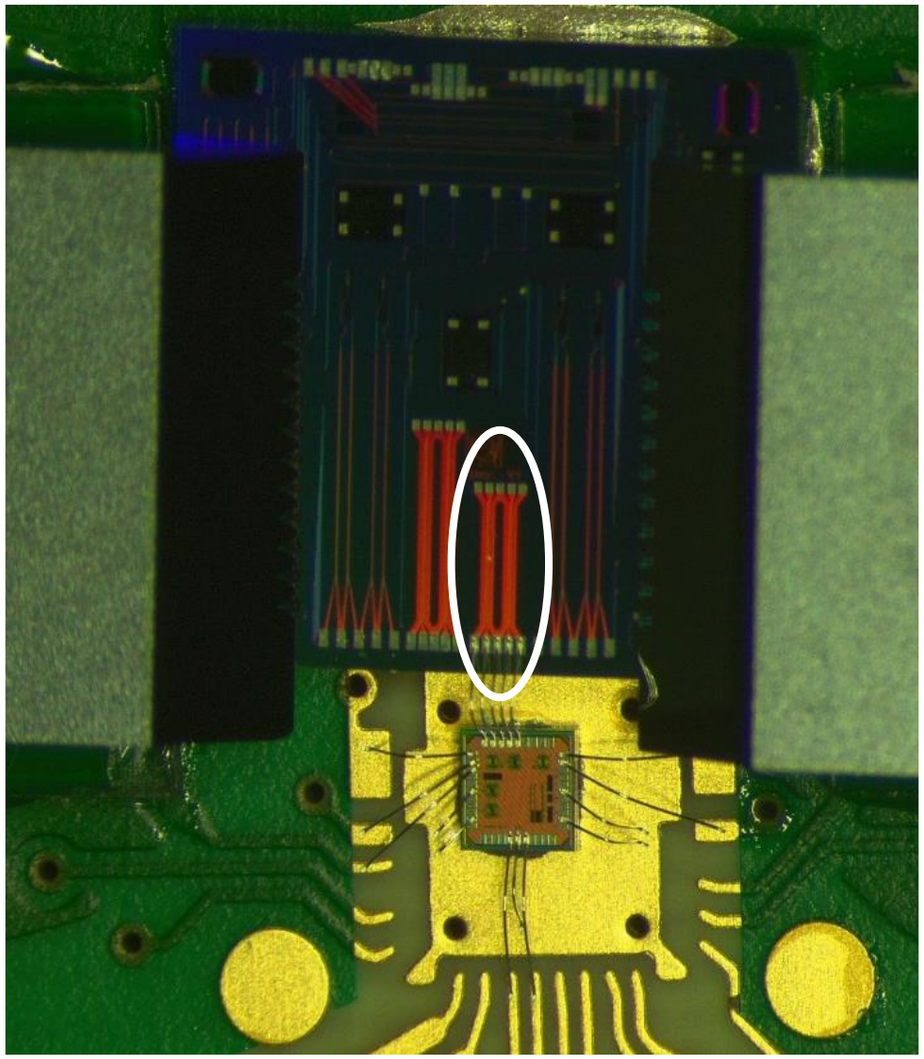
SiPh Modulators and Electronic Drivers



MZM and RR fabricated by IMEC under CERN's design in ISIPP25G technology



MZM and Electronic Driver chips

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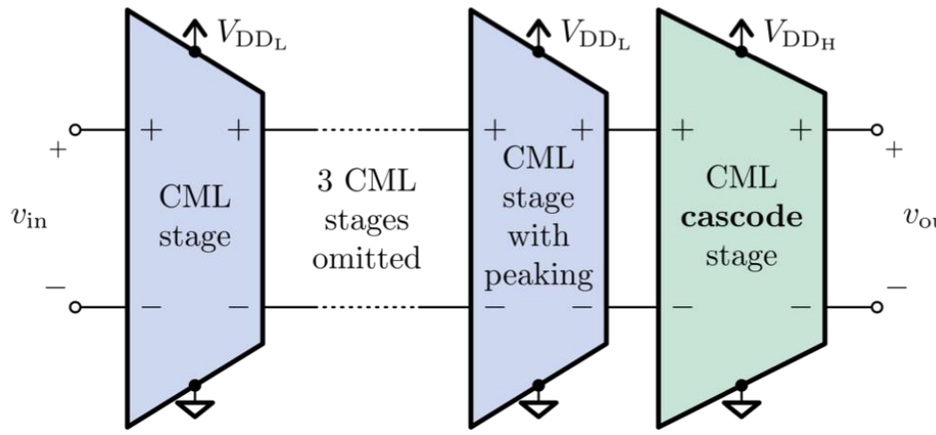
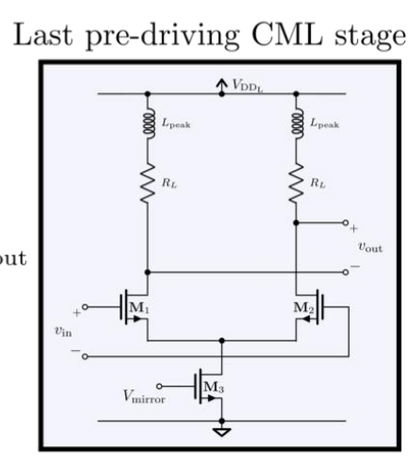
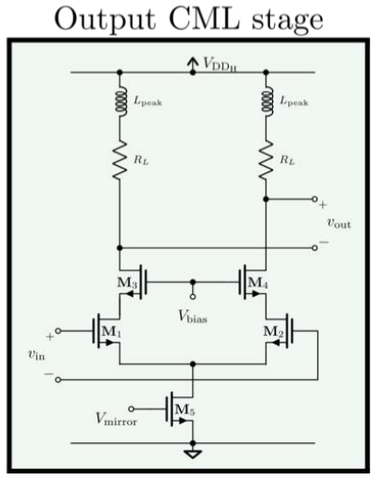
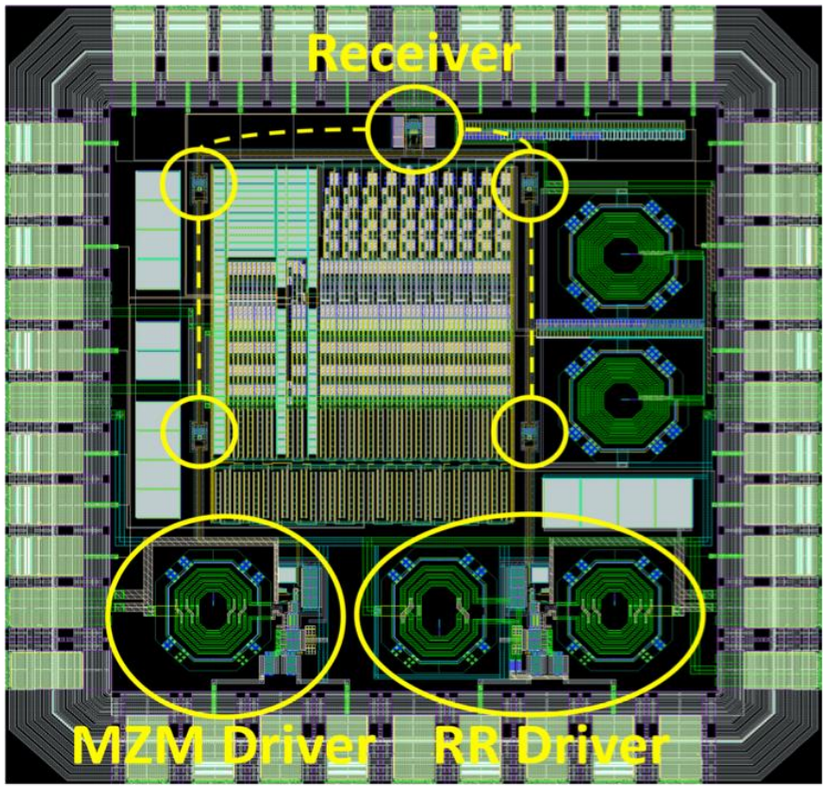
Driver in 65 nm TSMC technology

Driving voltage: above 1 V_{pp} for each arm of the MZM
Speed: 5 Gb/s
Rad Tolerance: HL-LHC compatible

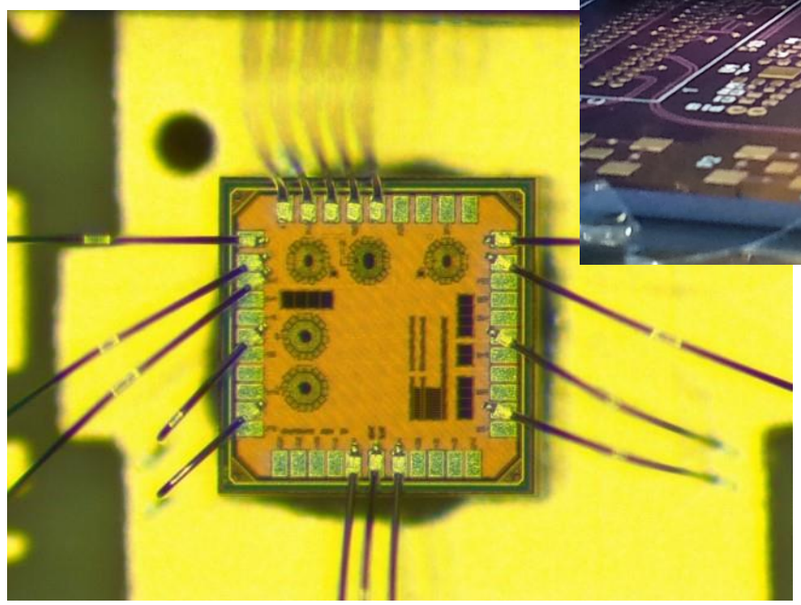


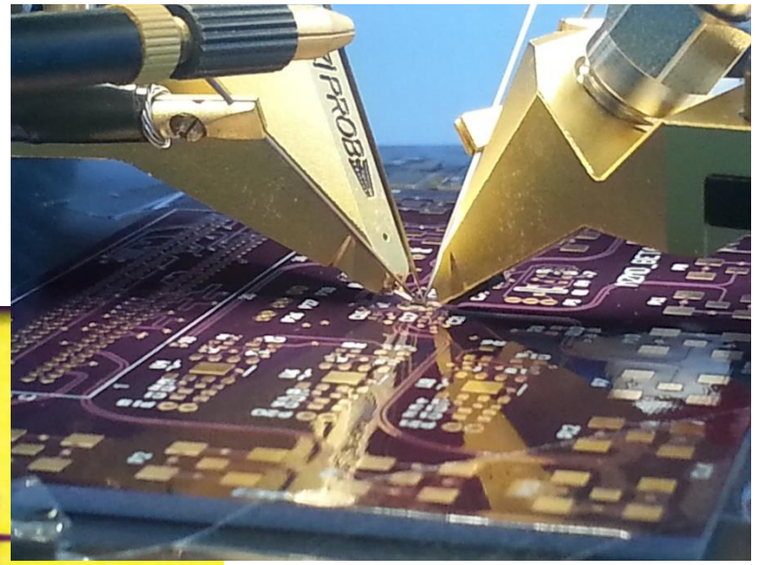




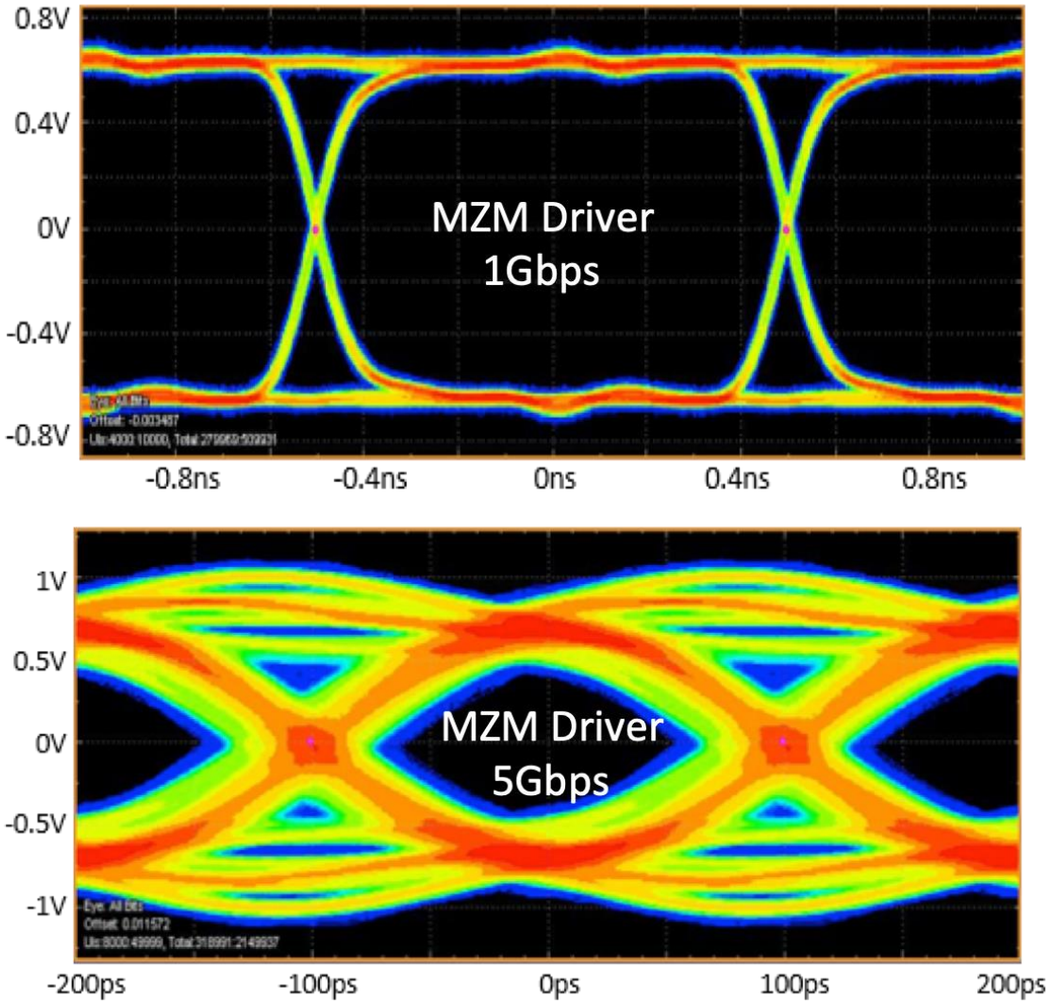


Driver chip fabricated in 2018

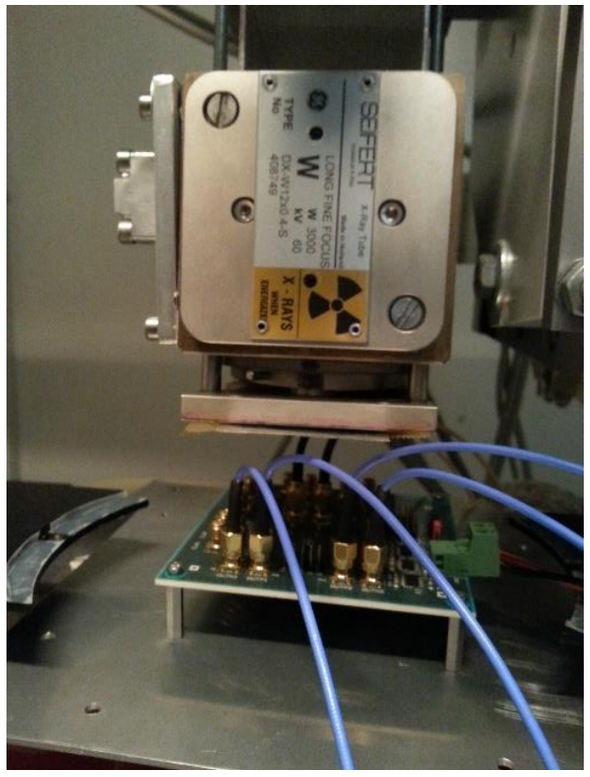


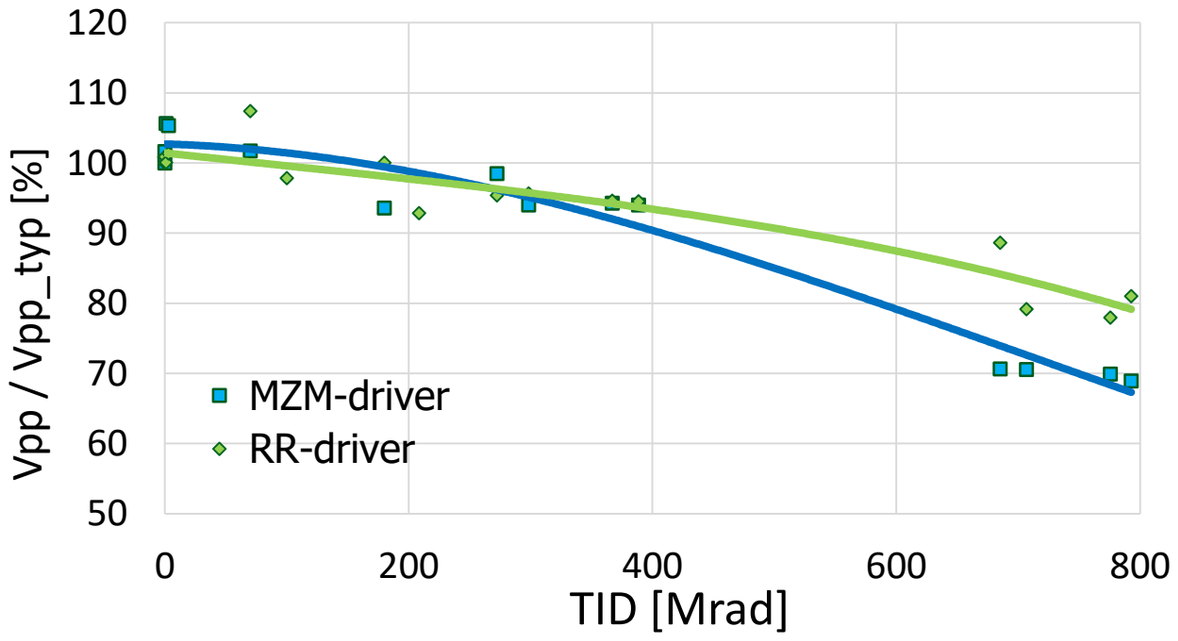


Electrical and TID Measurements



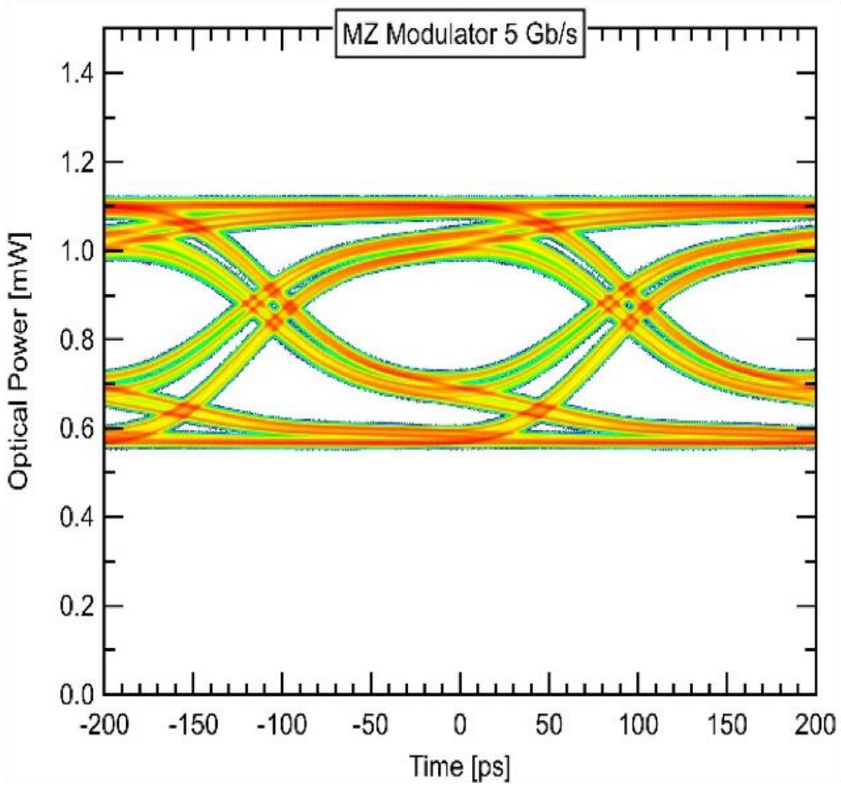
X-ray test at *INFN Padova*



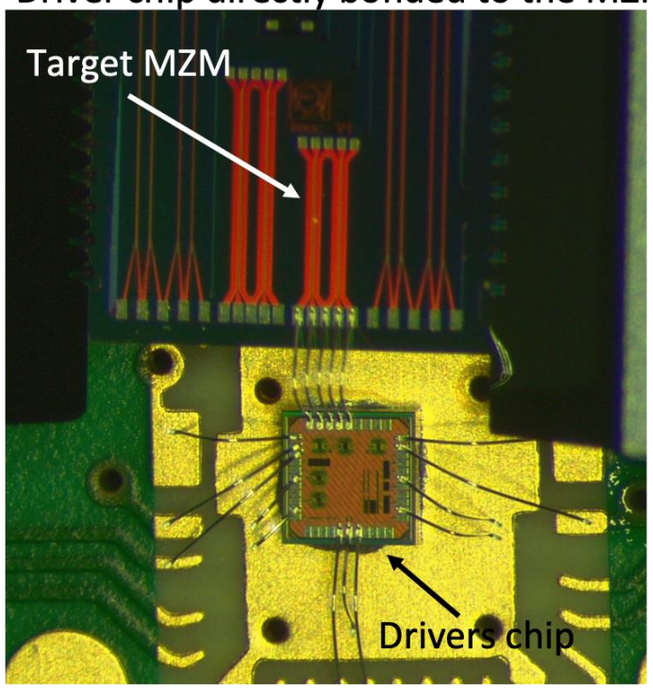


Results of the optical tests

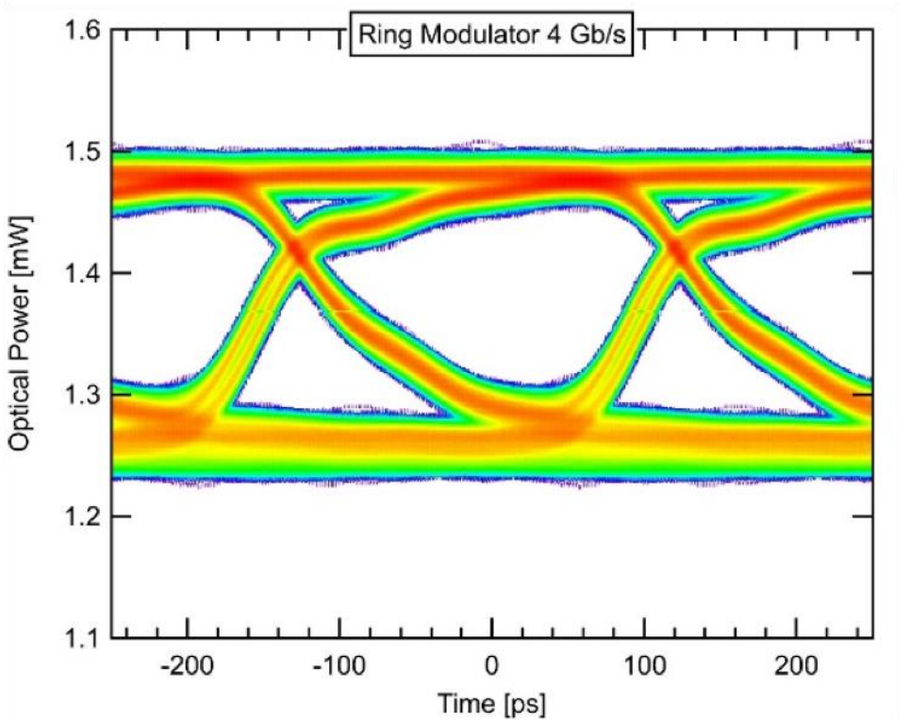
ISIPP25 MZM + Driver



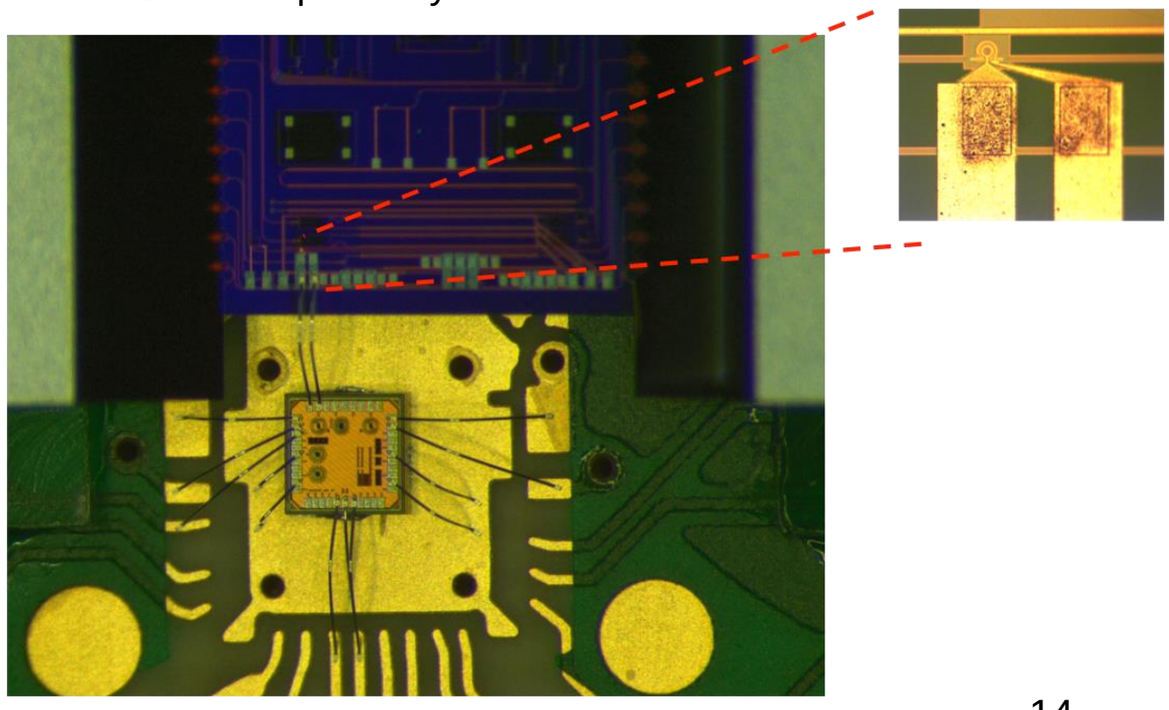
Driver chip directly bonded to the MZM



ISIPP25 RR + Driver



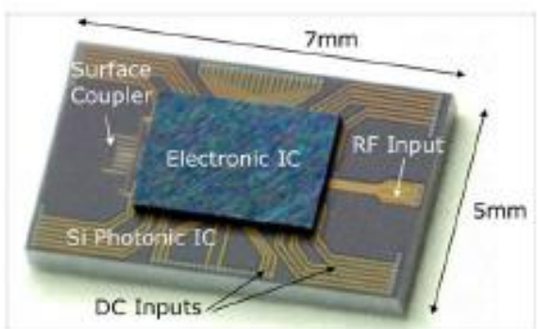
Driver chip directly bonded to the RR



Ongoing activities at Pisa

- Design
  - New Silicon Photonic circuit with MZM and RR in ISIPP50G technology
  - New drivers in 28 nm TSMC technology aiming at 25 Gb/s

- Integration
  - The photonics IC size is generally larger than the electronic IC size
    - Free carrier dispersion modulators are relatively large devices > 1 mm
    - Fiber attachment has a large footprint onto the photonic chip
  - Area on electronic IC is in general more expensive than on PIC
    - Hybrid integration is currently preferred to monolithic integration of electronics and photonics devices
  - Scaling of Photonic IC size might bring advantages for monolithic integration of electronics and photonics.



FABULOUS D4.1.4 Dissemination kit

Thanks for your attention

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