SNRI 2020 :
Laboratory Proposal

Advanced sensors and electronics characterisation

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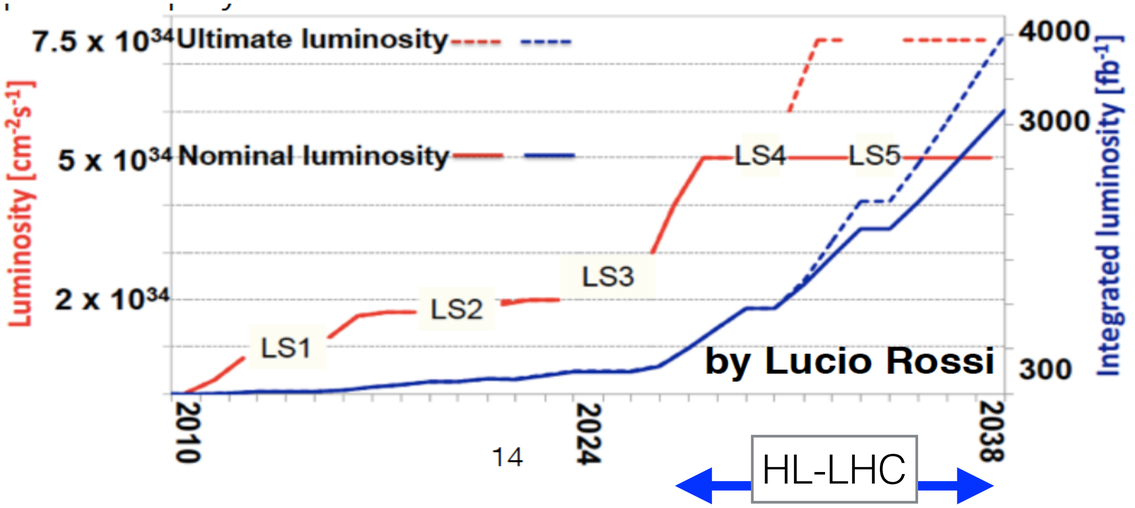
Challenges of HEP for tracking and vertexing in extreme conditions of particles rates and radiation:

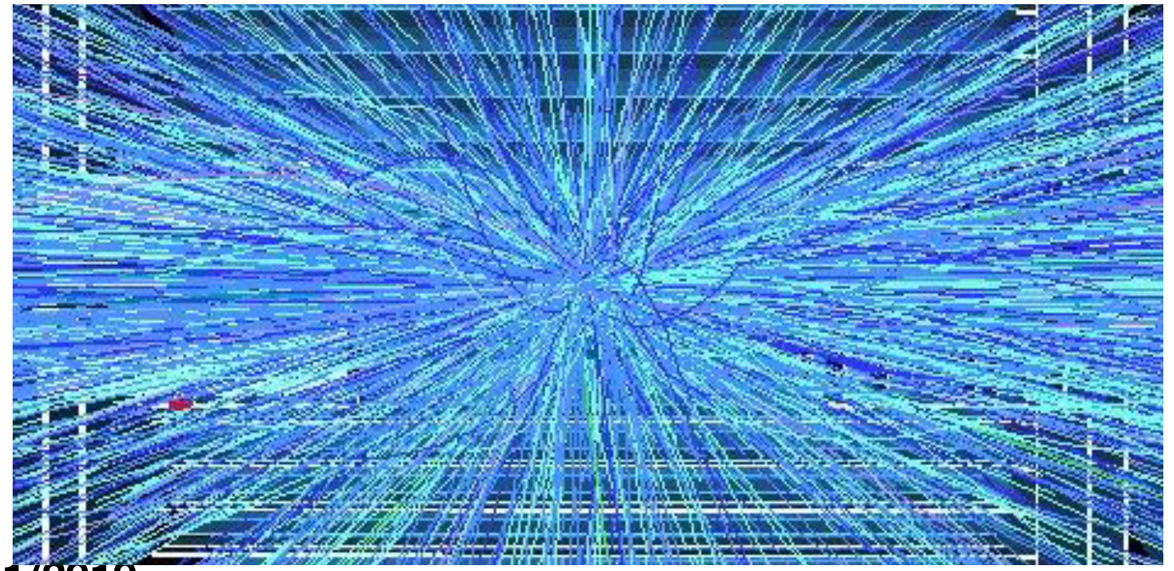
- Context and Principles : challenges and goals achieved
- Lab part-1 - Essential step for building pixel detectors: probe-station testing
- Lab part-2 - Calibration steps to fully characterise electronics wt/wo sensor

Contex: HL_LHC challenge

- High Luminosity LHC, a natural extension of LHC program
  - goal is to reach 3000 fb^{-1} in 10 years
  - x10 LHC Integral Luminosity
  - x5 LHC-0 instant Luminosity (=higher particle flux)
  - x5 LHC PU (140) : now also perspective for x7 PU (200)



A typical HL_LHC event: 140-200 overlapped events



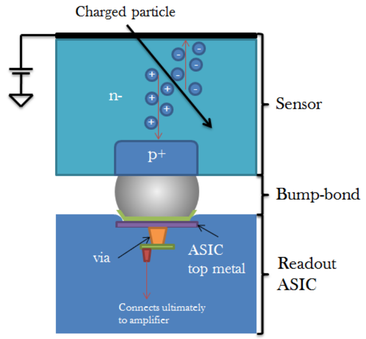
Principle and challenges

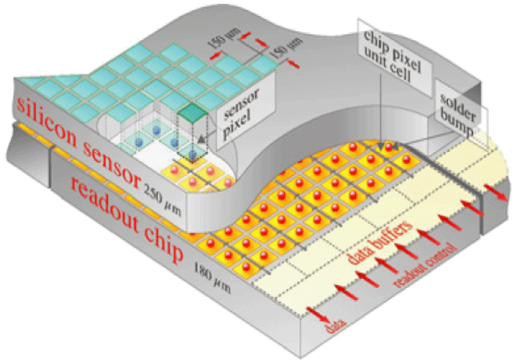
Requirements from HL_LHC experiments :

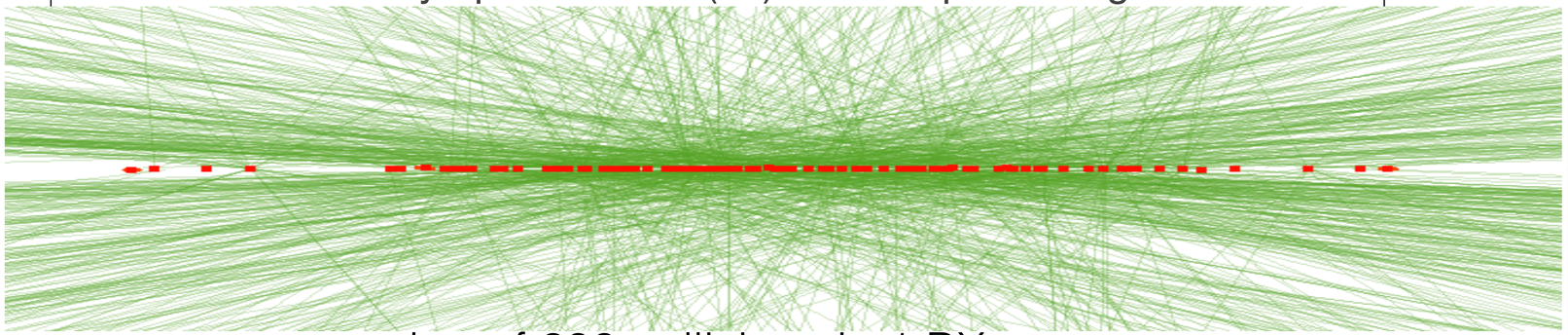
Small pixels: 50x50um^{2}.
Low noise / Low power Front End electronics
Large chips : 2cm x 2cm (~0.5 billion transistors)
Pixel Hit rates: up to 3 GHz/cm^{2} (200 P.U.)
Radiation : 1Grad, 10^{16} n/cm^{2} (unprecedented)

Trigger: up to 1MHz with 12.8us latency
(~100x buffering and readout)
Low power - Low mass systems

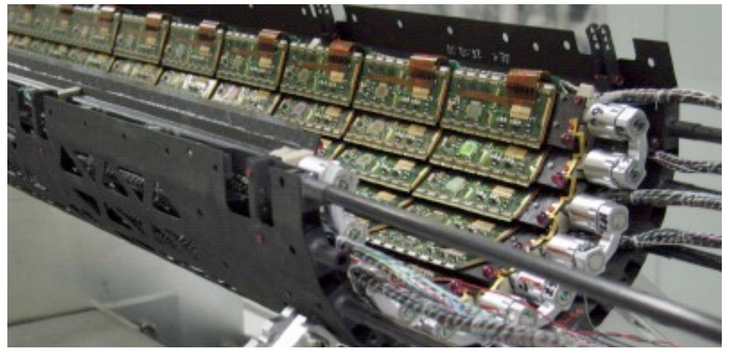
Data readout : up to 4-5 Gbs/s
TRIGGER Latency up to 12.8us (x3) ==> deeper storage buffer





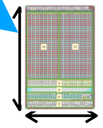


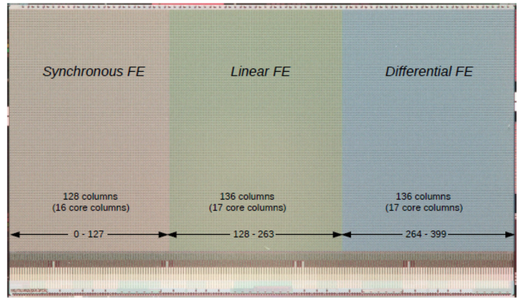
overlap of 200 collisions in 1 BX

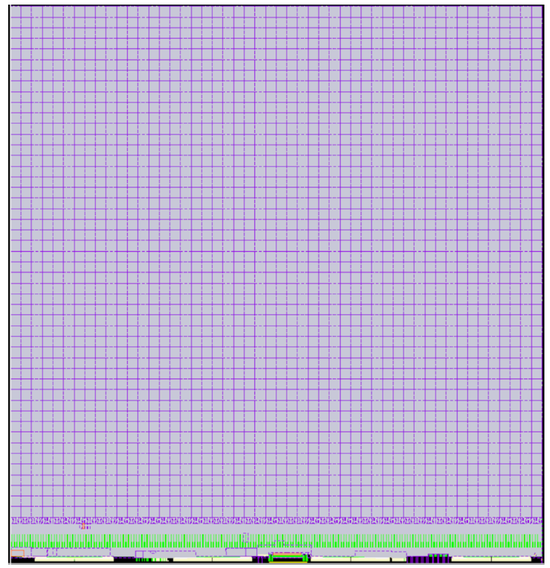


Contex : new generation pixel readout chip in 65nm CMOS technology

- INFN CHIPIX65 project (dimostratore: 2013-2017) 64x64 pixel matrix
  - RD53 Collaboration (RD53A prototype: 2016-2017) 400x192 pixel matrix
    - CMS Pixel Upgrade for HL_LHC (RD53B 2018-2019) 400x400 pixel matrix







12mm² **2cm²** **4cm²**

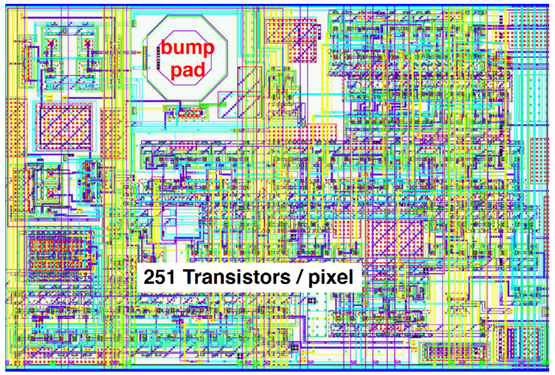
From Present to near-Future

PRESENT DETECTORS for pp@LHC

innovation allow to decrease of a factor ~5 the pixel size either improving performance (threshold, speed, data rates…)

CMS

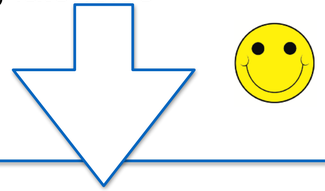
PSI46 (150um x 100um)



- 250nm CMOS tech
- **251** transistors/pix

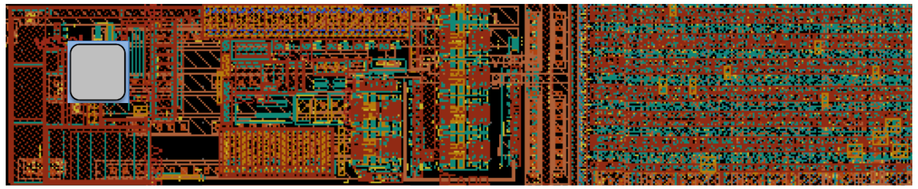
YES !

65nm technology allows to design a smaller pixel capable to sustain extreme particle fluxes and long latencies



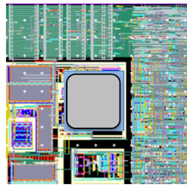
ATLAS

FEI4 (50um x 250um)



- 130nm CMOS techn
- ~**2500** transistors/pix
- ~0,5 trans/um^2

RD53 / CHIPIX65



(50um x 50um)

- 65nm CMOS tech
- ~**2500** transistors/pix
- ~2 trans/um^2

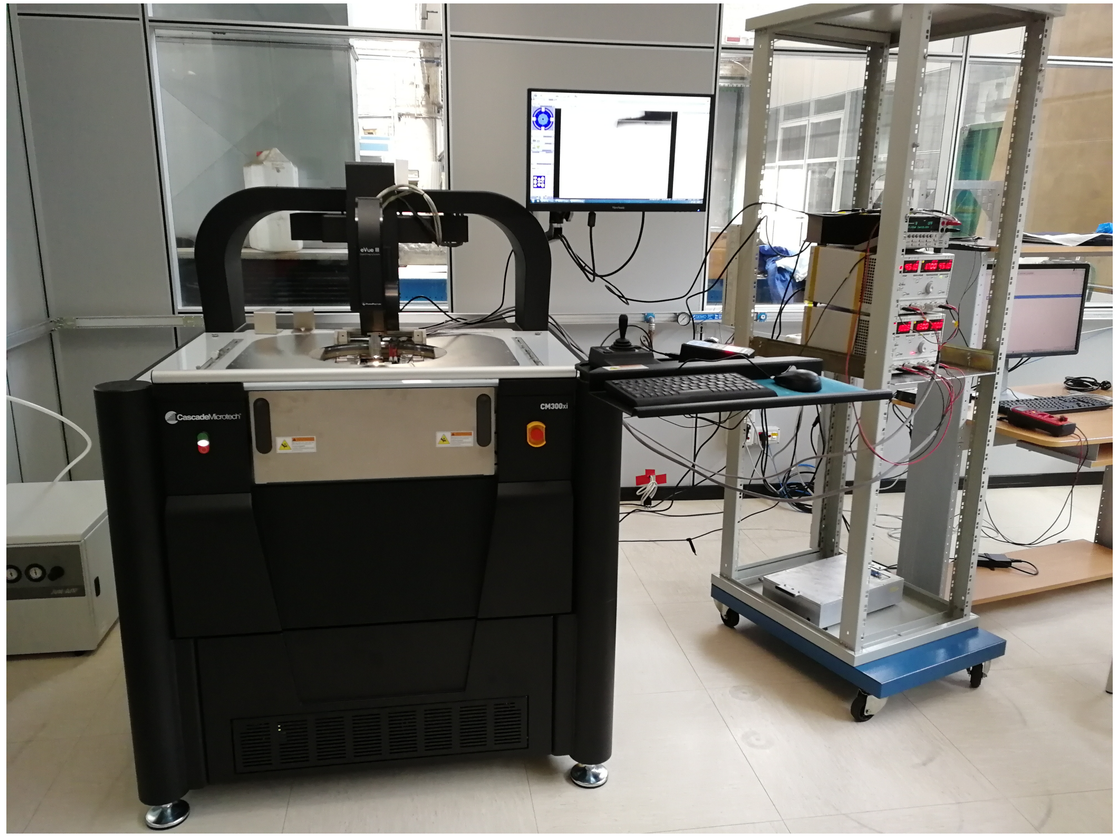
50% of area to digital

for ATLAS & CMS

Laboratory : part one

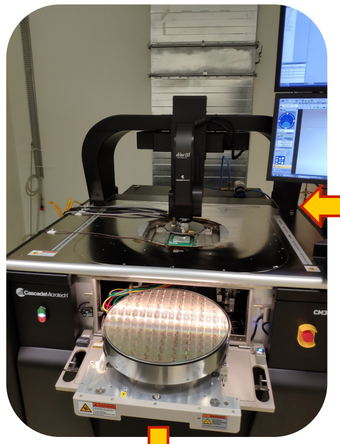
- Fresh from the Fab ! see how ASIC arrives from industry
- Look to a Pixel Readout Chip from a Probe-station
- Learning how to test a naked chip
- Doing Quality assurance and selection of good chip
- Learning how to behave in a clean room …

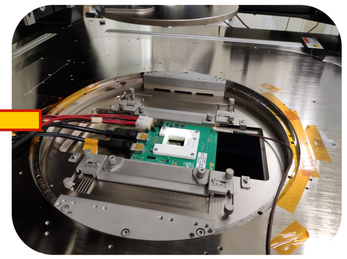
Laboratory : part one



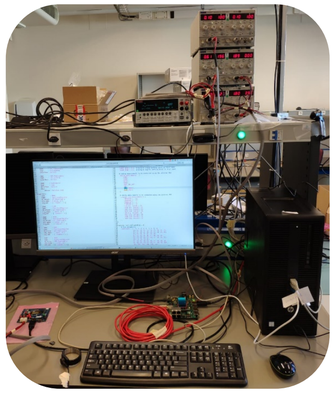
PROBE STATION 12” @ TORINO Clean Room
Unique facility in INFN for making
Wafer Level testing on microelectronics

Different Steps to make Wafer Level Testing

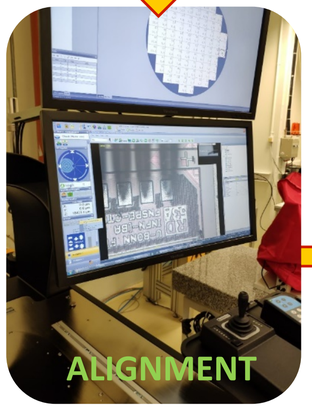




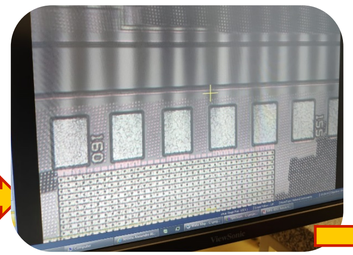
NEEDLE CARD TILT ADJUSTMENT



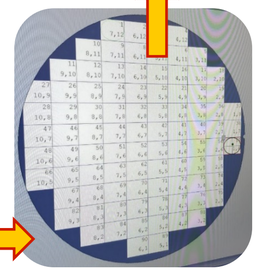
TEST THE WAFER WITH BDAQ



ALIGNMENT



PATTERN RECOGNITION

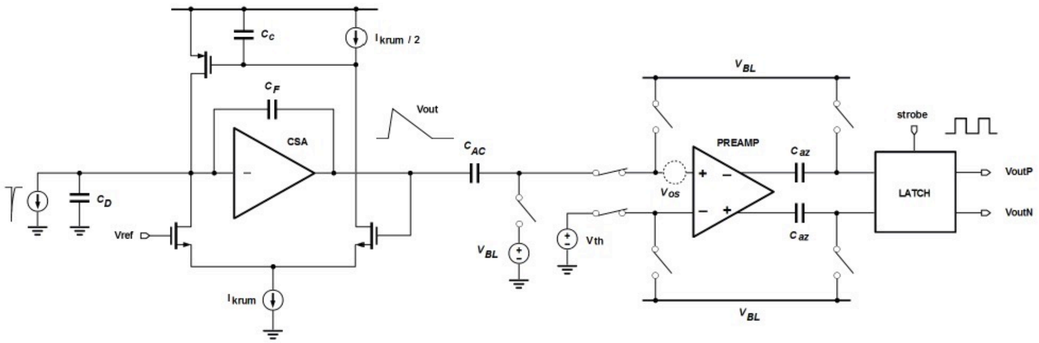


CHECKS IN REST OF THE CHIPS

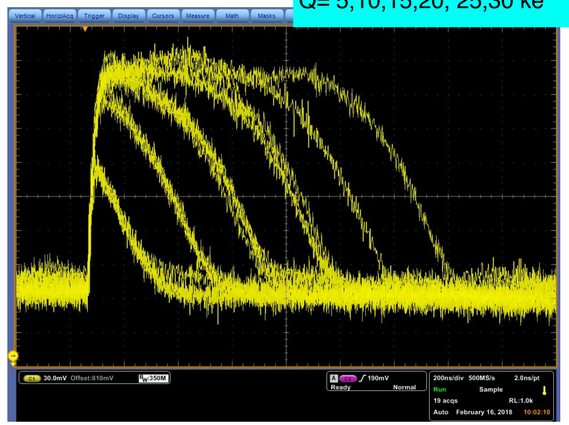
Laboratory : part two

- Doing characterisation of a chip &/or a chip+sensor
    - Looking to a signal coming from a Pixel Front End
    - Learning what is an S_Curve
    - Learning how to measure threshold and noise
    - Tuning the threshold and make it as low as possible
    - Checking linearity of the Front End vs charge injected
    - Collecting data with Sr90

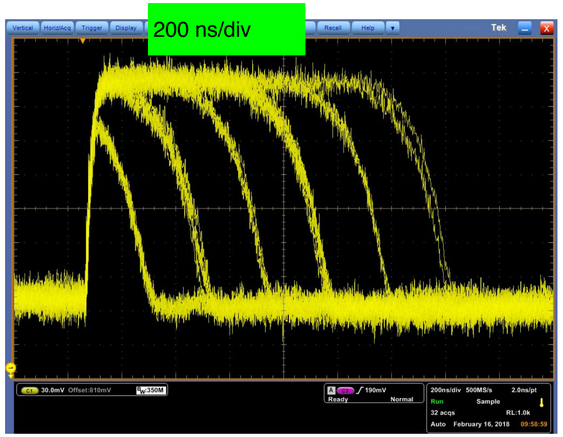
Laboratory : part two



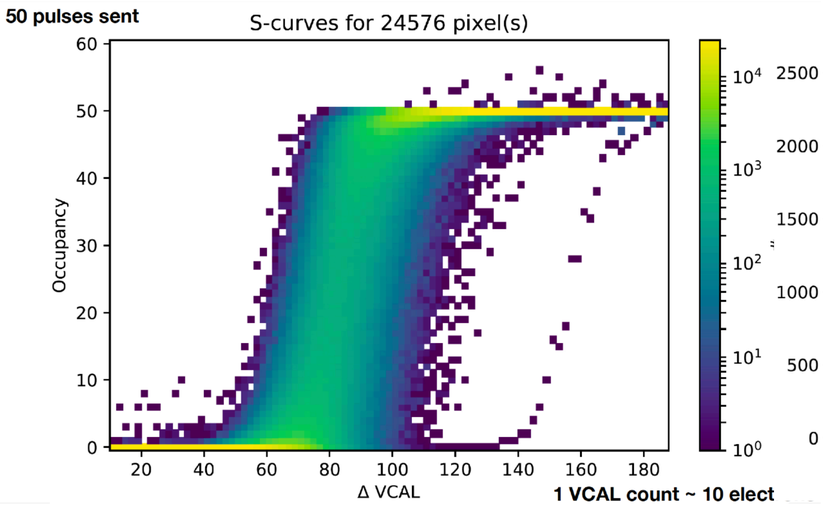
Q= 5,10,15,20, 25,30 ke

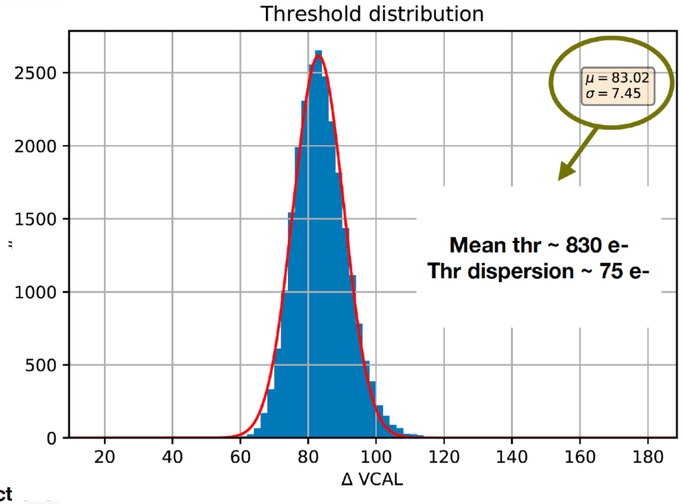


200 ns/div

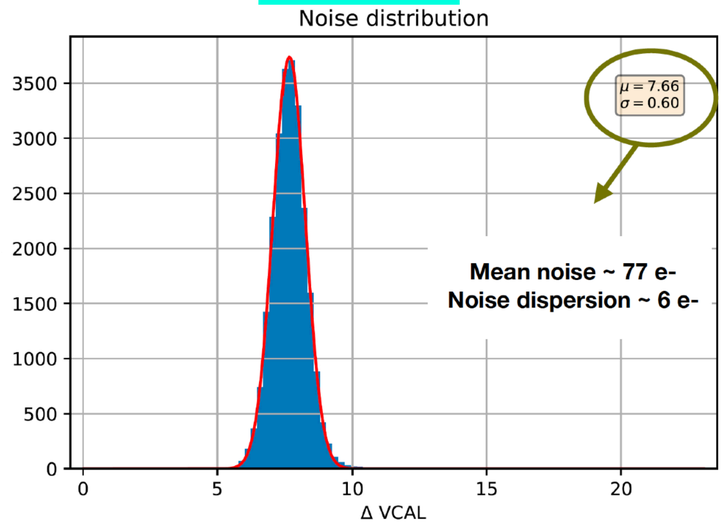


Low Gain

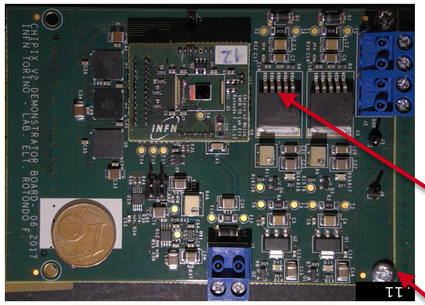


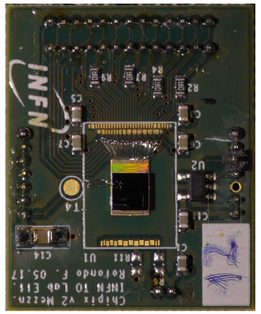


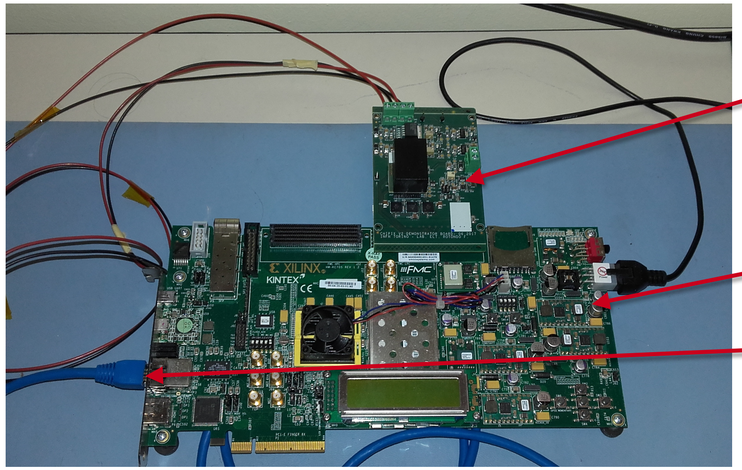
High Gain



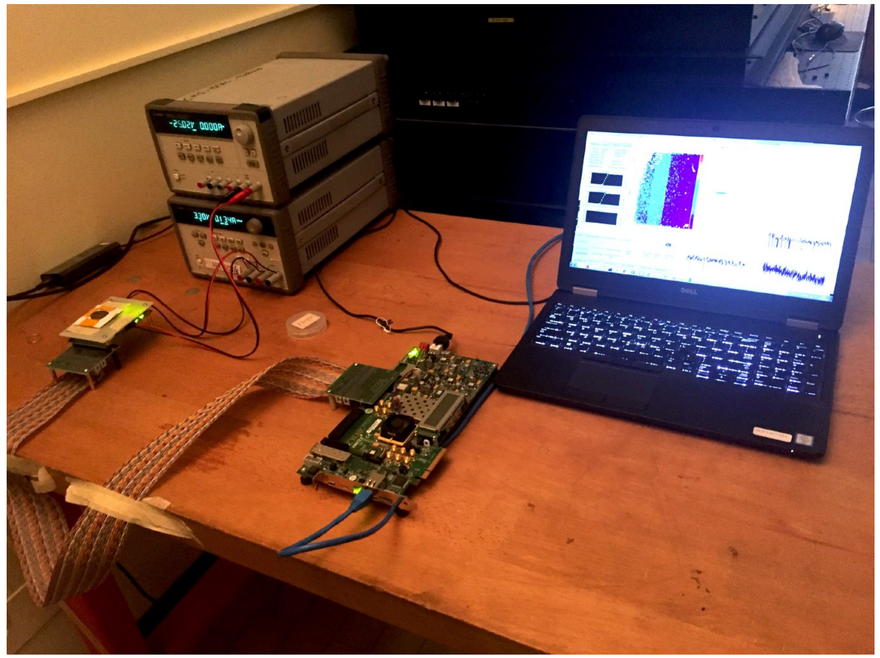
Laboratory two : setup (1)



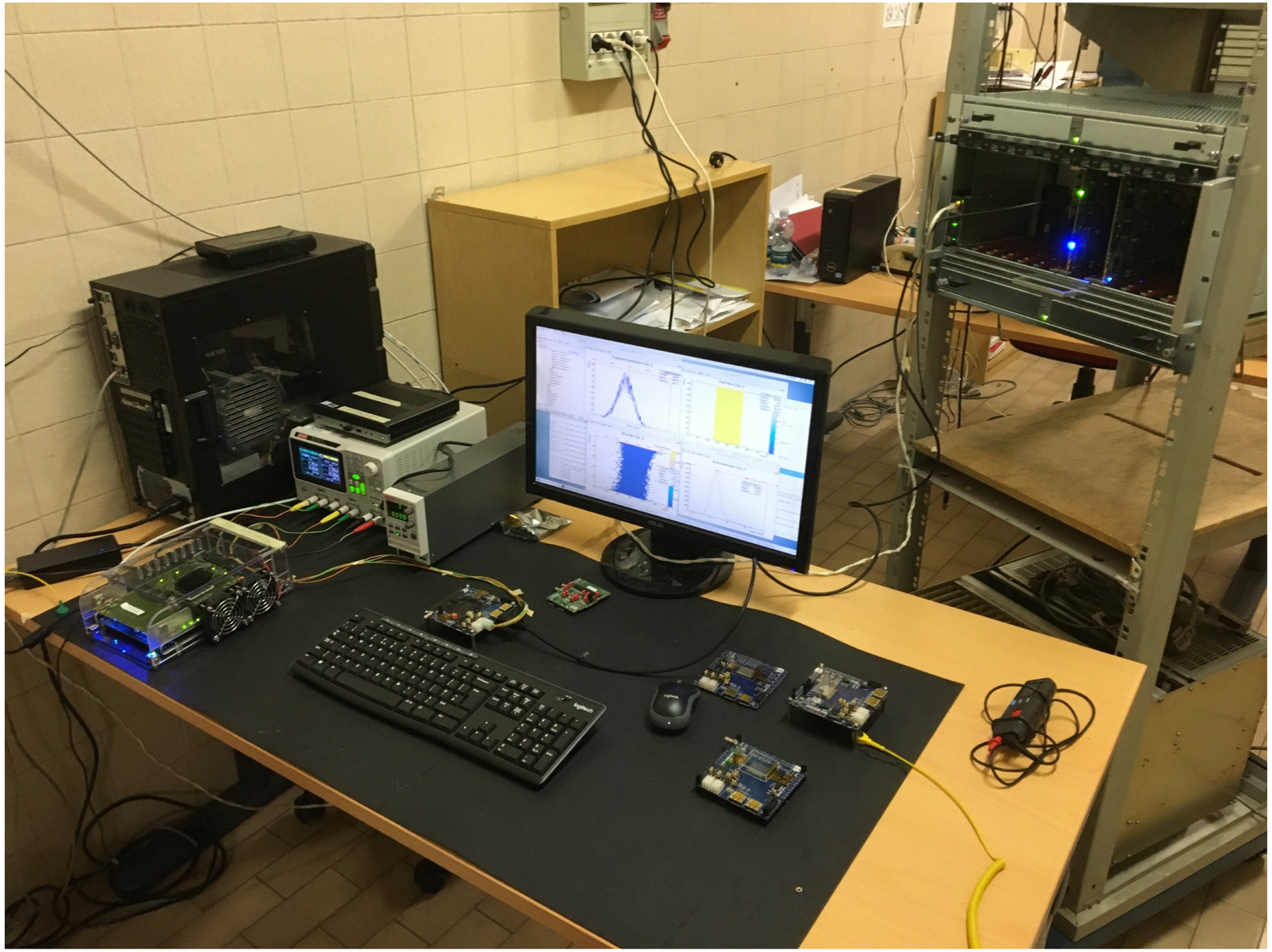




- Mezzanine with wire bonded chip
- Carrier board mounting mezzanine. FMC-connection to FPGA. External low voltage converted to 1.2V via power regulators
- FPGA board : Xilinx evaluation board (Kintex-7 kc605)
- Ethernet connection to PC running Labview

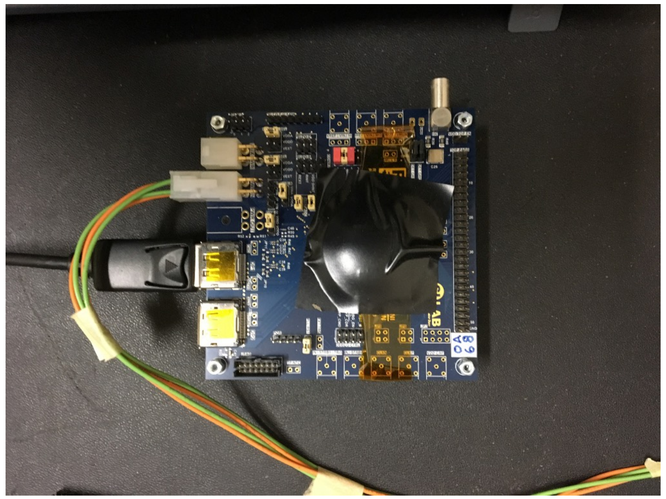


Laboratory two : setup (2)

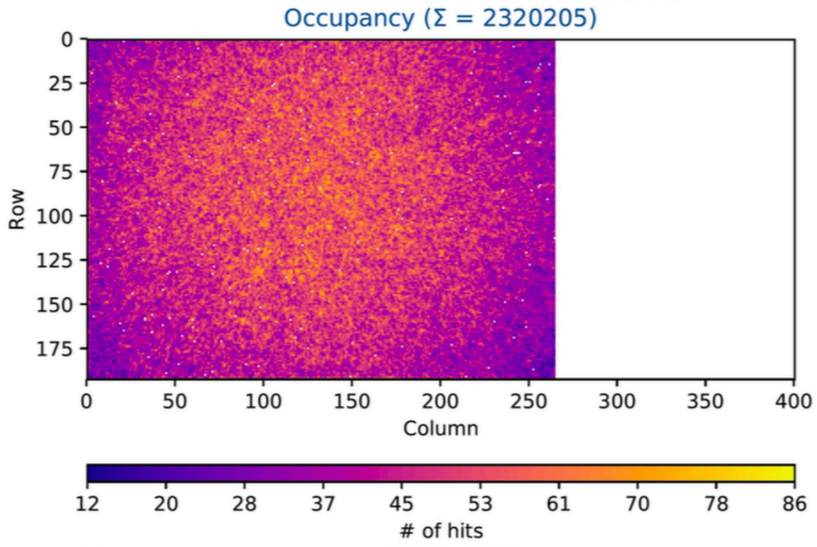


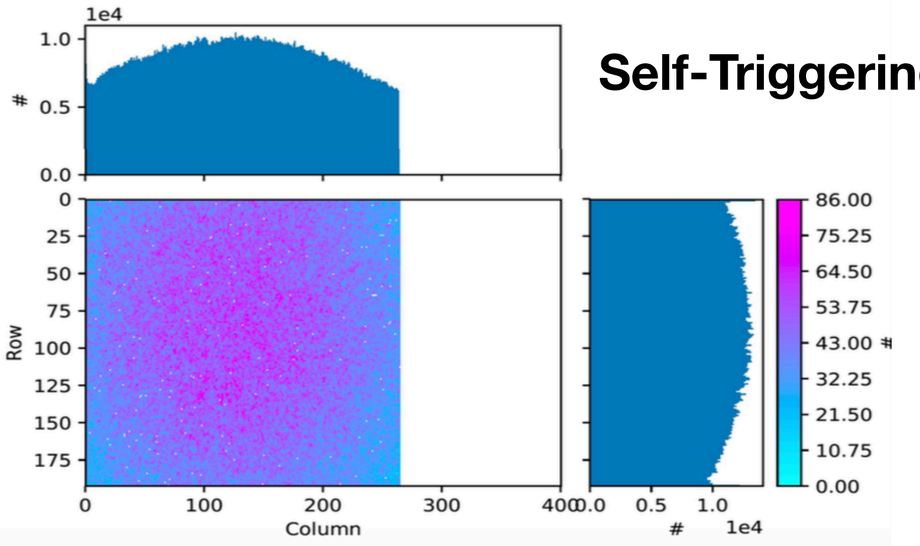
micro-TCA crate
containing several boards with Kintex-7

- communication via Ethernet to several Boards
- upload of Firmware into each Kintex (1 for Board)
- calibration of RD53A chip alone
- calibration of module : RD53A bumpbonded to sensor

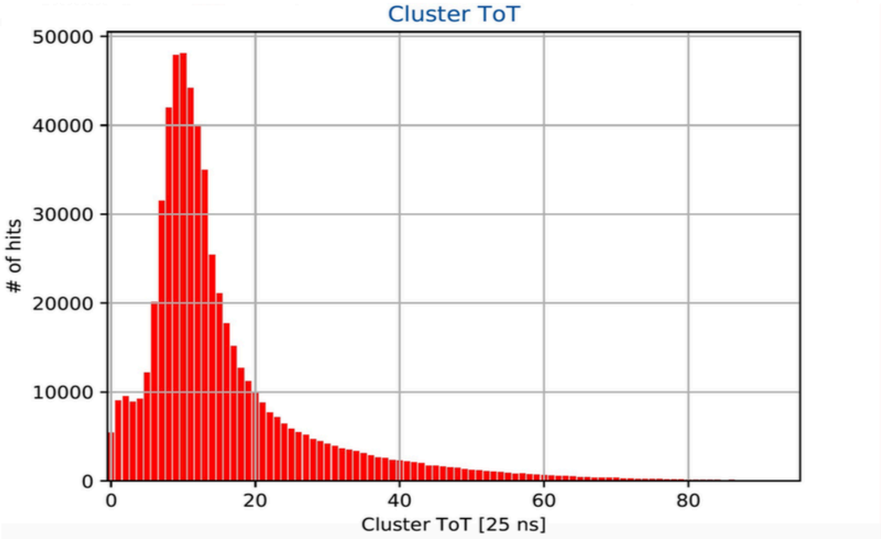


Laboratory two : optional



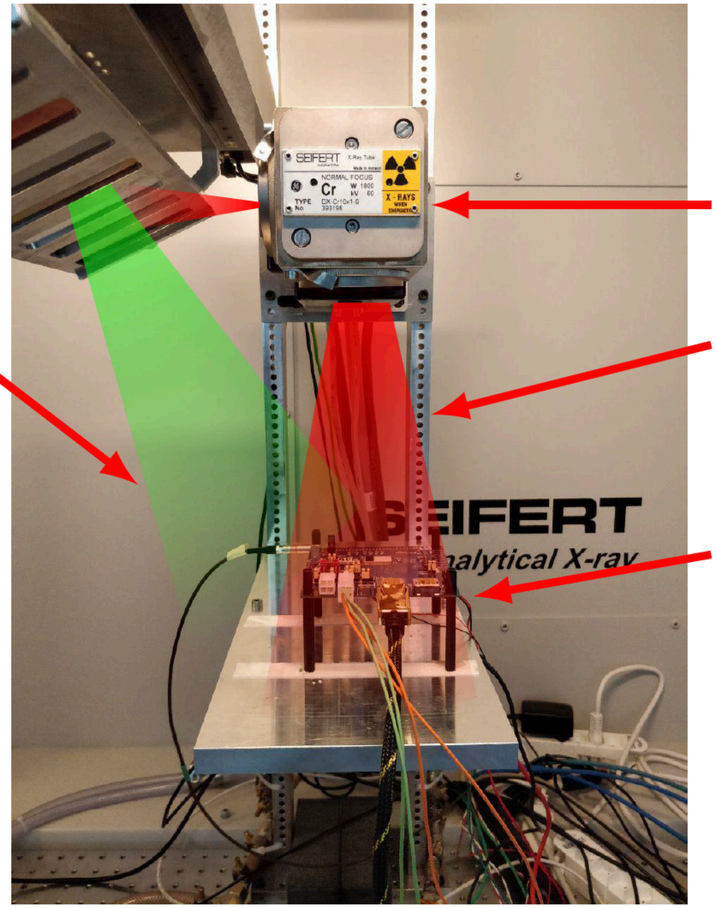


Self-Triggering with Sr90 source



Laboratory two : optional

Monochromatic beam from metal targets (not used in this measurement)



X-ray source

Direct beam

Module

…or new
x-ray machine coming Q2/2020

Efficiency vs trigger frequency