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#### Firmware at the Mu2e Test Stand

Micol Rigatti Final Report 25/09/2019

#### **Mu2e Experiment**

A search for Charged-Lepton Flavor Violation



neutrino-less coherent conversion of the muon in electron

The observation of this physics process would demonstrate the existence of physics beyond the standard model



#### Mu2e Concept



- Generate a beam of low momentum muons  $(\mu^{-})$
- Stop the muon in a target (aluminum)
- The stopped muons are trapped in orbit around the nucleus
- Look for events consistent with  $\mu N \rightarrow eN$



#### **The Mu2e Detector**





#### Tracker

Identify and measure 105 MeV/c electrons

18 stations are assembled into the completed tracker



A station is 1 plane of 6 panels

A panel is a group of 96 straws









The detector has 23,000 straws distributed into 20 measurement

stations across a 3 m length.

Each straw is instrumented on both sides with preamps and TDCs.

Signal from the straws need to be amplified, digitized and trasmitted to the DAQ.





#### DRAC





# Mu2e tracker digitizer and readout controller board

It sits on the outer edge of each Mu2e tracker panel and services the entire panel via 12-bit 50 Mbps ADCs (MAX19527) digitizing the hit energy from each of the 96 straws.

The time of the hits from the two ends of the straws is digitized inside two Microsemi PolarFire FPGAs (MPF300TS-1FG1152), called DIGI HV and DIGI CAL.

A third Microsemi PolarFire FPGA, called ROC, is connected to each DIGI via four 5 Gbps SERDES lanes and to the TDAQ via a two 2.5 Gpbs fibers connected to a Data Transfer Controller.



#### **Optical Fibers**





#### **TDAQ - Mu2e Trigger and Data Acquisition**



### TDAQ - DTC



The Data Transfer Controller (DTC) collects data from multiple detector Readout Controllers.

The DTC is implemented using a commercial PCIe card located in the DAQ Server.

There are a total of 36 DAQ servers, occupying four racks in the electronics room.



#### **TDAQ -** Run Control Host



The Command Fanout (CFO) module in the Run Control Host is responsible for generating and synchronizing packets by sending Heartbeat control packet for each event window.



#### **ROCs – Readout Controllers**







#### **Firmware concept on DRAC**



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# **TOP SERDES**

The main purpose of the firmware developed on the evaluation board is to manage communication between the Trigger and Data Acquisition (TDAQ) and the Mu2e detector subsystem Readout Controllers (ROCs).



#### **Testing link between ROC and DTC**



# Data Transfer Controller Optical Fiber

#### Evaluation board with TOP SERDES





#### **Libero SoC**

Libero - C:\M\08172019\_ReqAndReadTestingTry2\V121\_05152019\_ResetExtravaganza.prjx\*

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#### **TOP SERDES**



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17 23/8/2019 Micol Rigatti | Midterm Report

#### otsDAQ - off-the-shelf data acquisition

otsdaq is an online DAQ software framework. It is a web interface to configure, control, and monitor the online DAQ software entities from Chrome.





#### Vivado – signals from DTC

| 🝌 Vivado Lab Edition 2018.3  |   |                                       |   |               |                      |   |              |               |                     |   | - 0 )         |  |
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| Name. nw_lia_5   | <   | Updated at: 2019-Aug-19 15            | :05:30                                  |               |                      |   |              |               |                     |   | ~ ~           |  |
| Cell: RingController_inst/RingInterface  |   |                                       |   |               |                      |   | _            |               |                     |   |               |  |
| Device: @ xc7k325t_0   | Settings - hw_ila_6 Status - hw_ila_6 × ? _ D                               |                                       |   |               |                      | Trigger Setup - hw_ila_6 × Capture Setup - hw_ila_6 ? _ 🗆 |              |               |                     |   |               |  |
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| General Properties   |   |                                       |   |               |                      |   |              |               |                     |   |               |  |
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| <pre>     display_hw_ila_data [upload_hw_ila_data [get_hw_ila</pre>  | as -of_objects [get_hw_devices xc7k325t                                     | t_0] -filter {CELL_NAME=~"RingContro: | <pre>ller_inst/RingInterfaces[0].</pre> | u/GTX0ILAs.il | all_i"}]             | 1   |              |               |                     |   |               |  |
| ; INFU: [Labtools 27-1966] The ILA core 'hw_ila_5' tr<br>INFO: [Labtools 27-3304] ILA Waveform data saved to   | riggered at 2019-Aug-19 15:09:38<br>p file C:/Users/mrigatti/AppData/Roamin | ng/Xilinx/vivado lab/.Xil/vivado lab- | -21376-CD-132133/backun/hw i            | la data 5.ila | . Use To             | 1 command   | 'read hw ila | data' or Viv  | ado File->Import->' | mport ILA Data menu item                | m to import t |  |
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#### What so far?

#### PROBLEMS SOLVED:

- Bad synchronization on latches
- RESET bug
- Wrong calculation on the CRC
- Bad handling of the RESET on the retransmission





#### TASK ACCOMPLISHED:

- Debugging, testing and fixing retransmission of corrupted data
- Changed marker detection
- Testing of Read, Block Read, Write, Block Write Request
- Testing of Heartbeat and Data Request
- Stress Test



#### What now...?



#### **Pictorially: Event Window synchronization**





Each spill contains approximately 32 000 uBunches, for a total of 256 000 Bunches in a 1.4 second supercycle. A Bunch is 1695 ns.

# Timing





#### Loopback

- 1. The Command Fan Out (CFO) is the 40 MHz single clock source and fans out clock to N Data Transfer Control (DTC) units
- 2. Transmission to the front-end ROCs will be done using optical fiber employing clock-encoded data at 4.0 Gbps



#### **Clock test**





# Next goals

Understand why clock is not recovering and solve that



27 25/9/2019 Micol Rigatti | Final Report

#### Thank you!



### **DDR INTERFACE**



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