BES-III off-detector readout electronics for the GEM detector: GEMROC status update

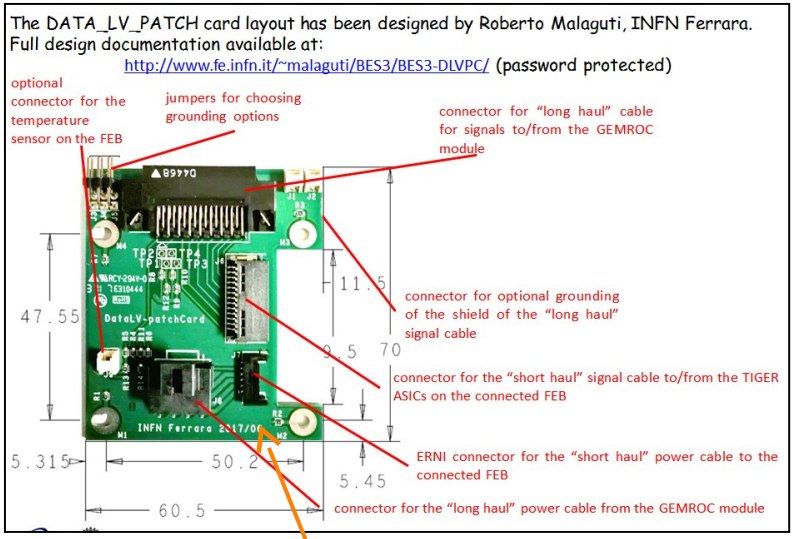
The CGEM off-detector collaboration
(INFN/University FE, INFN LNF, Uppsala University)

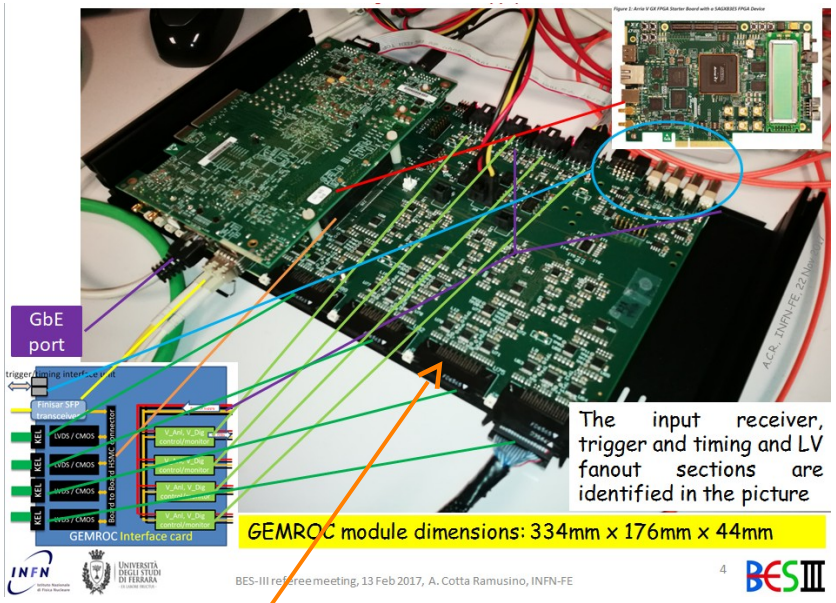
The latest update on the GEMROC modules and auxiliary resources was given at the CGEM Workshop at IHEP on 17 Sep 2019. The presentation covered the status of the off-detector electronics firmware and hardware and the description of ancillary resources to be built to improve the overall noise immunity.

Summary of this report:

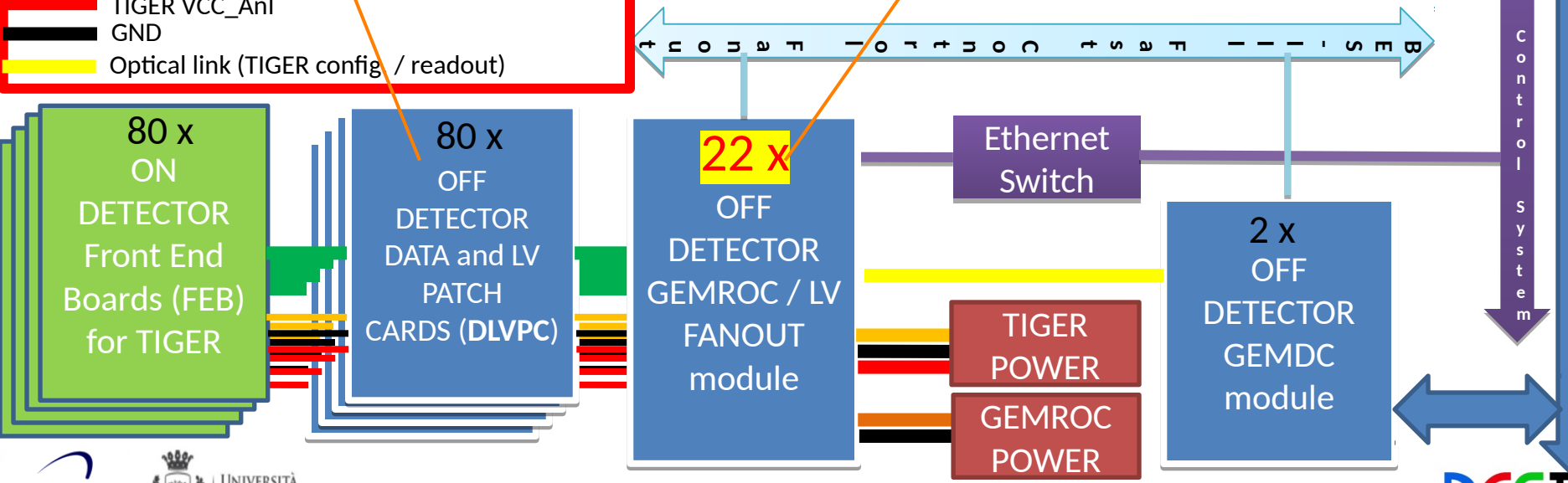
- reminder
- off-detector electronics hardware production status
- GEMROC firmware status
- GEMROC spare components and modules
- NEW ancillary modules:
  - GEMROC BES-III FC system FANOUT (FCF)
  - GEMROC BES-III FC system Local Fanout (FCLF)
  - LVDS repeater (to improve integrity of serial data links from TIGER to GEMROC)
- outlook

- **reminder**: off-detector readout for CGEM detector





Legenda:
- GEM ROC VCC
- TIGER VCC_Dig
- TIGER VCC_Anl
- GND
- Optical link (TIGER config / readout)

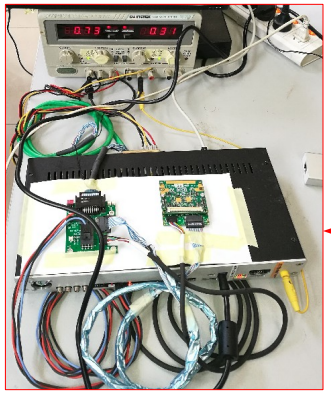


- **off-detector electronics hardware production status**

DATA_LV_PATCH_CARD status:

- 100 manufactured (80 needed)
- all shipped to IHEP on Nov 9 2018 (except for a few spares)

GEMROC MODULE (GEMROC_IFC_CARD (v2) + ARRIA V GX development card) **status**:



- 25 modules assembled (of 22 needed)
- All GEMROC modules are at IHEP presently except:
  - One at INFN-Torino (for performance evaluation and GUFI development)
  - One in INFN-Ferrara (for firmware development)
  - One is in Xiaolu's lab at IHEP to be tested along with a GEM-DC

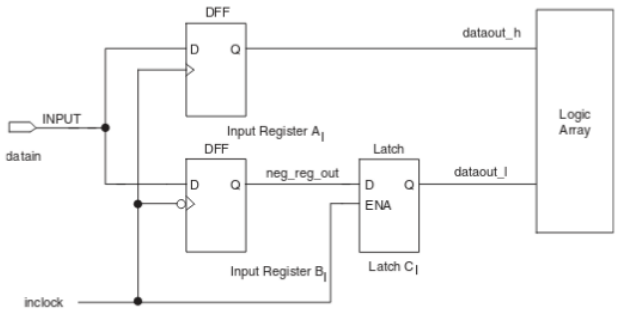
- **GEMROC firmware status**

The current version of the GEMROC firmware is version 9. It has been installed in the GEMROC modules at IHEP on Aug 2nd 2019.

The main feature of version 9 is the insertion of a DDR (Double Data Rate) primitive on the signal path for the TX serial data from the TIGER.

The DDR primitive allows the programmable selection of the edge of the sampling clock on which the TX serial data is sampled.

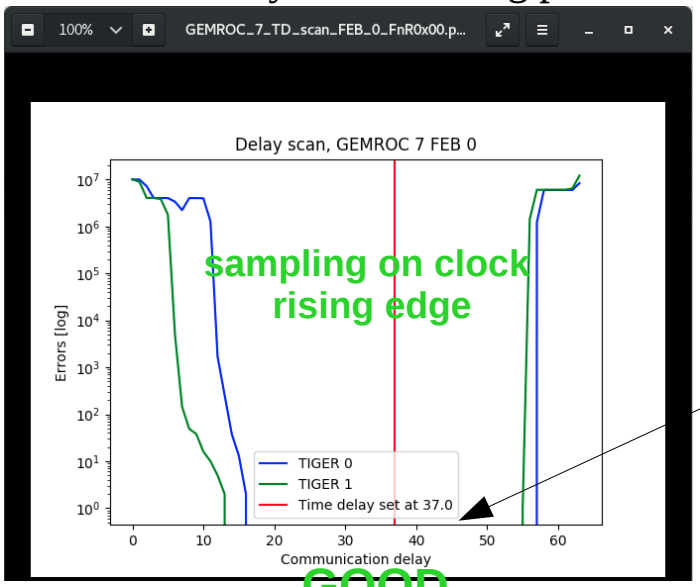
Figure 1–1. Input DDR I/O Path Configuration for a Stratix Series or APEX II Device

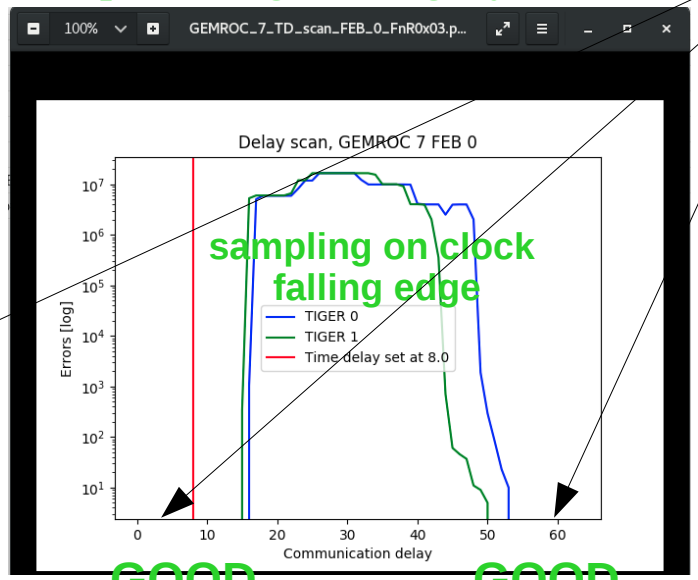


Note to Figure 1–1:

(1) On the falling edge of the clock, the negative-edge triggered register B_I acquires the first data bit. On the corresponding rising edge of the clock, the positive-edge triggered register A_I acquires the second data bit. For a successful data transfer to the logic array, the latch C_I synchronizes the data from register B_I to the positive edge of the clock.

These new degree of freedom extends the range of sampling delay values for which **no receive errors are detected**, as shown by the following pictures. **The effect is: improved signal integrity**





GOOD range

GOOD range

GOOD range

- **GEMROC firmware status**

TODO:

1) Issues to be solved (affecting but not stopping the data taking)

a) TM data packets are sometimes sent to the DAQ PC in response to the trigger (sometimes even 2 triggers) following the right one. It affects the data from TIGERs connected to inputs ports 4, 5, 6 and 7.
This issue can only be partly recovered by software and thus it affects the data taking somewhat.

b) The efficiency of Trigger Matching is up to more than 97% with firmware version 9. By comparison, in the same input rate (pulser) conditions the triggerless DAQ is 100% efficient -> the TM algorithm needs to be improved

2) To be commissioned:

a) Back pressure signal from the GEM-DC (Data Concentrator) modules to the GEMROC

b) full data taking through the GEM-DC modules

- **GEMROC spare components and modules**

SPARES NEEDED for 4 more **GEMROC modules** to be built in 2019 / 2020 to have a safe (hopefully) supply of spares even when using **22** GEMROC instead of the minimum 20:

- **7** pieces of **ArriaV GX FPGA development kit**:
  - **3** (so far) to replace the ones with failing JTAG port: these may be used, and are in use, for data taking but some features of FPGA (such spying internal signals for instance) are not available. Mode of failures:
    - USB to JTAG adapter installed on the FPGA development kit lost configuration: possibly repaired by reprogramming on board device
    - JTAG port of target FPGA not accessible (neither with on on-board nor off-board USB to JTAG adapter); failure in reading back from FPGA. Can't tell whether it is repairable.

    Reason for failures:
    - Failed while in operation but reason for failure hasn't been detected
  - **4** additional spares
- **4** pieces of **GEMROC_IFC** cards
- **4** pieces of **TEKO DS3470** enclosures

- **NEW ancillary modules**

GEMROC BES-III FC system FANOUT (FCF)

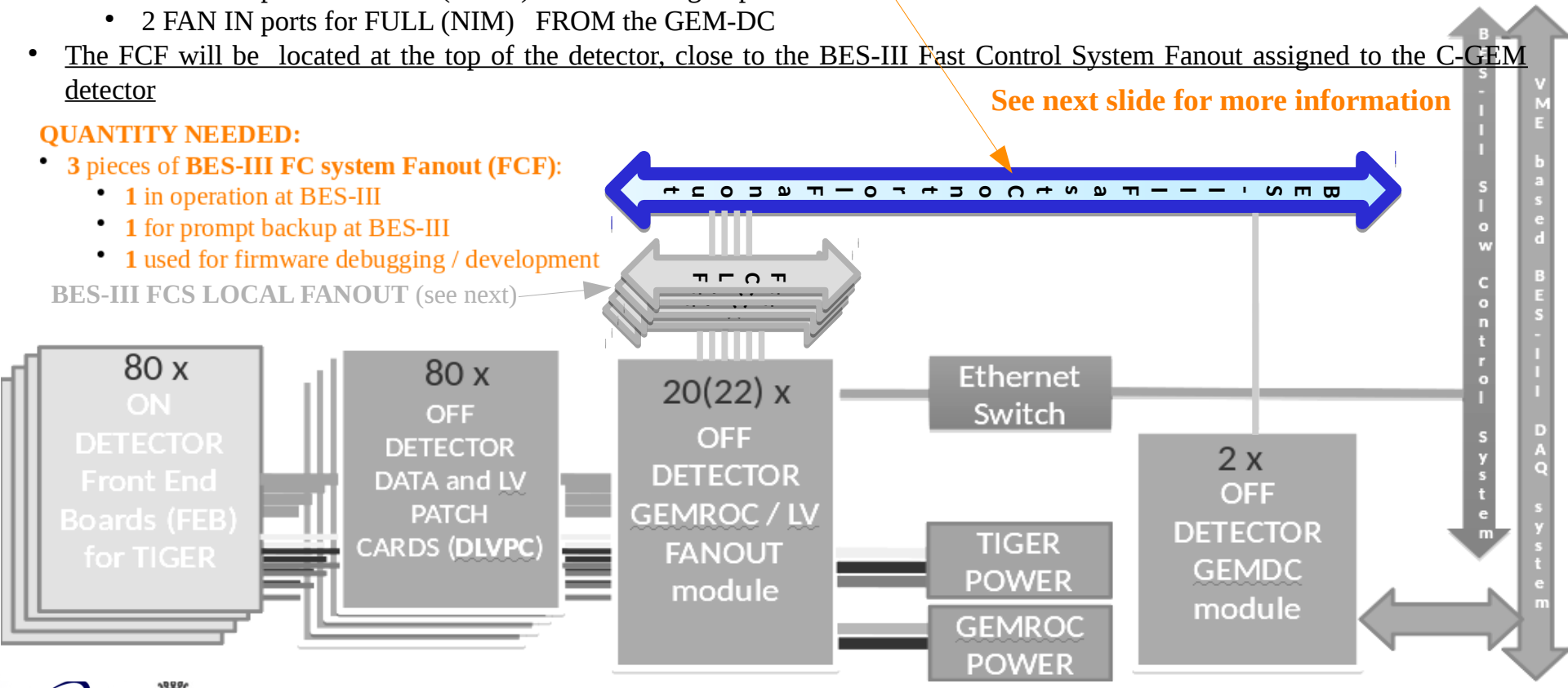
- **The BES-III Fast Control System Fanout (FCF) is a modified GEMROC module** which connects to the CLK, L1, L1_CHK, FULL signals from the BES-III Fast Control System Fanout. It is programmable so it can generate simulated Fast Control signals for stand-alone data taking
- The FCF will have:
  - **4 FAN OUT ports for CLK, L1, L1_CHK (LVDS) TO the 4 groups of GEMROC installed around the BES-III detector**:
    North East, South East, North West, South West
  - 2 FAN OUT ports for CLK, L1, L1_CHK (NIM) TO the 2 GEM-DC
  - 4 FAN IN ports for FULL (LVDS) FROM the 4 groups of GEMROC installed around the BES-III detector
  - 2 FAN IN ports for FULL (NIM) FROM the GEM-DC
- The FCF will be located at the top of the detector, close to the BES-III Fast Control System Fanout assigned to the C-GEM detector

See next slide for more information

QUANTITY NEEDED:

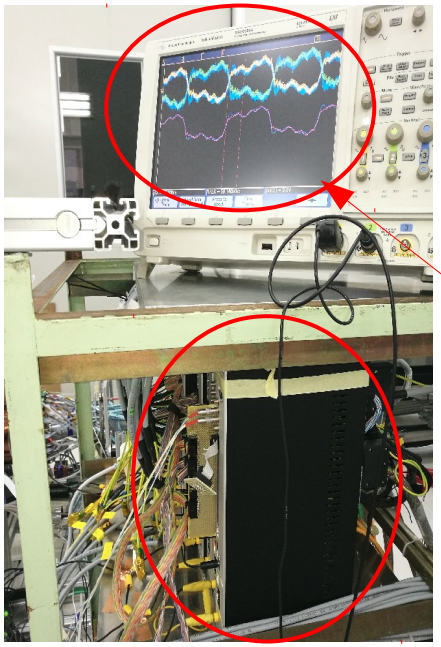
- **3** pieces of **BES-III FC system Fanout (FCF)**:
  - **1** in operation at BES-III
  - **1** for prompt backup at BES-III
  - **1** used for firmware debugging / development

BES-III FCS LOCAL FANOUT (see next)



- **NEW ancillary modules**

GEMROC BES-III FCS SYSTEM FANOUT (FCF)



One prototype Fast Control System Fanout (FCF) has been installed during the last integration week at IHEP (June 2019) to distribute Fast Control Signals (FCS) to the GEMROCs in the cosmic test setup at IHEP (*).
Note: in this installation it has acted also as a Fast Control LOCAL Fanout (FCLF) described in the next slide.

Features of the BES-III FC system Fanout (FCF) prototype module :

- Generation of the main clock for all the GEMROCs in the setup
- Fanout, over 4 identical ports, of:
  - **Clock** : internally generated.
  - **"In-time"** signal : received from the PMT front end. Used to generate a test pulse in coincidence with the cosmic event to a dedicated TIGER channel
  - **Trigger** : received from a delay module. The signal, arriving 8.6us after the "In-time" pulse is used to trigger the event readout
- Programmable self generation of all fast timing signals listed above.

Effects of its introduction in the June 2019 integration week at IHEP:

- It has allowed full synchronization across all GEMROCs through the common Clock and Trigger signals
- It has improved the system stability by distributing a slower (¼ BES-III clock frequency) and better terminated reference clock

- **NEW ancillary modules**

GEMROC BES-III FC system Local Fanout (FCLF)

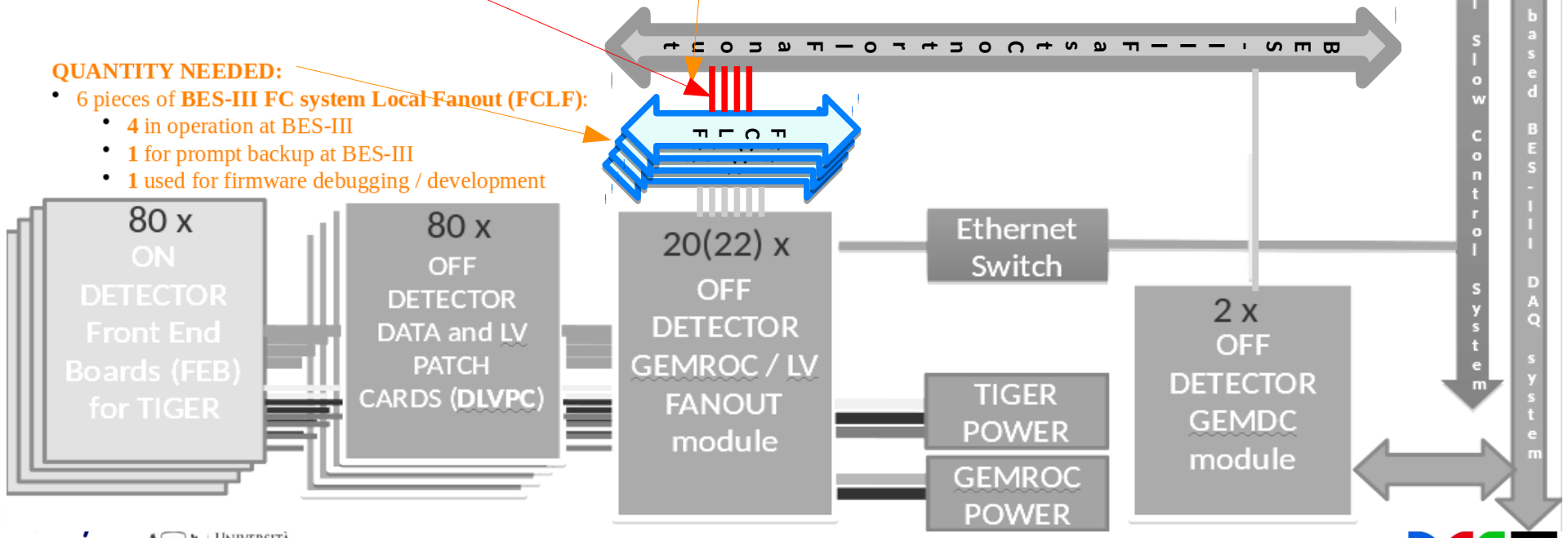
- **The BES-III Fast Control LOCAL Fanout (FCLF) are** a LOW COST, non programmable, fanout modules which connects to the CLK, L1, L1_CHK, FULL signals from the **BES-III Fast Control System Fanout (FCF)**.
- The FCLF(s) will be located at the middle of each of the 4 groups of FEBs located around the detector:
  North East, South East, North West, South West
- The FCLF will have:
  - 6 to 8 output ports for point to point connection to the GEMROC belonging the same group
  - 1 receiver port for the FCS signals from the **BES-III Fast Control System Fanout (FCF)**

The System Fanout (FCF) module will be located on the BES-III platform for DAQ, on top of the detector. An option to use low cost optical links based on DC to 50MHz transceivers in SFP format is also under evaluation for its connections to the LOCAL Fanout (FCLF) modules. This would allow:

- **relaxed constraints on the distance between the System Fanout (FCF) and the LOCAL Fanout (FCLF) modules**
- **reduced concerns about ground loops**

QUANTITY NEEDED:

- 6 pieces of **BES-III FC system Local Fanout (FCLF)**:
  - **4** in operation at BES-III
  - **1** for prompt backup at BES-III
  - **1** used for firmware debugging / development



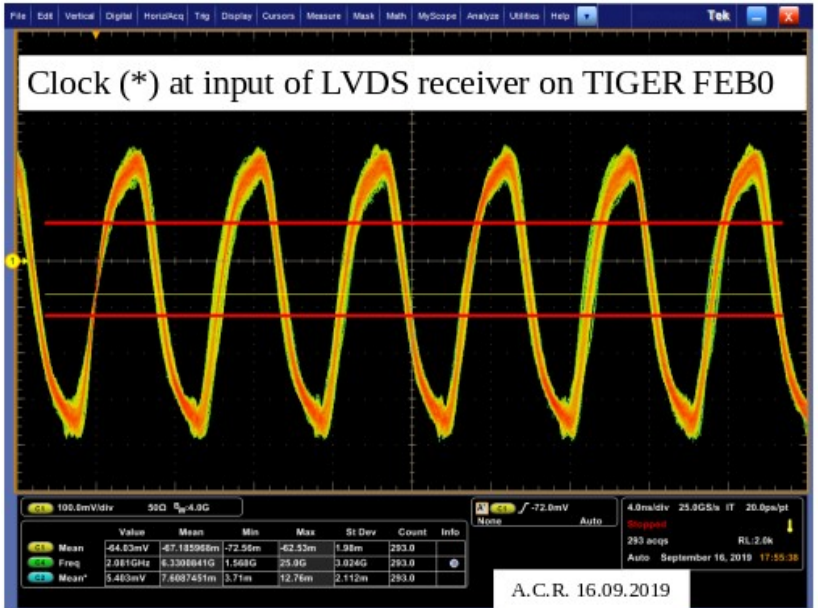
- **NEW ancillary modules**

LVDS repeater (to improve Signal Integrity of serial data links GEMROC ↔ TIGER FEBs)

WHY?

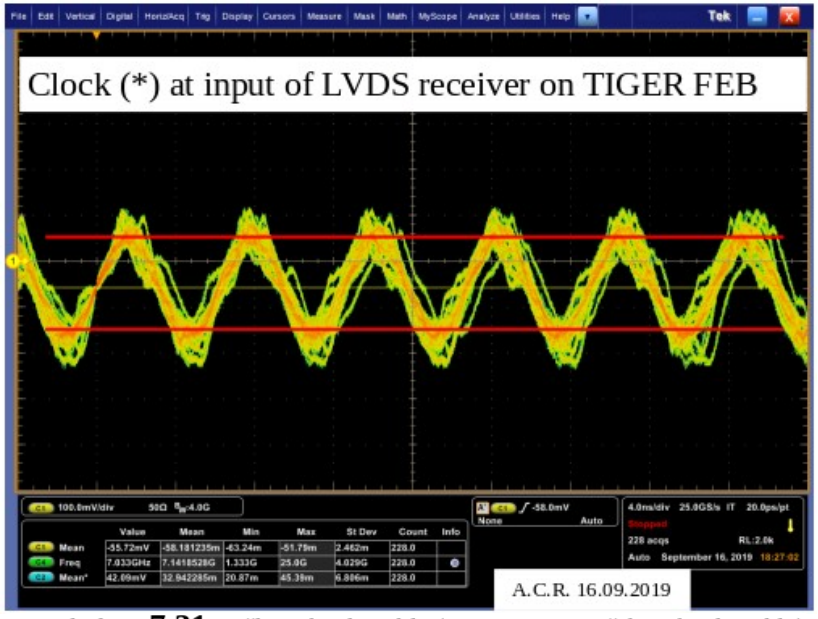
LVDS repeaters (at least for the clock signal toward the TIGER FEBs) are suggested from the following consideration:

the main source of receive errors in the serial data processed by the GEMROC FPGA seems to be the marginal quality of the clock signal reaching the TIGER FEBs on the "long haul cable + DLVPC + short haul cable" path, resulting in excessive jitter in the transmitted data.



signals for a **1m** "long haul" cable (+ DLVPC+1m "short haul" cable)

(*) sampled with a 12GHz active differential probe



signals for a **7.31m** "long haul" cable (+ DLVPC+1m "short haul" cable)

- **NEW ancillary modules**

LVDS repeater (to improve Signal Integrity of serial data links GEMROC ↔ TIGER FEBs)

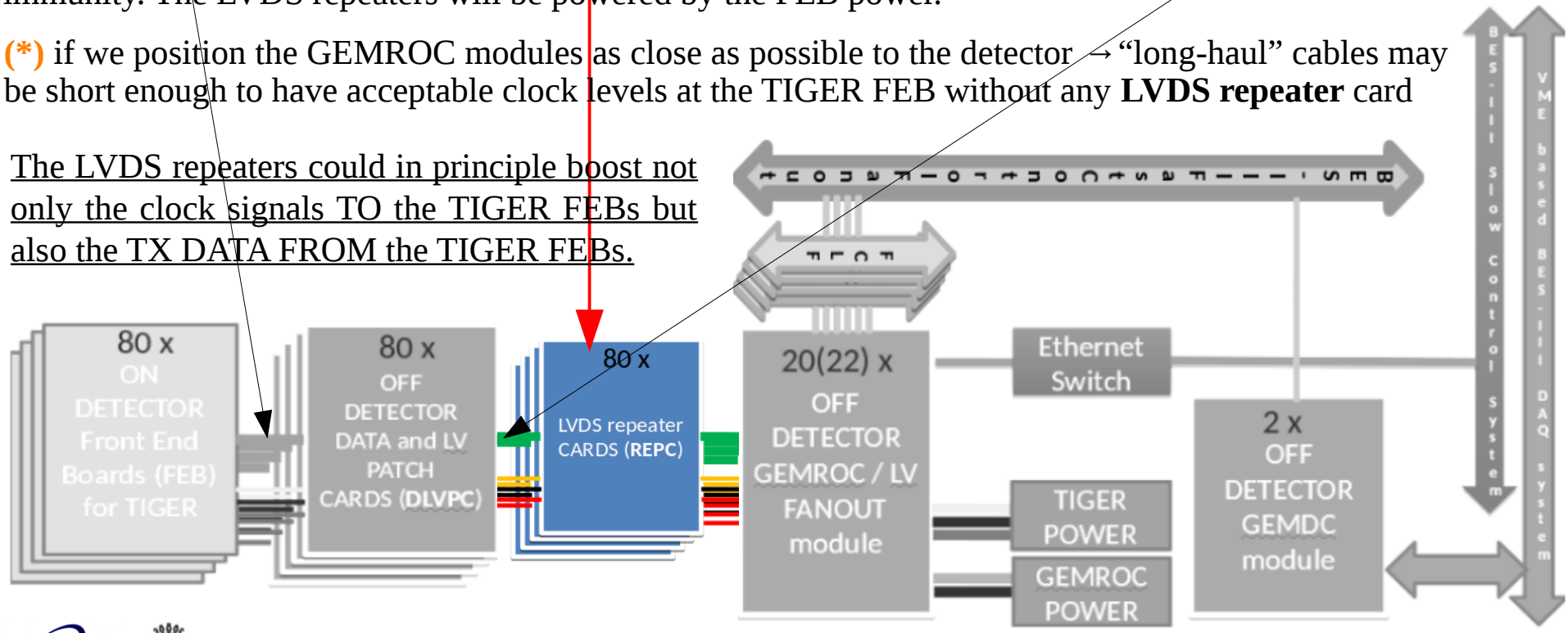
QUANTITY NEEDED:

- **100** pieces of **LVDS repeater** cards **(REPC)** which:
  - **80 maximum (*)** in operation at BES-III
  - **20** spares

As seen in the previous slides, the clock signal reaching the TIGER FEBs through the "long-haul cable + DLVPC + short-haul cable" path is attenuated (and somewhat affected by pick-up noise).
Inserting an **LVDS repeater** cards **(REPC)** in the CLOCK signal path will improve the system noise immunity. The LVDS repeaters will be powered by the FEB power.

(*) if we position the GEMROC modules as close as possible to the detector → "long-haul" cables may be short enough to have acceptable clock levels at the TIGER FEB without any **LVDS repeater** card

<u>The LVDS repeaters could in principle boost not only the clock signals TO the TIGER FEBs but also the TX DATA FROM the TIGER FEBs.</u>



- **NEW ancillary modules**

LVDS repeater (to improve Signal Integrity of serial data links GEMROC ↔ TIGER FEBs)

Alternative to LVDS repeater modules

If tests confirm that boosting the clock signals alone is sufficient

THEN

there is an alternative to LVDS repeaters which is currently being investigated:

to install patch cards in the GEMROC modules based on an LVDS buffer chip with pre-emphasis suggested by colleague Roberto Malaguti of INFN Ferrara.
This will increase the level of the LVDS clock transmitted by the GEMROC and, as a consequence, the levels of the LVDS clock signal received by the TIGER FEBs.

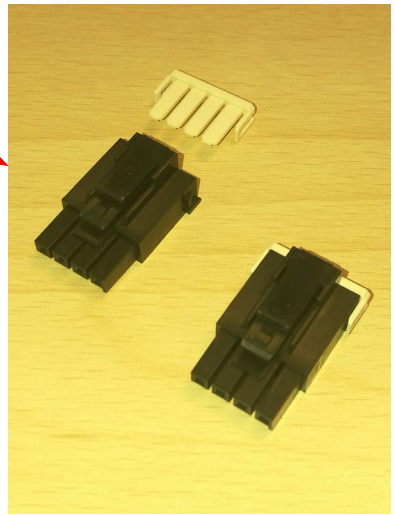
One GEMROC module with boosted LVDS clock levels will be tested at IHEP during the next integration week.

- **outlook**

- Firmware v9 has improved data taking stability in the cosmic ray setup at IHEP. There remain some issues (not preventing data taking) to be solved.

- Installation of a prototype GEMROC BES-III FC system FANOUT (FCF) has improved data taking stability in the cosmic ray setup at IHEP but:

  TODO:
  - complete design and prototyping of ancillary resources (clock buffers, system fanout with XCVR local fanout, local terminator cards)
  - test the patch installed on the GEMROC module to boost the amplitude of the LVDS TIGER_CLOCK output signals (NOVEMBER 2019 at IHEP)
  - upgrade LV cables with new connectors with pin retention features (NOVEMBER 2019 at IHEP)
  - install miniature connectors on the signal cable shields to implement the final grounding scheme (NOVEMBER 2019 at IHEP)



- Funds for building spare GEMROC modules have been granted

- Funds for building GEMROC ancillary resources have been granted and orders for parts to be prototyped in 2019 have been issued

- Aiming to have prototypes of all ancillary modules ready by end of 2019