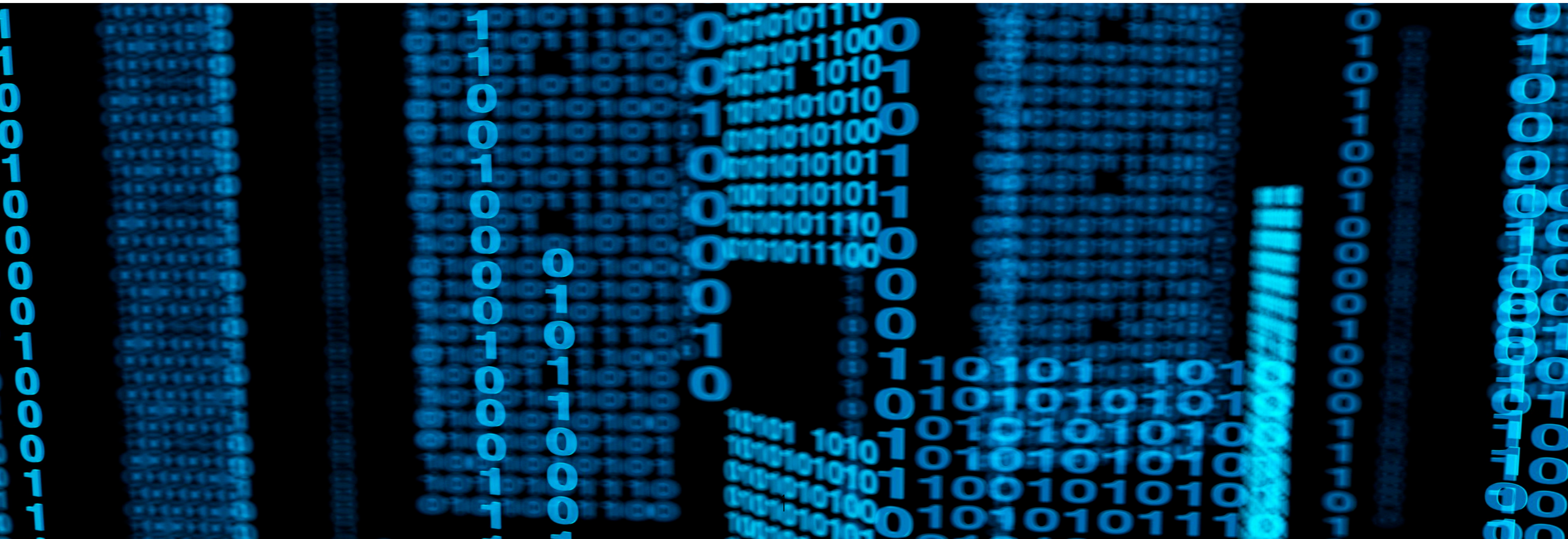
# Lite-DTU status

Torino, Lite-DTU Group

02 October 2019

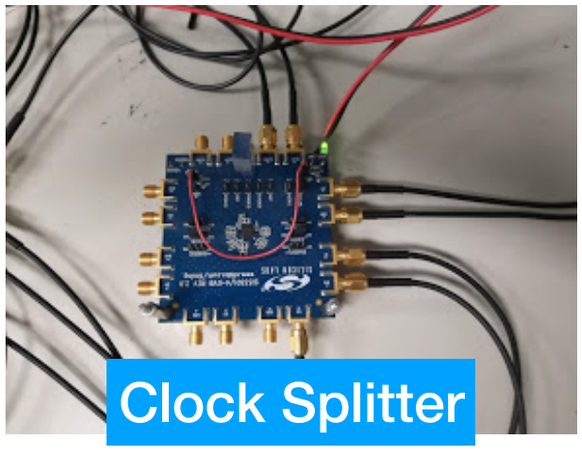


# Introduction

- 8 test boards arrived in Torino at the end of May, after some delay in the design due to INFN central database for CADENCE licenses.
- Two boards are fully functional, the others need some investigation.
- As soon as we mounted the boards, we discovered a hardware bug in the I2C logic. We couldn't communicate with the I2C standard protocol via FPGA.
- We got around the problem adding an external level shifter in the I2C-SDA line. Now we can write/read the registers of the ADC, still problems with the DTU part.
- We needed time to learn how to communicate via FPGA, how to align the FPGA sampling with the data coming out from the ADC. Now we have programmable delays to adjust the phase of the sampling and acquire data in stable conditions.
- We now obtain promising results from the ADC, but not exactly close to the specifications.
- We are here today to show you our results and look for some clarifications.

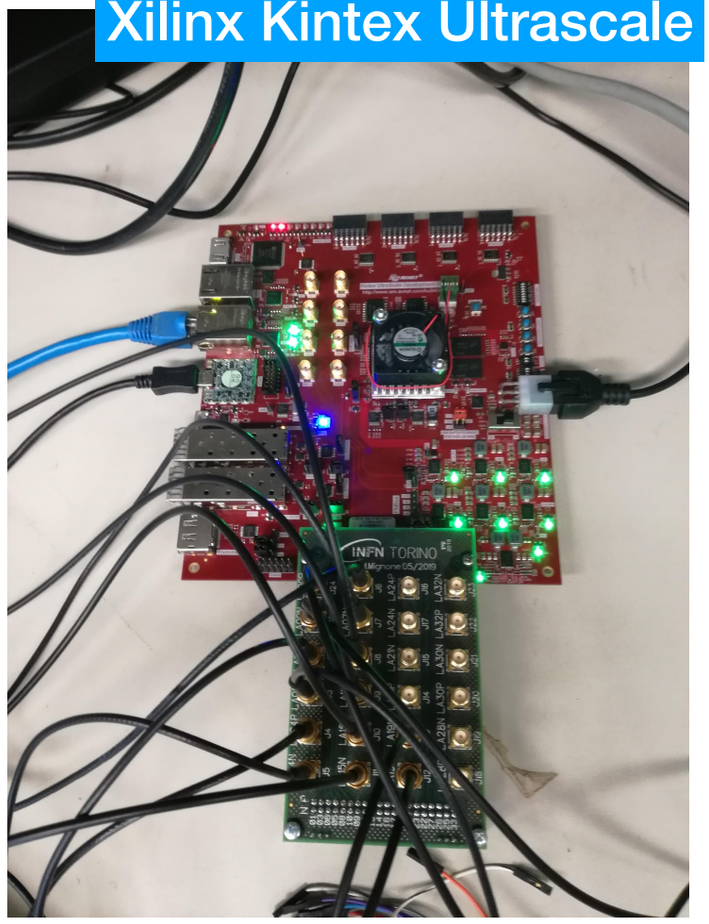
# Test bench setup in Torino

Clock 160 MHz



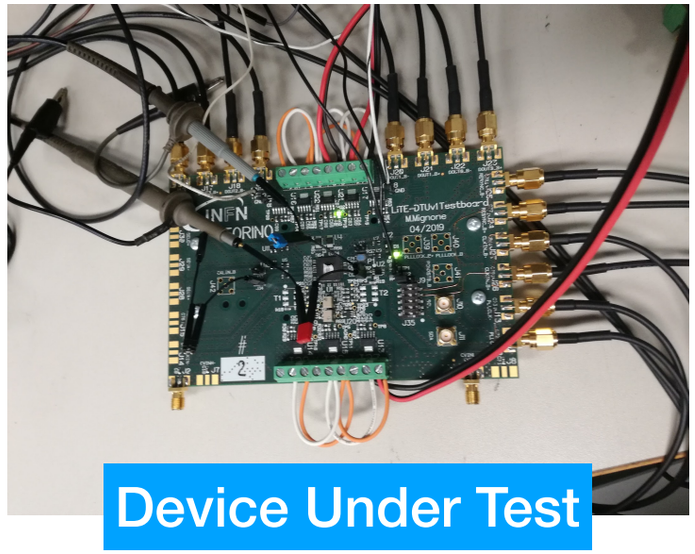
Clock Splitter

Xilinx Kintex Ultrascale



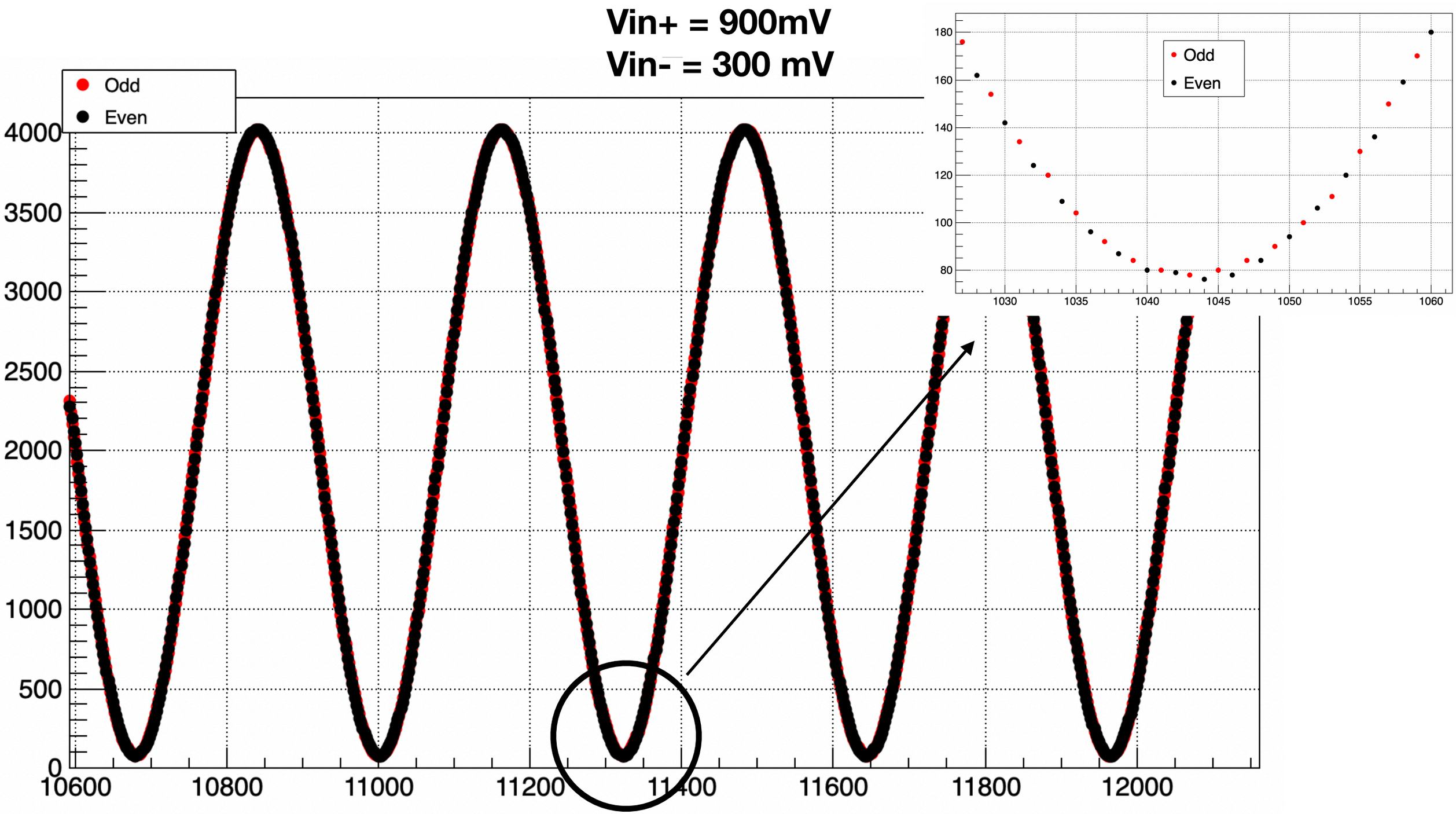

Clock 1.28 GHz

Waveform Generator




Device Under Test

# Calibration



# Calibration

## CHANNEL High gain

**Even samples, sine fit parameters:**
- 0) Amplitude [ch]: 1971.06
- 1) Frequency [Hz]: 498077
- 2) Phase [rad]: 3.13828
- 3) Offset [ch]: 2048.67

**Odd samples, sine fit parameters:**
- 0) Amplitude [ch]: 1972.14
- 1) Frequency [Hz]: 498077
- 2) Phase [rad]: 3.13827
- 3) Offset [ch]: 2048.3

**Sine fit parameters after calibration:**
- 0) Amplitude [ch]: 1972.16
- 1) Frequency [Hz]: 498077
- 2) Phase [rad]: 3.13828
- 3) Offset [ch]: 2048.03

**Calibration parameters:**

*Offset difference (odd - even): -0.36 ch*

***Amplitude difference (odd - even): 1.08 ch***

*Phase difference (odd - even): -8.6e-06 rad*

## CHANNEL Low gain

**Even samples, sine fit parameters:**
- 0) Amplitude [ch]: 1978.2
- 1) Frequency [Hz]: 498077
- 2) Phase [rad]: 3.13906
- 3) Offset [ch]: 2048.8

**Odd samples, sine fit parameters:**
- 0) Amplitude [ch]: 1979.91
- 1) Frequency [Hz]: 498077
- 2) Phase [rad]: 3.13905
- 3) Offset [ch]: 2047.96

**Sine fit parameters after calibration:**
- 0) Amplitude [ch]: 1979.88
- 1) Frequency [Hz]: 498077
- 2) Phase [rad]: 3.13905
- 3) Offset [ch]: 2047.68

**Calibration parameters:**

*Offset difference (odd - even): -0.831585 ch*

***Amplitude difference (odd - even): 1.7116 ch***

*Phase difference (odd - even): -1.29125e-05 rad*

**we see a ~1 lsb between even and odd samples.**

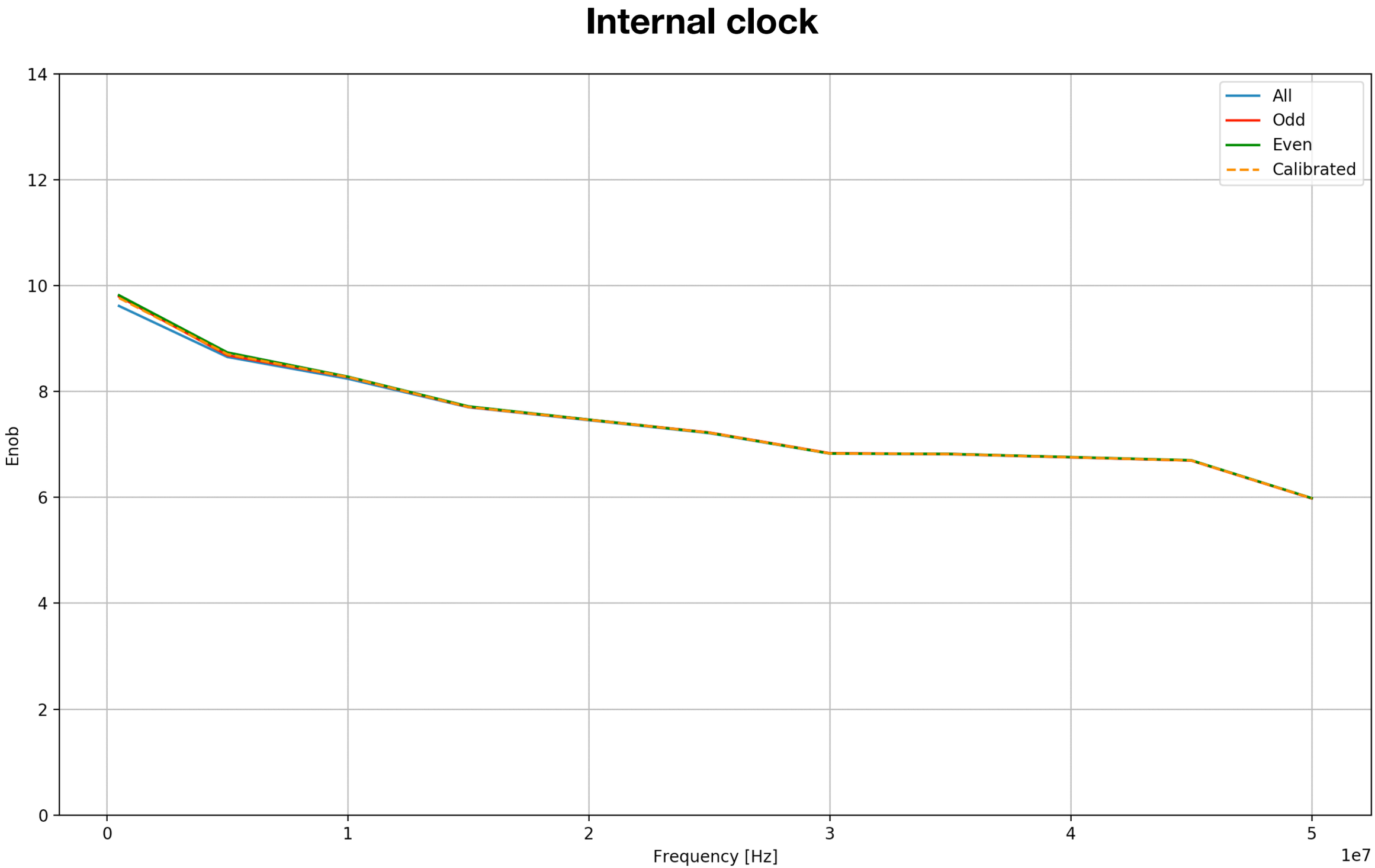
# ENOB Calculation

- Analysis software based on - IEEE Std 1241TM-2010 guidelines.
- Fit with A*sin( $2\pi f_0 t + \phi$ ) + Offset
- Calculate noise and distortion from the fit (it is the rms with respect to the "true" fit data):

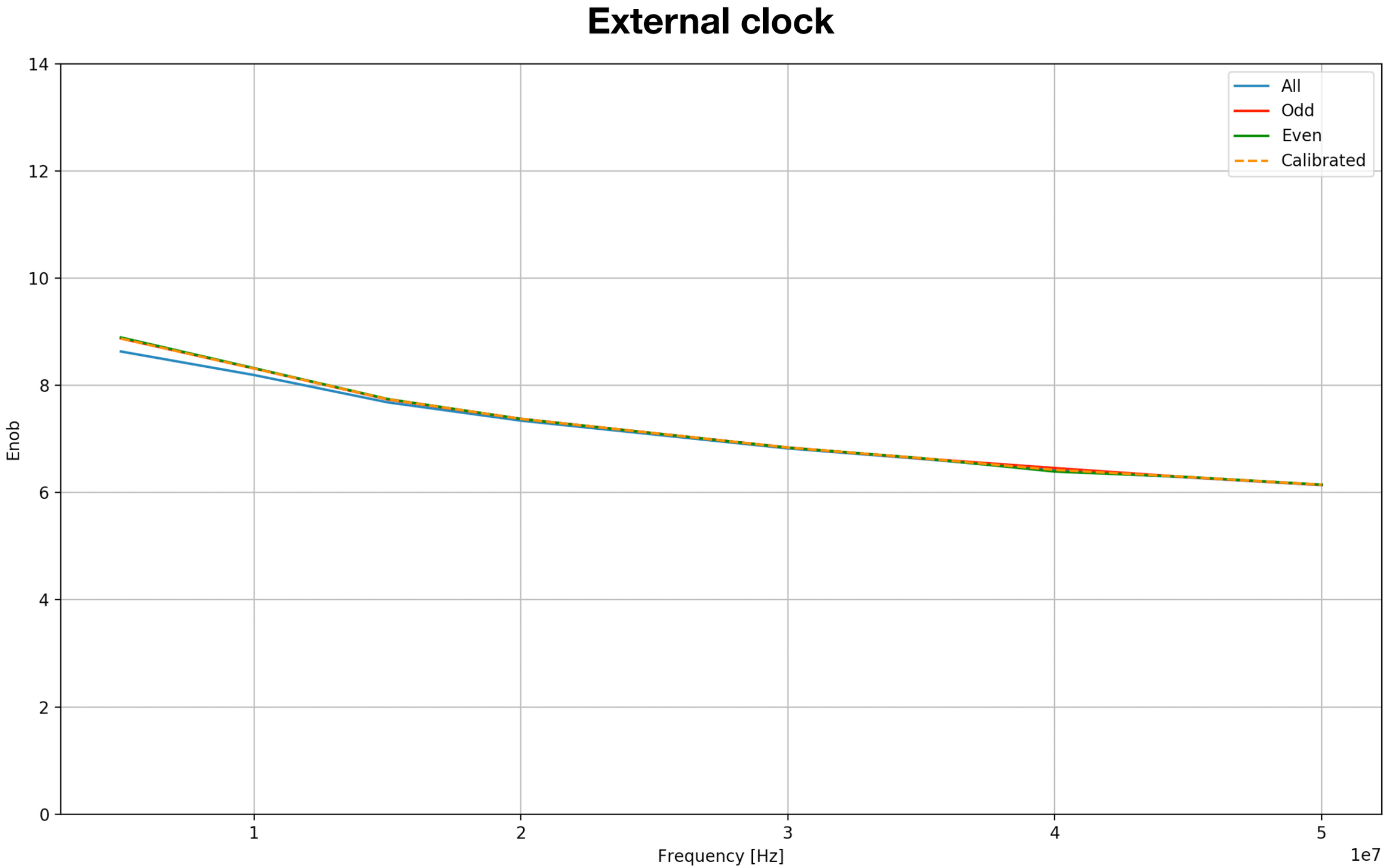
$$\mathrm{NAD} = \sqrt{\frac{1}{M}\sum_{n=1}^{M}(x[n]-x'[n])^2}$$

- Effective number of bits: ENOB: $\mathrm{Log}_2$[FullScaleRange / ($\sqrt{12}$ * NAD)]
- This method allow us to calculate the ENOB directly from the fit, avoiding to use the input voltage to the ADC, as the SINAD method requires. We don't have access to the input voltage to the ADC (the input wave given si attenuated by the filter, the drivers…)

# Scan board 2


Internal clock
All
Odd
Even
Calibrated
Enob
Frequency [Hz]
1e7
0
2
4
6
8
10
12
14
0
1
2
3
4
5

# Scan board 5 before irradiation



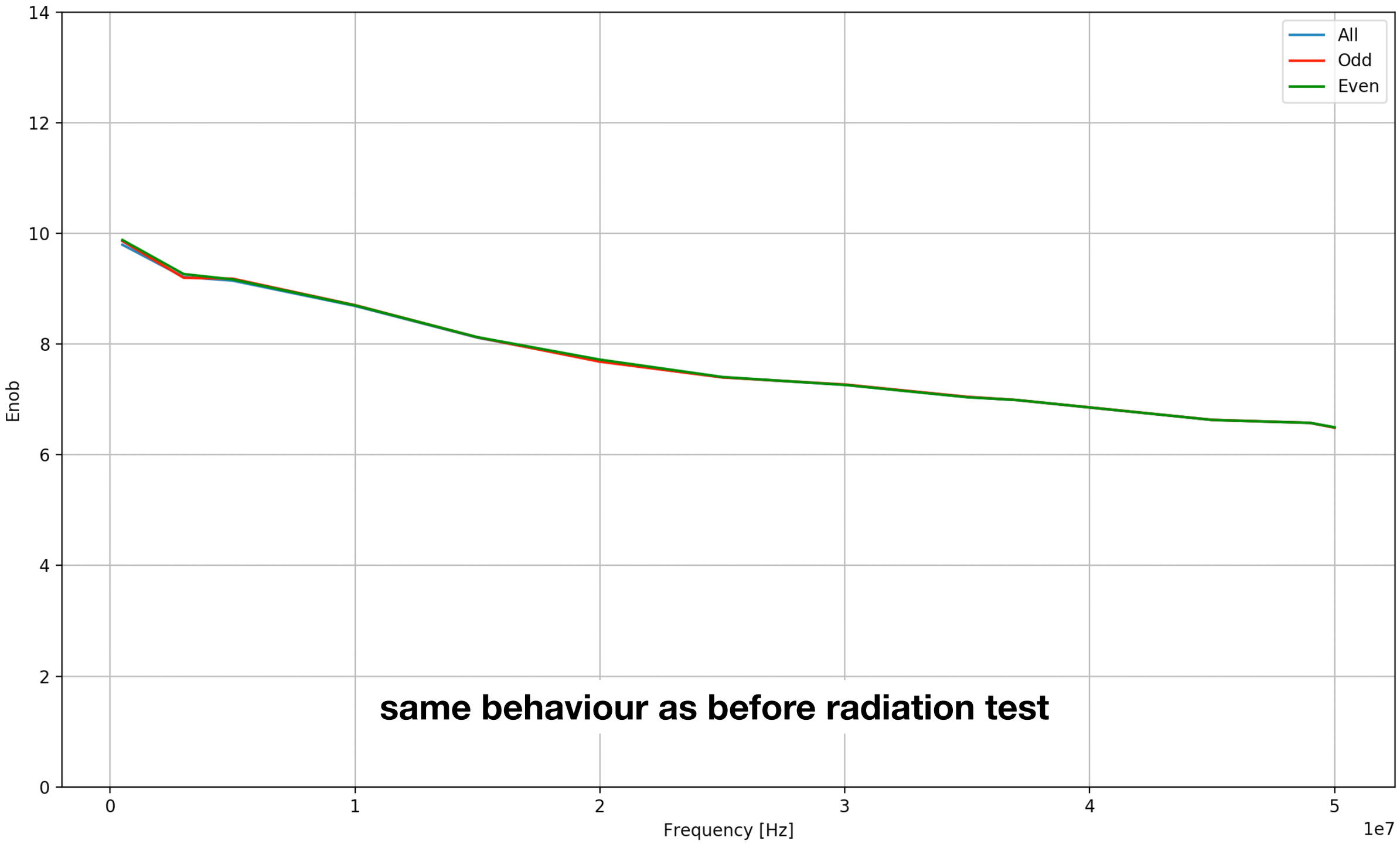
# Irradiation test

- We brought the board 5 to Padova, where there is a X-ray machine to irradiate the chip.
- We monitored the consumption of the components and the jitter of the PLL.

| | Analog [mA] | Digital [mA] | Drivers [mA] |
|---|---|---|---|
| **0** | 26 | 130 | 115 |
| **0.5 [MRad]** | 26 | 136 | 115 |
| **1 [MRad]** | 26 | 131 | 115 |
| **2 [MRad]** | 26 | 137 | 115 |
| **3 [MRad]** | 26 | 135 | 115 |
| **5 [MRad]** | 26 | 137 | 115 |

- We didn’t see any difference in power dissipation.

# Scan board 5 after irradiation



# Enob scan

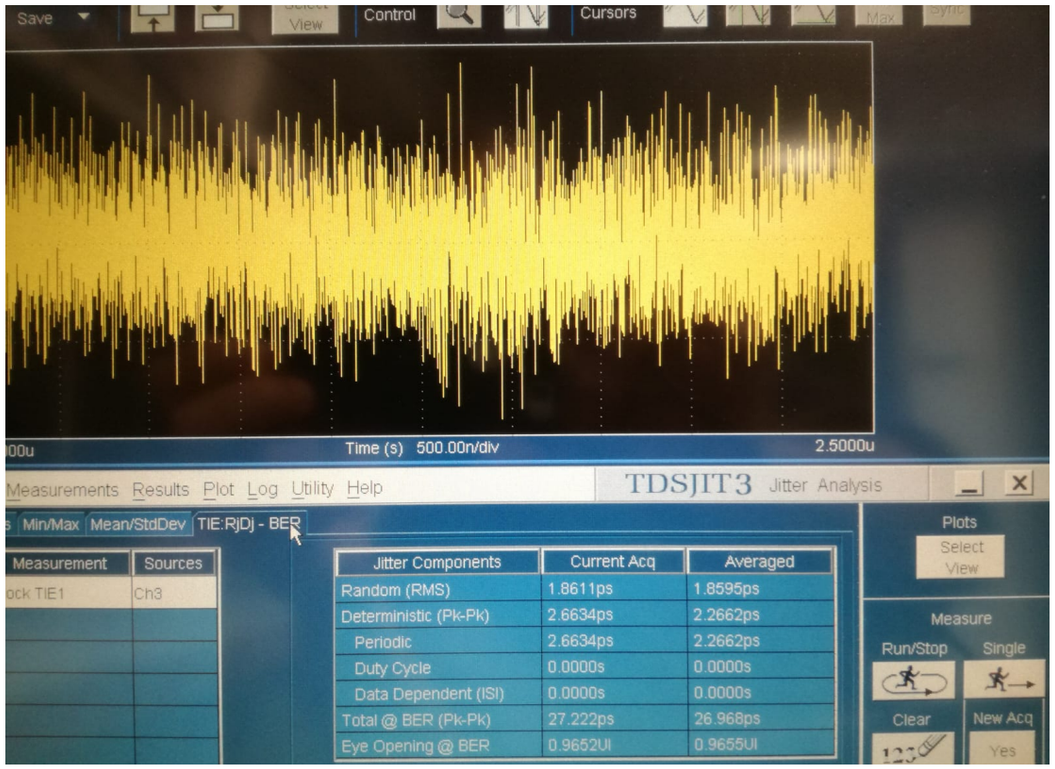
| Freq | Fit method $\omega$ fixed | FFT result | Fit method $\omega$ fitted |
|---|---|---|---|
| 500k | 9.79 | 9.88 | 9.89 |
| 5M | 9.14 | 9.06 | 9.24 |
| 10M | 8.70 | 8.63 | 9.14 |
| 15M | 8.11 | 8.12 | 8.76 |
| 20M | 7.69 | 7.74 | 8.43 |
| 25M | 7.40 | 7.47 | 8.21 |
| 30M | 7.26 | 7.20 | 7.97 |
| 35M | 7.04 | 7.02 | 7.86 |
| 37M | 6.99 | 6.93 | 7.87 |
| 45M | 6.67 | 6.60 | 7.51 |
| 49M | 6.57 | 6.55 | 7.44 |
| 50M | 6.49 | 6.48 | 7.34 |

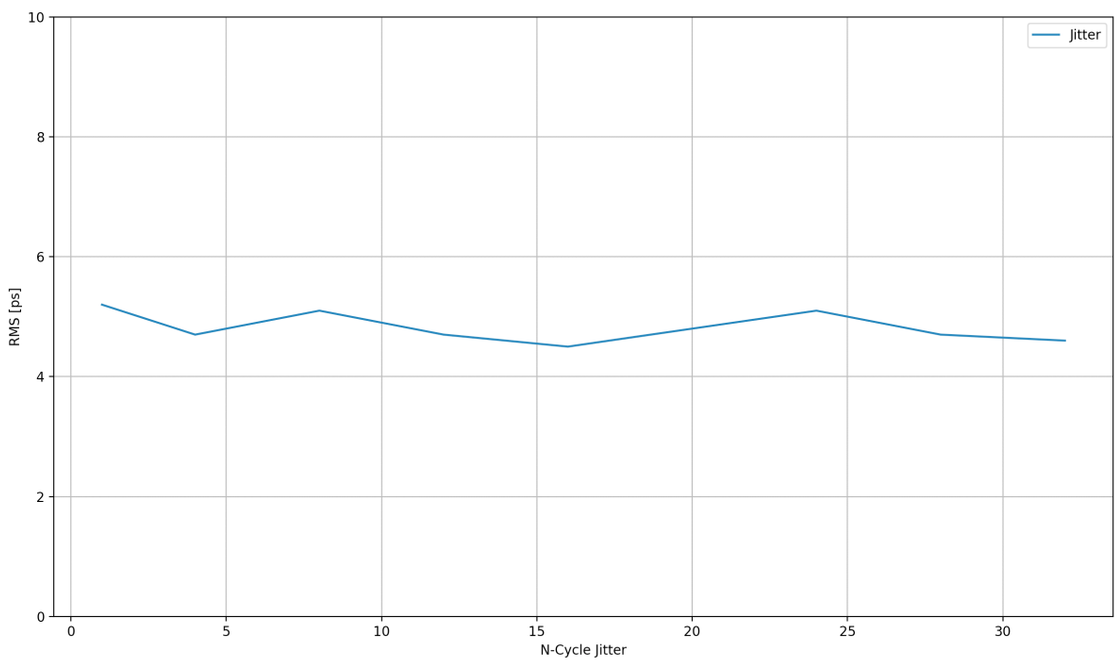
**Fit settings: [Amplitude]*TMath::Sin([Omega]*x+[Phase])+[Offset]**

**Omega = 2π * $freq_{in}/freq_{sampling}$ Period in units of samplings**

# Clock generator performance

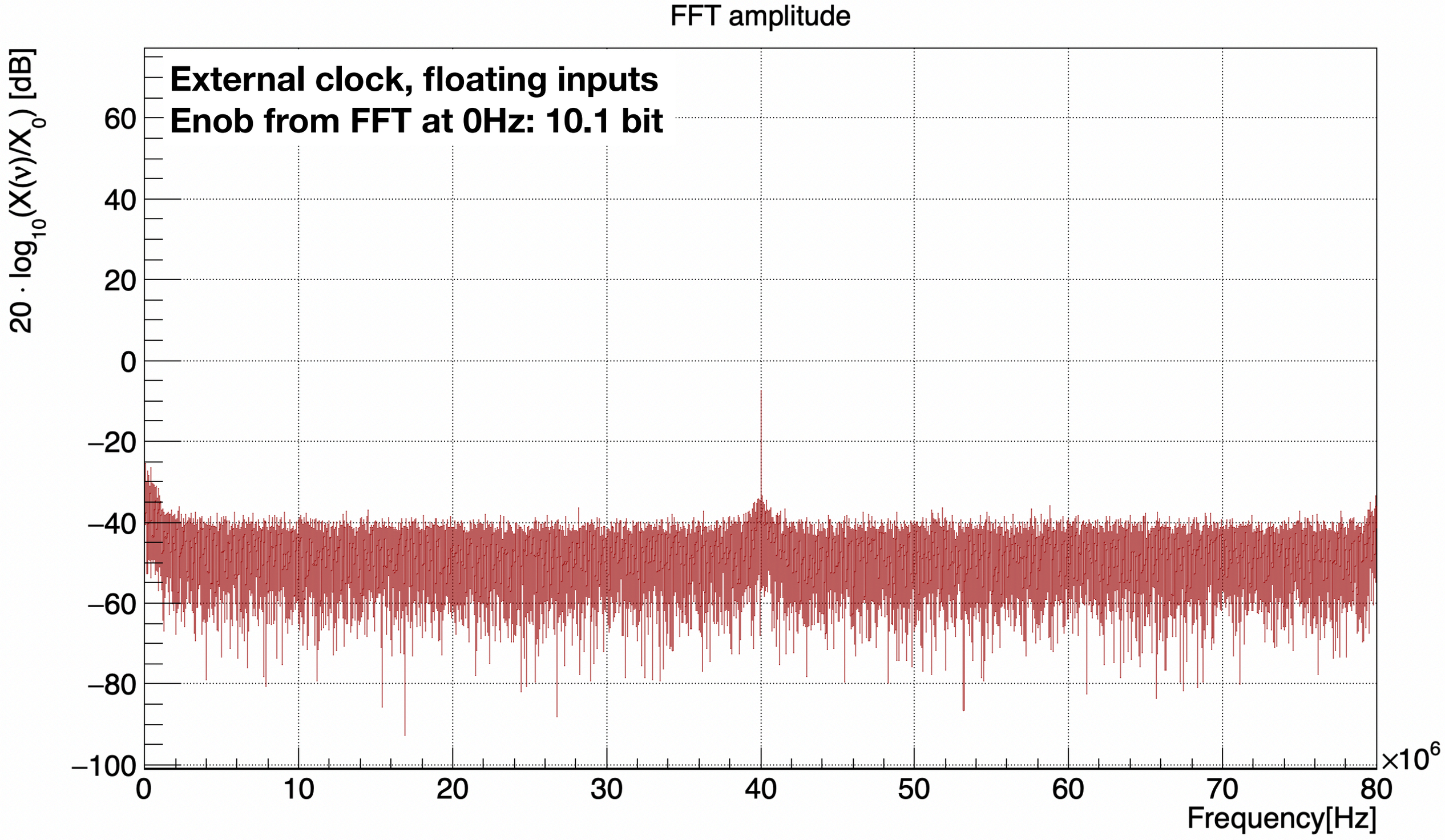
**The clock generator is used to inject the external clock to the ADC.**



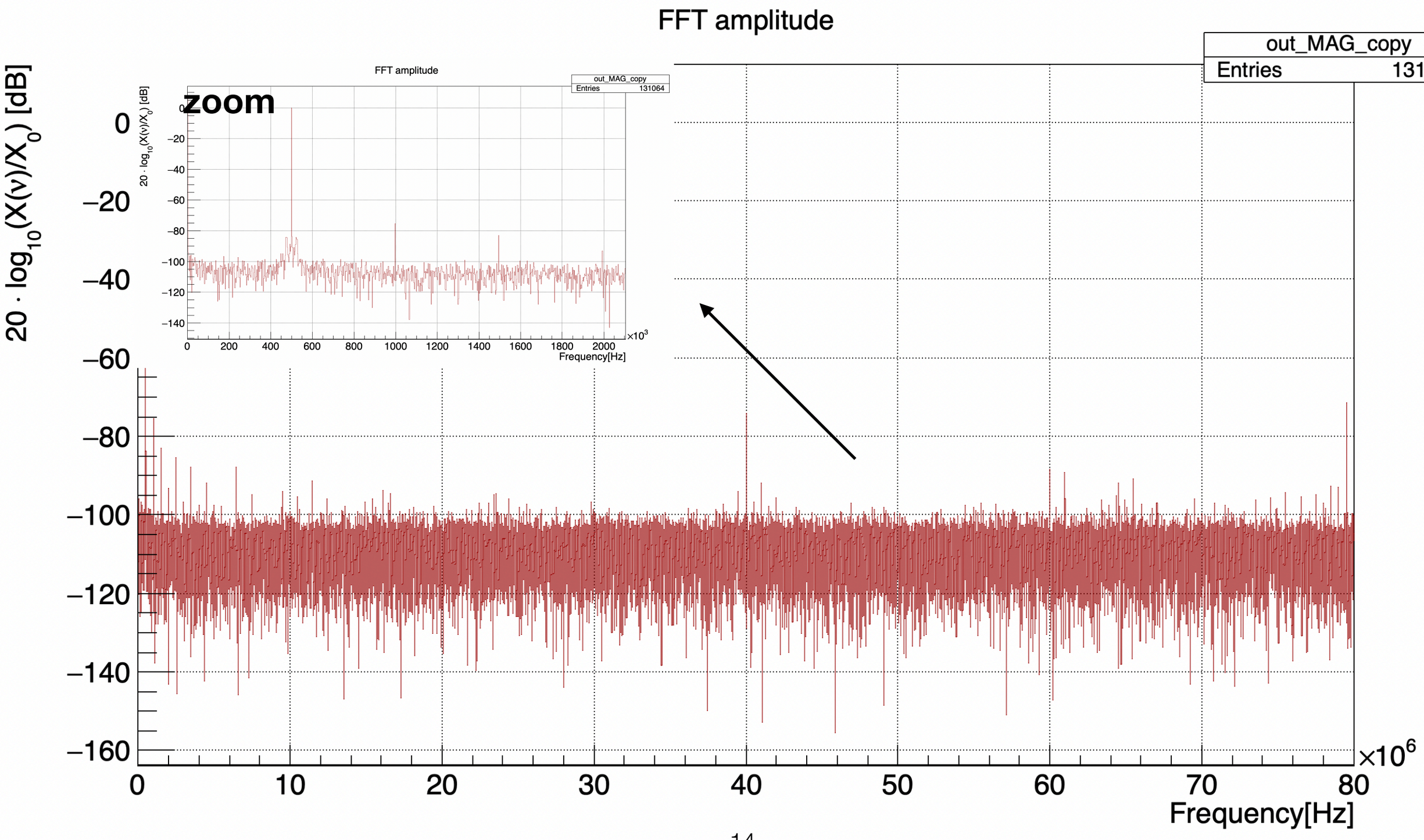




- Results from Tektronix DPO70604.
- Jitter (RMS): ~1.8 ps
- Deterministic Jitter (Pk-Pk): ~2.3 ps
- Period jitter (RMS): ~2.9 ps: jitter between two rising edges.
- Cycle to Cycle jitter: ~5.1 ps: simple arithmetic to the period measurements just taken. The difference between two adjacent periods is the cycle-to-cycle change: period one minus period two.
- N-Cycle jitter: N*(Cycle to Cycle).
- N-Cycle jitter: stable changing N

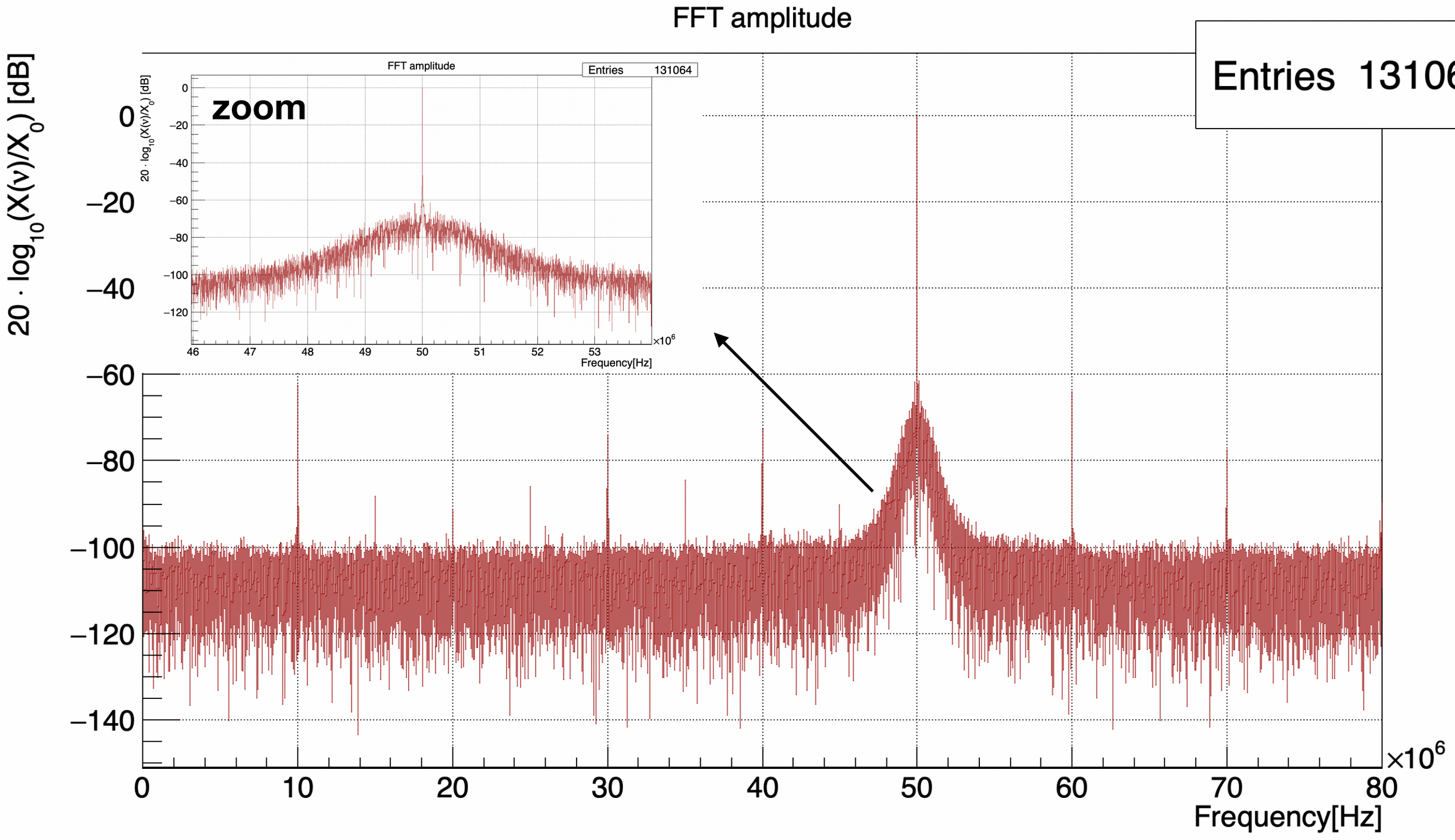
# FFT - 0Hz


FFT amplitude
External clock, floating inputs
Enob from FFT at 0Hz: 10.1 bit
20 · log10(X(ν)/X0) [dB]
60
40
20
0
−20
−40
−60
−80
−100
0
10
20
30
40
50
60
70
80
×10^6
Frequency[Hz]

# FFT - 500kHz


FFT amplitude
out_MAG_copy
Entries 131064
zoom
$20 \cdot \log_{10}(X(\nu)/X_0)$ [dB]
Frequency[Hz]
$\times 10^3$
$\times 10^6$

# FFT - 50MHz


FFT amplitude
Entries 131064
zoom
$20 \cdot \log_{10}(X(v)/X_0)$ [dB]
Frequency[Hz]
$\times 10^6$

# Conclusions, outlook and questions

- We learnt how to acquire data from the board in stable conditions.
- We obtain promising results from the ADC at low frequencies.
- We see a dependence of the ENOB value as a function of the frequency.

- When we calibrate the ADC using +900mV, +300mV, we see a ~1 lsb between even and odd samples. Is that expected?
- The Enob degrades vs frequency, both with internal and external clock. Can be this due to aperture jitter?
- Do you have hints on the origin of the peak broadening at 50 Mhz in the FFT? Balun?
    - (we plan to bypass it and use differential input)
- Which method do you think is most reliable for the ENOB measurement vs frequency?
- Operatively, how can we organize the tests at S3?

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# Spares

# Details of experimental setup

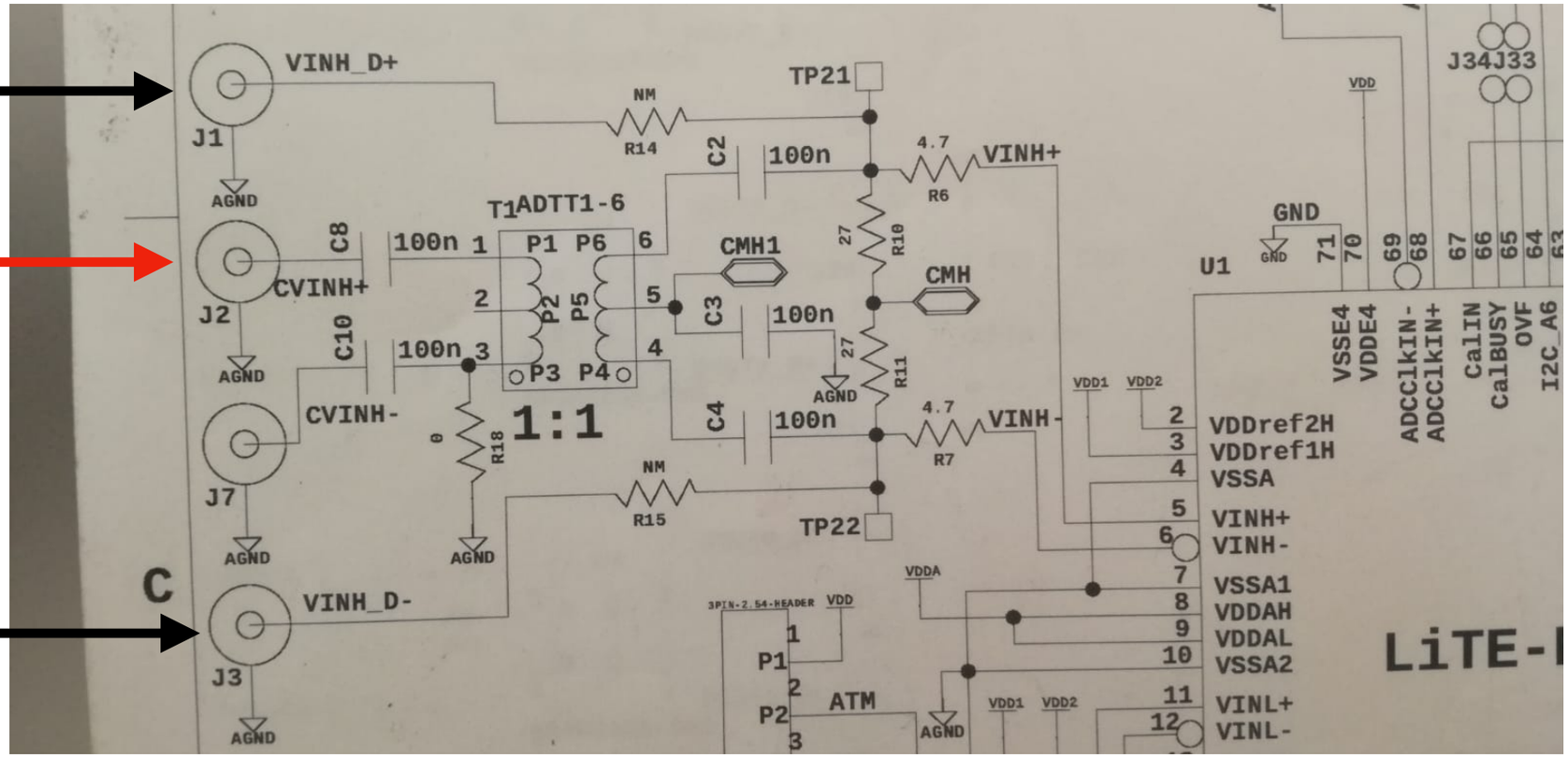
- Power supply Kenwood PWR18-18Q.
- Power supply Agilent E3631A.
- Power supply Rode Schwarz NGE100.
- Clock generators Stanford Research System CG635.
- Waveform Generator Teledyne T3AFG120.
- Oscilloscope Tektronix DPO70604.
- Osclilloscope Tektronix TDS 3054B.
- Xilinx Kintex Ultrascale.
- Custom clock splitter
- Level shifter texas instruments SN74AXC4T774.

# Bypass balun?

**Calib +900mV**

**Analog input**

**Calib +300mV**



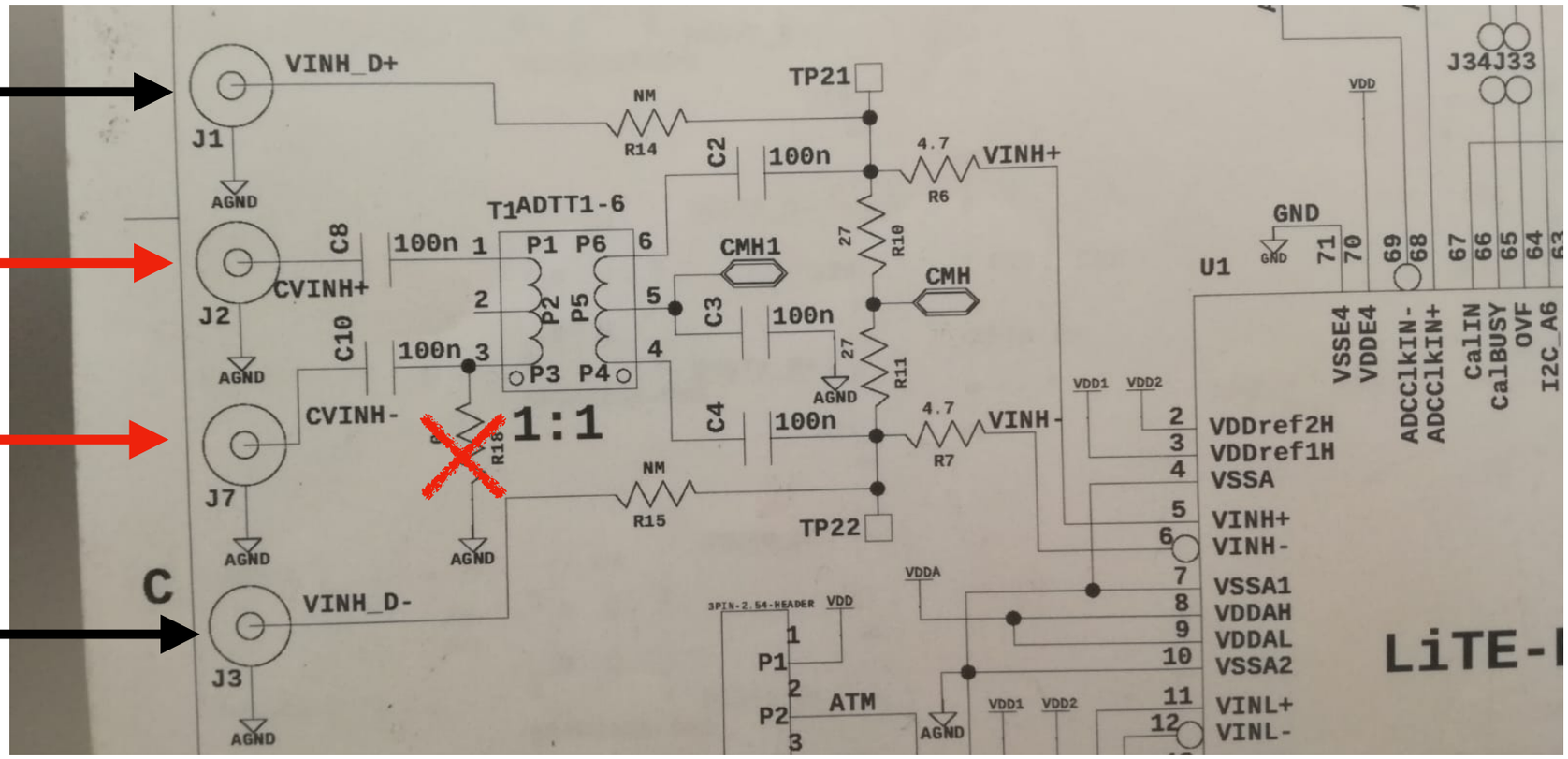
# Bypass balun?

**Calib +900mV**

**Analog input +**

**Analog input -**

**Calib +300mV**



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**Calib +900mV**

**Analog input +**

**Calib +300mV**

**Analog input -**