UK Activities on pixels.

(Previous report at Frascati, Dec 2009)

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Overview

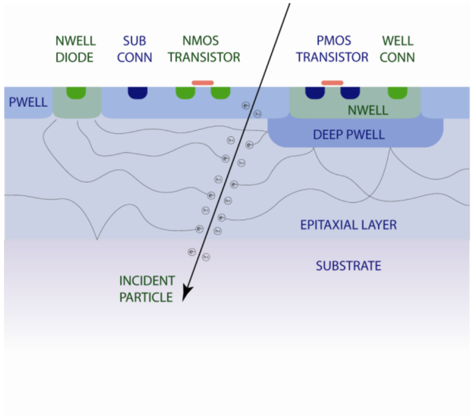
- Brief Reminder of the concept:

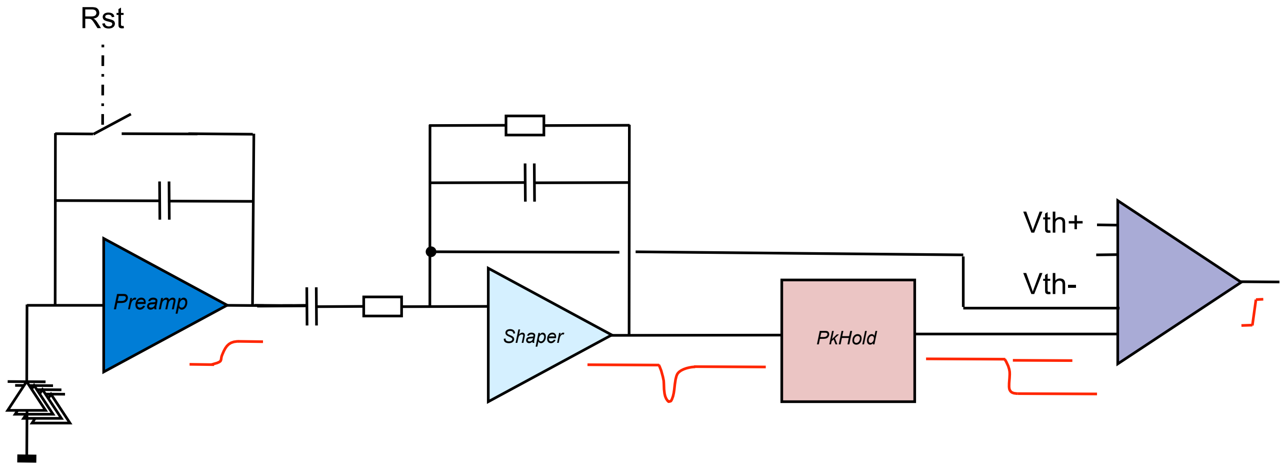
- Work since Frascati:
  - Discussions with Pisa (March)
  - Material Budget
  - Geometries: Long Barrel
    Lampshade

- To Do... (a long list):
  - Chip
  - Support
  - Physics studies

TPAC-style sensor for SuperB

- Deep p-well pixel design (derived from TPAC).
- On pixel preamp, shaper, peak hold.



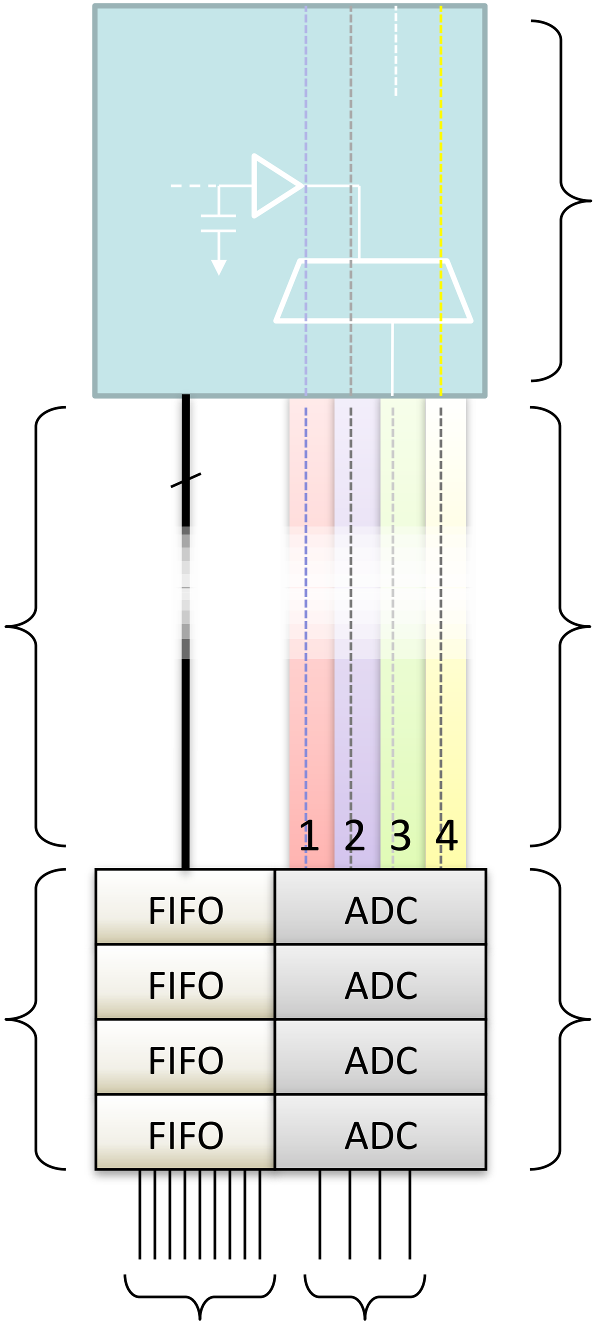


The PeakHold keeps data until pixel can be readout/reset.

~12μW static power per pixel.

- Token seek readout logic.
- 5bit Ramp ADC per column of pixels to provide some dE/dx information (need to evaluate the impact from this).

J. Crooks



Hit Pixel

One digital read channel
- Digital bus
- Records row address of each token location

Four parallel read channels
- Token seek logic
- Analog read line

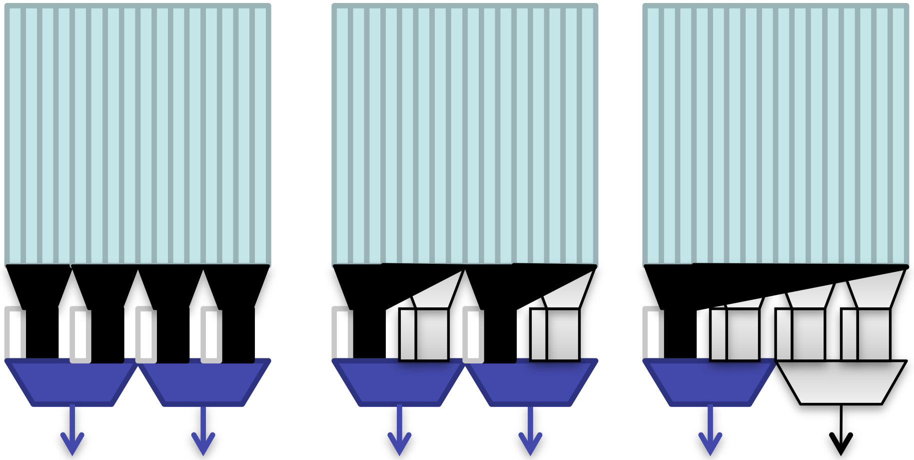
Row Data FIFO
- 4 stages

Pipelined ADC
- 4 stages

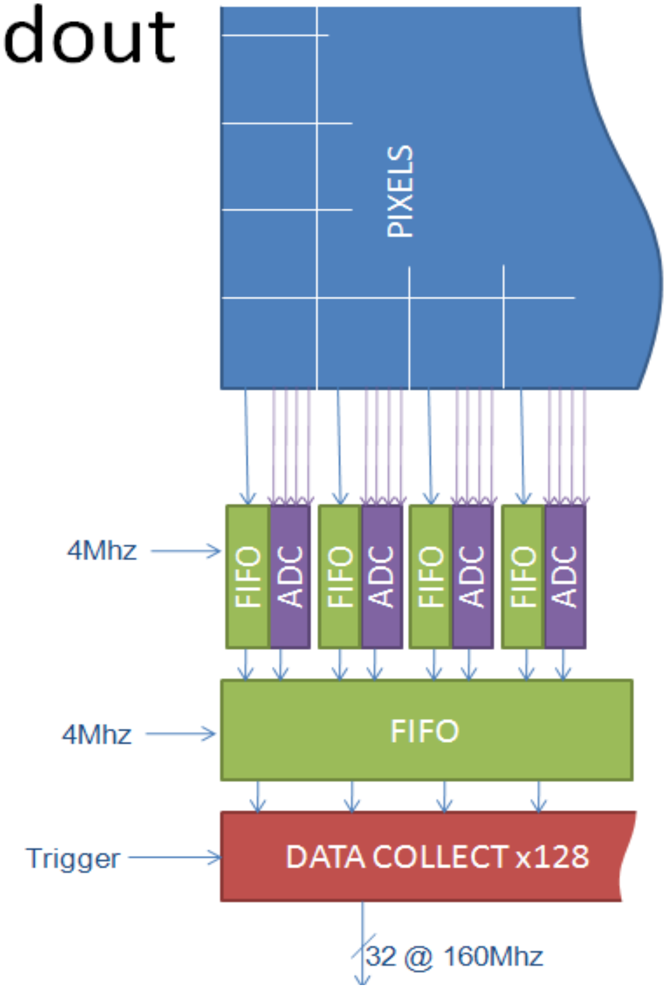
Row Addr Hit Data

TPAC sensor for SuperB

- Data rates from Layer 0 are very high
  - Consider an on-chip FIFO with external veto /trigger to reduce data volume
- Data rates from outer layers are much lower
  - Consider a column multiplexer circuit that allows ADCs to be shared while others are powered down in outer layers
  - Could use the same ASIC design with less connections (bonds) for outer layers?

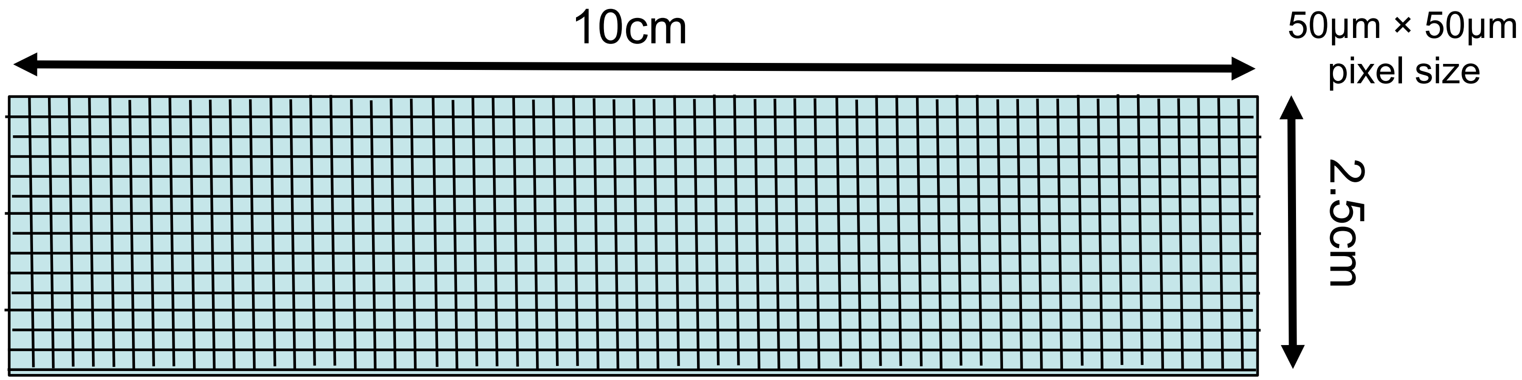


Readout



Sensor module for SuperB

- Alter layout of the chip: ($4 \times 2.5 cm^2$ chip stitched together)
    - 1 module = a 10cm × 2.5 cm × 50μm sensor.

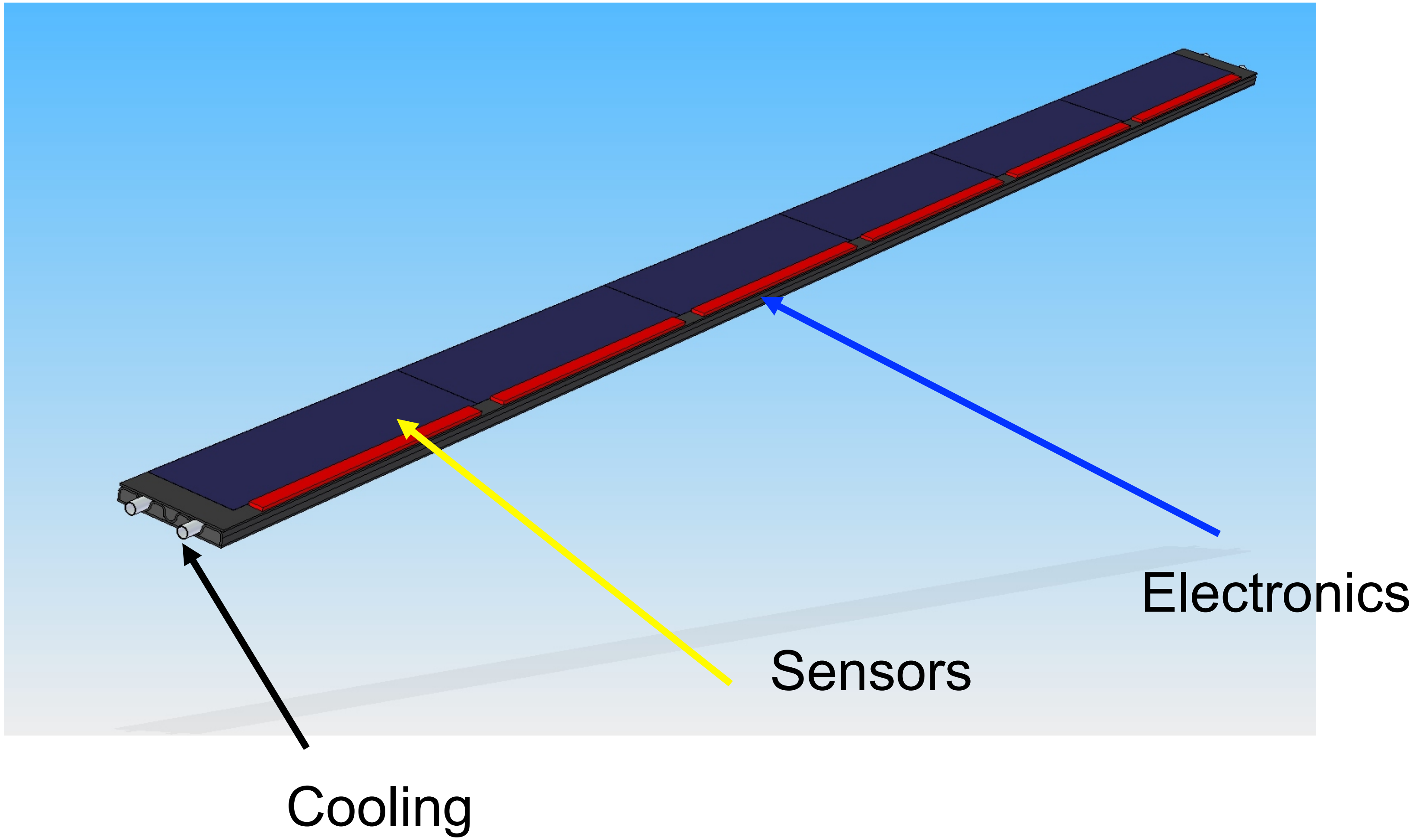


- Radiation hardness should be acceptible~10^{13} n/cm^2.

- 10 W power per module: < 5KW per 6 layer SVT.
    - Requires active cooling.
    - Ramifications for:
        - Material Budget.
        - Utility hook-up (cooling/power/readout).

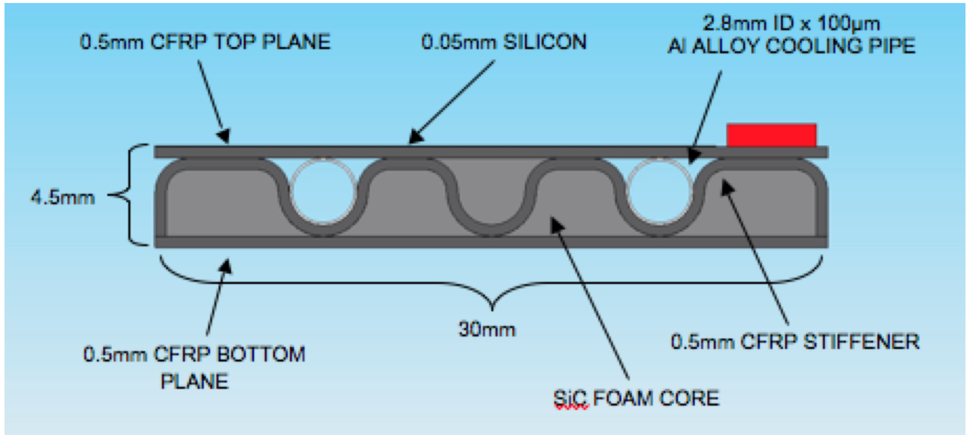
Stave Drawings

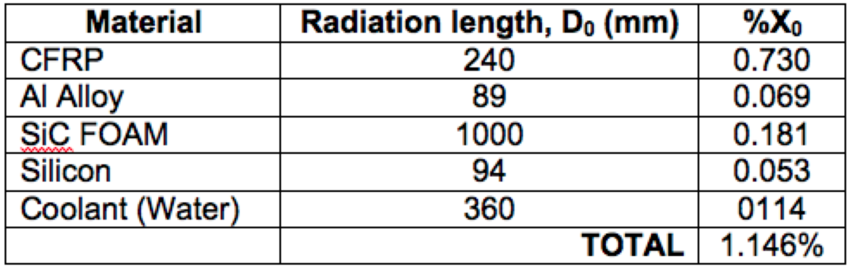
Concept: use staves as a basic unit for assembly of the detector.
Design a rigid stave to be supported from the ends, with minimal saggital sag (250um).



Material Budget: Some initial studies

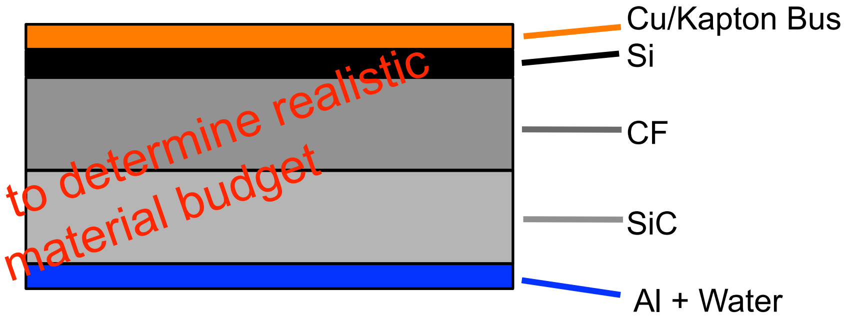
- Made first go at Stave structure
- Sandwich
  - Silicon 50 microns
  - Carbon Fiber
  - Silicon Carbide Foam
  - Aluminum Cooling pipes
- Current Material budget
  - 1.1 % per stave
  - Dominated by carbon fiber
- Very conservative design
  - Will be reduced after more FEA studies
- Expect bus material is about 250μm of Al/Kapton bus (as in FastSim for other solns.).





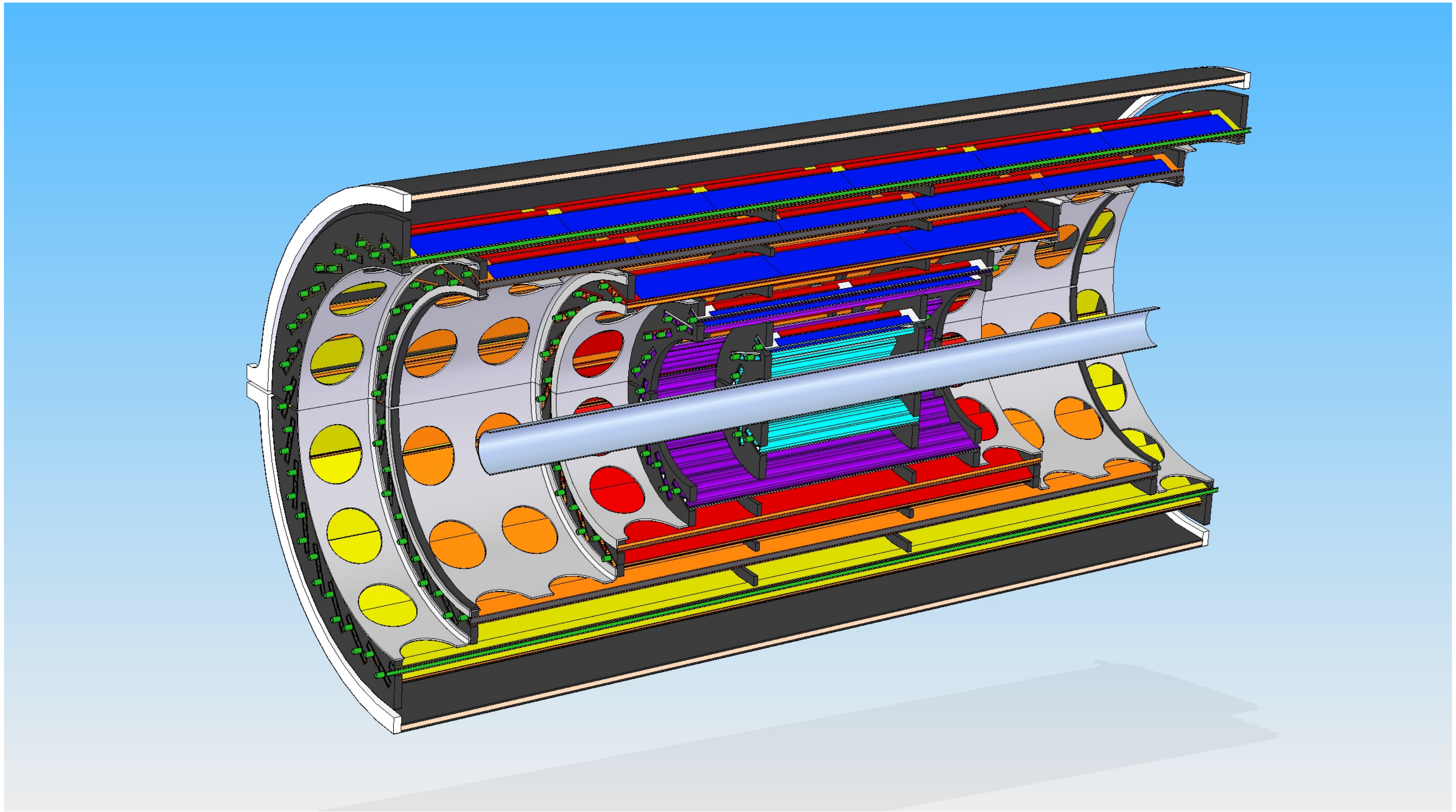
Material	Radiation length, D_0 (mm)	$\%X_0$
CFRP	240	0.730
Al Alloy	89	0.069
SiC FOAM	1000	0.181
Silicon	94	0.053
Coolant (Water)	360	0114
	TOTAL	1.146%

(Material thickness averaged over section of stave)



Need to determine realistic bus material budget

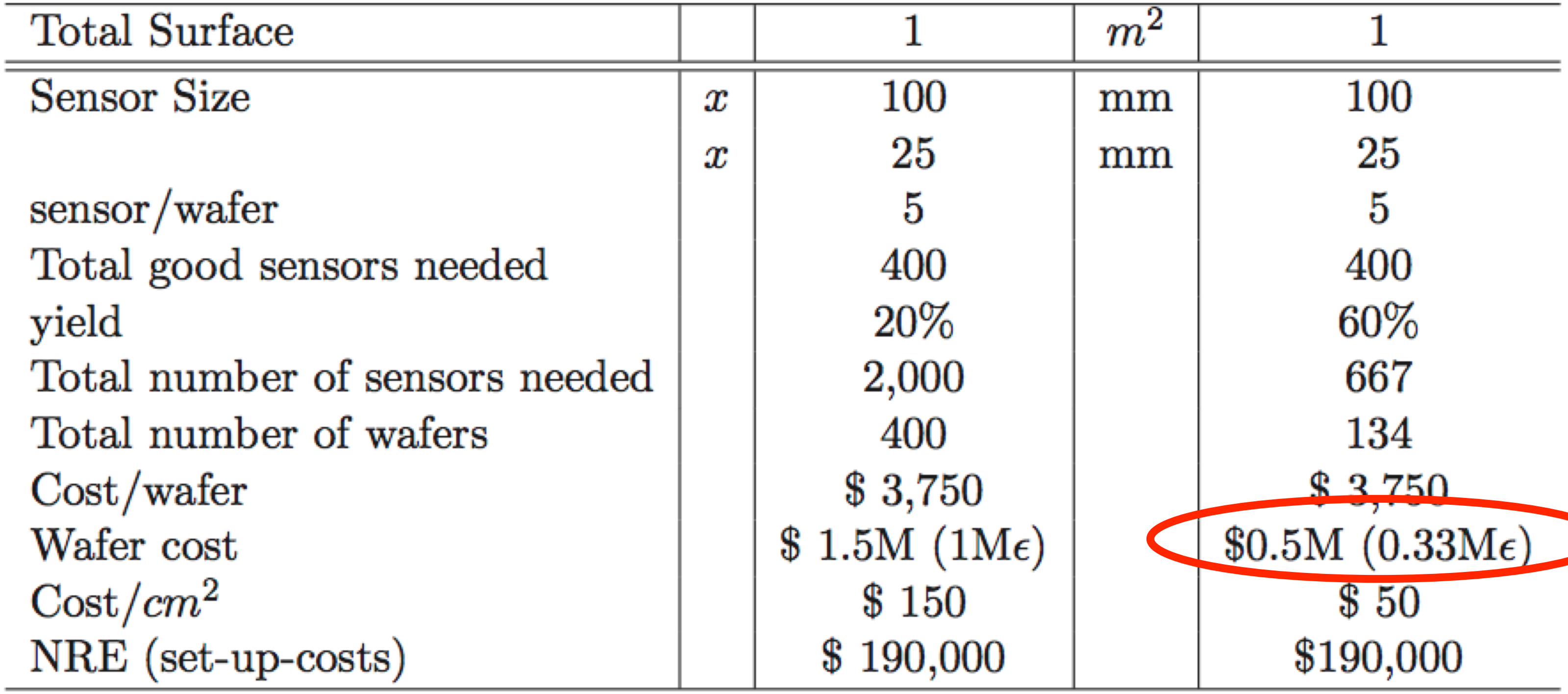
Mechanical Layout



The Lamp-Shade geometry can be adapted from this design – need to try barrel vs LS optimization studies to quantify any gains.

Costs

- Expect a yield of ~60%
  - This is based on previous experience with this foundry.
  - Expect sensor cost of \$0.5M / 330K€.



Total Surface		1	m^2	1
Sensor Size	x	100	mm	100
	x	25	mm	25
sensor/wafer		5		5
Total good sensors needed		400		400
yield		20%		60%
Total number of sensors needed		2,000		667
Total number of wafers		400		134
Cost/wafer		\$ 3,750		\$ 3,750
Wafer cost		\$ 1.5M (1Mϵ)		\$0.5M (0.33Mϵ)
Cost/cm^2		\$ 150		\$ 50
NRE (set-up-costs)		\$ 190,000		\$190,000

Discussions with Pisa

- Marcel Stanitzki, Fergus Wilson, AB recently visited Pisa.

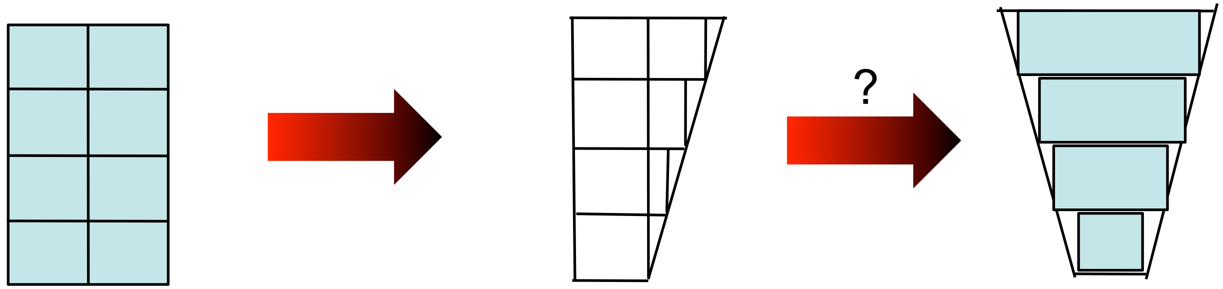
  - Extremely useful meeting – many ideas exchanged.
    - Concepts for lighter support structure.
    - Geometry of the detector, and how to realise this.
    - Visited the Pisa facilities to see the status of their R&D.

  - Detailed list of things to investigate between now and the end of the TDR period (see later).

  - Outlined a path for tighter collaboration between UK and Italian efforts.

To Do List

- Work on the chip:
  - How can we make LS end modules?



Easy to fabricate

Not so clear cut

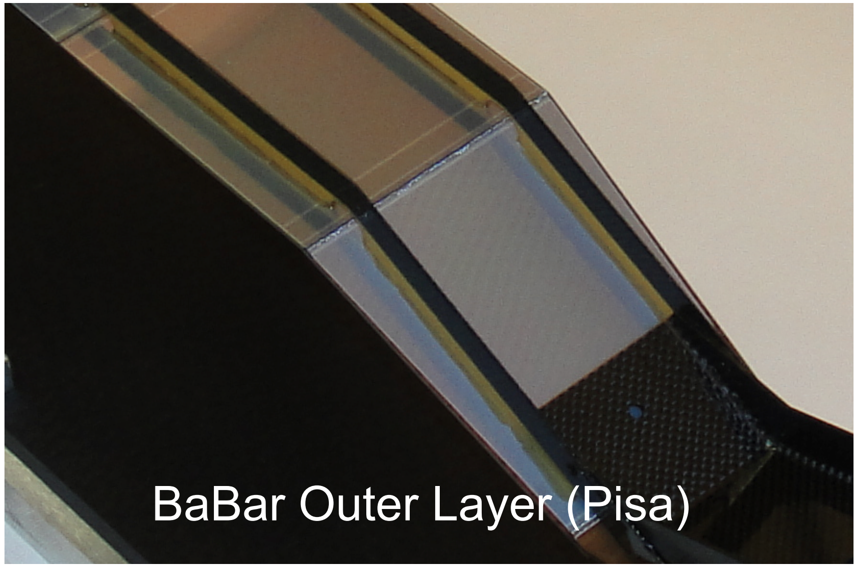
Easy

Started to think about geometry issues for the tapered ends of the LS setup.

Bus cable is a solvable issue

The CMOS structure – especially with stitching is a little more complicated...

- While it is easy to make trapezoidal sensors with strips; this is harder for INMAPS.
- Can make a variant on Rectangular geometries.

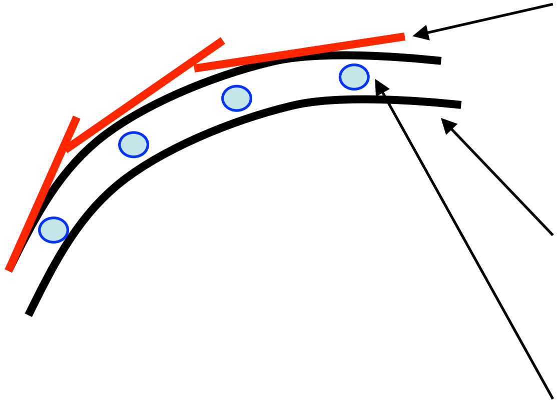

BaBar Outer Layer (Pisa)

To Do List

- Work on the Chip:
  - Radiation hardness.
  - Power consumption vs. hit rate.
  - Signal resolution as a fn of incident angle.
  - Usefulness of dE/dx measurement from 50um of silicon (Re: ADC).
  - Power distribution/signal bus over 30cm (utilities issue) & do we need coupling capacitors over this length.
  - Cooling over 30cm (utilities issue)

To Do List

- Work on the mechanics: L0 off bellows, L1-N off cryostat
  - How much material in the bus.
  - What is the material budget for inner/outer layers (between 0.2 and 1.14%).
    - Half shell space-frame geometry with overlapping sensors to minimize material budget?



Retain pinwheel for the silicon sensors (50um thick).

Superstructure would support sensors at ends (struts in the middle as/if needed).

Cooling infrastructure would support the sensor along z (into page).

    - What would the material budget of this be vs. stave design?

To Do List

- Work on physics studies:
  - Study low level information on particle tracking: d_0, ...
  - Low momentum tracking performance
  - Affect on θ_C resolution in DIRC from material.
  - Study a number of modes to see how each design choice affects the potential output:
    - $\pi^+\pi^-$, $\pi^0\pi^0$, D*X (soft pions), D-mixing (at 4S and threshold), τν &/ Kνν [aim to define Barrel and LS geometries in Fast Sim to check signal performance]
  - Study the material budget as a function of θ, etc. ... using particle gun modes of FastSim and Bruno.
  - Physics benefit of r=1.3 vs. r=1cm.

Summary

- Already had some good ideas to go away and think about as possible variant concepts on the support.
    - A natural to tie in with work from Filippo Bosi.

- Now need to knuckle down and do some more work...

- Aim to define a long barrel and lampshade design for signal studies in the simulation programmes as soon as we define the amount of bus material.
    - As we understand the mechanics of the space-frame geometry, will put a geometry together on that as well.
- A lot of work to do!