DCH Readout Architecture

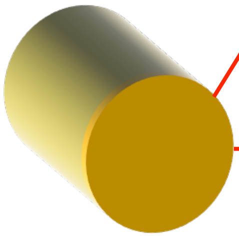
G. Felici

Outline

- *DCH FEE – Constraints/Estimate & Main Blocks*
- *DCH FEE – OL*
- *DCH FEE – KLOE-like scenario : on-detector electronics*
- *DCH FEE – KLOE-like scenario : off-detector electronics*
- *DCH FEE – BaBar-like scenario*
- *Conclusions*
- *Budget: KLOE-like scenario (very close to BaBar-like)*

DCH FEE – Constraints/Estimate & Main Blocks

DCH



Constraints & Estimate

- Trigger rate (150 kHz)
- Trigger/DAQ data format
- I/O BW
- Trigger Latency
- Minimum trigger spacing
- ….
- Chamber occupancy (25%)
- Chamber gain
- …..

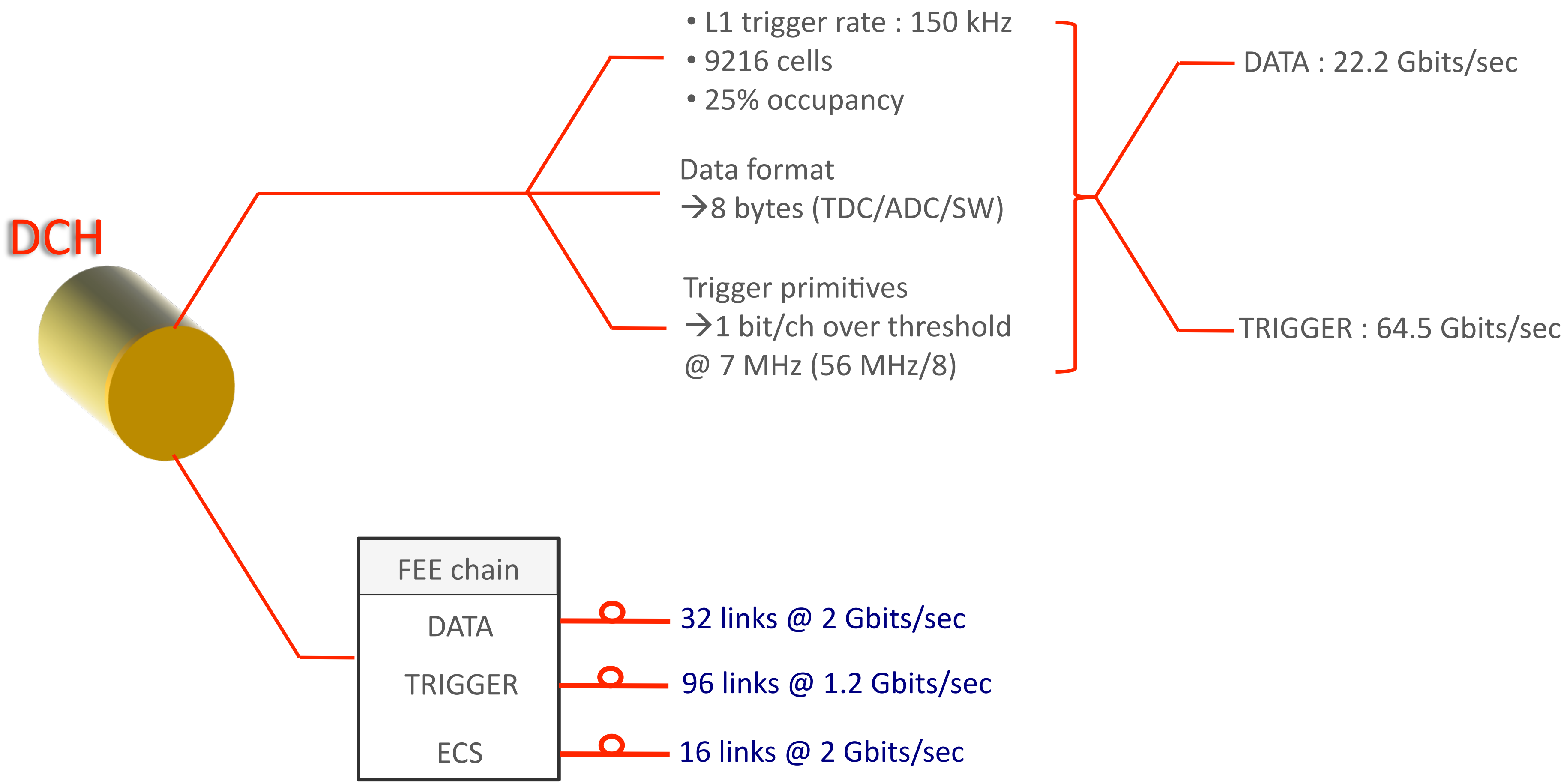
front-end

- minimize end-plate material & PD & RD issues (KLOE-like scenario) — Only preamplifier & HV distribution boards on end-plate
- minimize input/output connections (BABAR-like scenario) — Full fee chain on end-plate

main blocks

- Preamplifier & HV distribution boards
- ADB boards (charge & time information)
- ROIB boards (collects ADB data – implements sparse data scan & data reduction)
- DIOM (DAQ data concentrator)
- TIOM (Trigger data concentrator)
- ECS logic (shared width ROIB & DIOM – dedicated connections)
- HV filters boxes

DCH FEE – OL

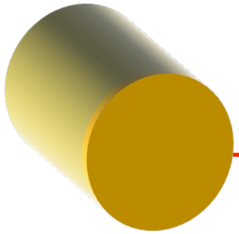


DATA : 8(bytes) x 8(bits) x 0.25(occupancy) x 9216(number of cells) x 150 kHz(L1 rate) ≈ 22.2 Gbits/sec

TRIGGER : 1(bits) x 9216(number of cells) x 7 MHz ≈ 64.5 Gbits/sec

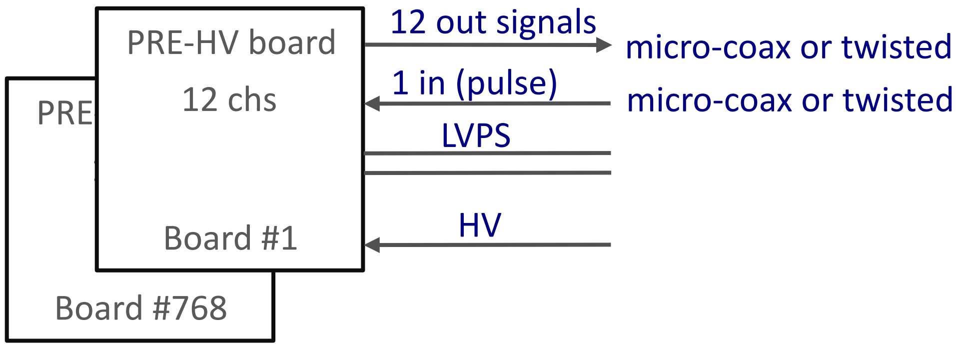
DCH FEE – KLOE like scenario : on-detector electronics

DCH



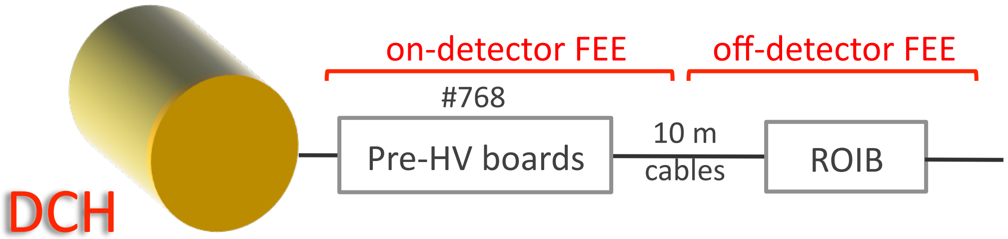
Only pre & HV distrib
boards on end-plate

- 768 pre & HV boards (12 chs)
- 9216 out cables (micro-coax or twisted)
- 768 in pulsing cables (micro-coax or twisted)
- 1536 LVPS cables
- 384 in HV cables (from HV filter boxes)
- PD (estimate) ≈ 200W → air flow cooling

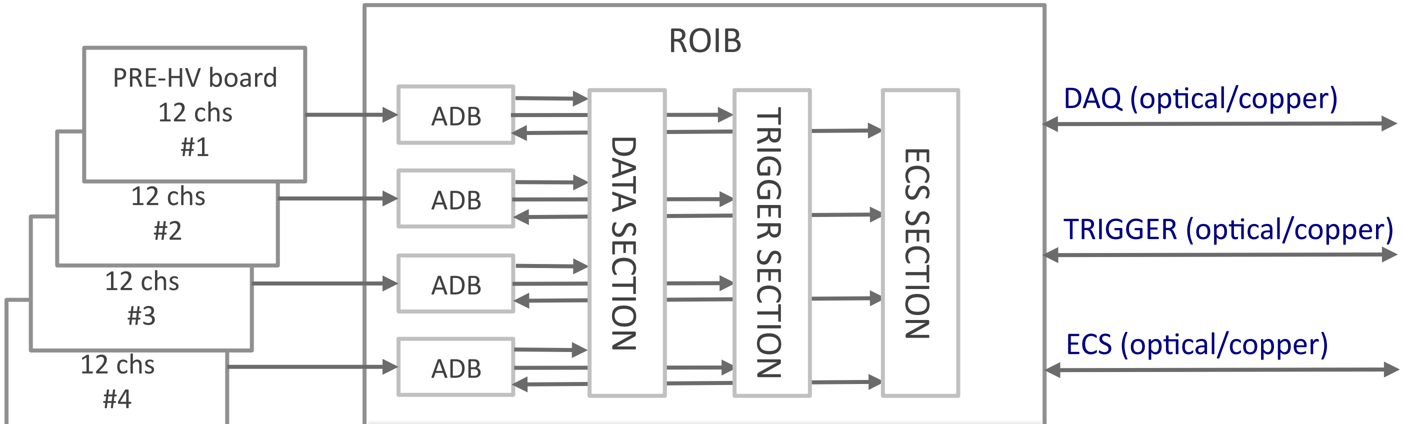


micro-coax KLOE experience : 18 x 2 mm^2

DCH FEE – KLOE like scenario : off-detector electronics (I)



- Hosts 4 ADB boards
- Receives 48 analog input signal
- Manages preamplifier boards (LVPS & pulsing)
- Manages ECS interface
- Generates both DAQ and Trigger data output
- Implements FEX on ADB data (≈ factor 4 in data size)



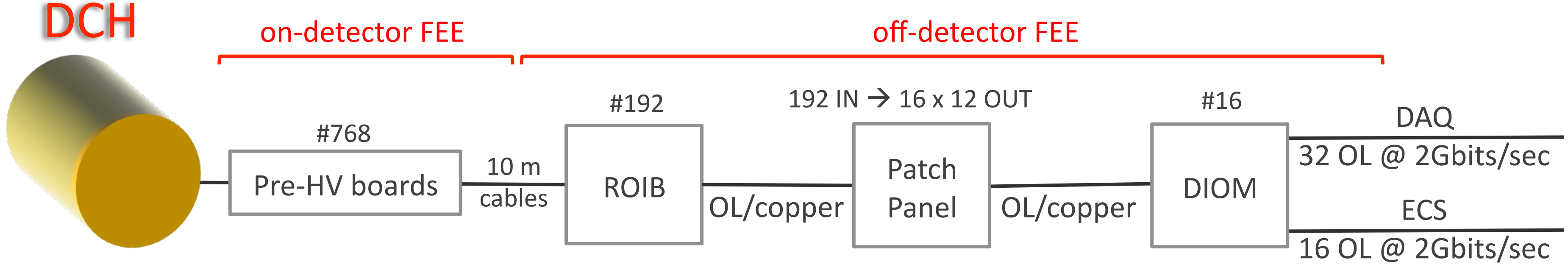
ADB
- sampled ADC value + TDC value (32 bytes)
- 32 samples @ 56 MHz ≈ 570 ns sampling period
- 12 bits trigger samples @ 7 MHz (56 MHz/8)

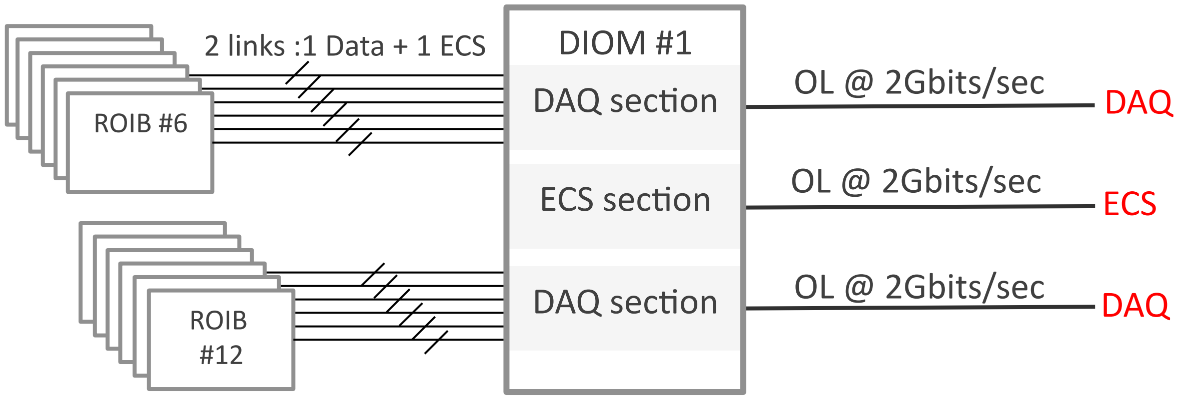
ADB (sparse data scan) → ROIB
- Data size : 12 channels/ADB
  - 12 (chs) x 0.25 (occupancy) x 32 (bytes) x 8 (bits) ≈ 768bits
- 8b data bus @ 56 MHz (448 Mbits/sec)
  - 224 Mbits/sec bus BW (***protocol overhead + FEX***)
- RO time : 615 (bits) @ 224 Mbits/sec ≈ *3.4 μs*

OR

ADB (sparse data scan) → ROIB (exploiting ADB latency buffer)
- Data size : 12 channels/ADB
  - 12 chs @ 25% occupancy ≈ 3 chs/ADB
- Processing the first pipeline event while writing the last the (FEX implemented in ADB)
  - 8 (bytes) x 3 (chs) @ 56 MHz (CLK) ≈ 1 μs (multiplexed RO - overhead included)

DCH FEE – KLOE like scenario : off-detector electronics (II)





ROIB (FEX) → DIOM (parallel RO)

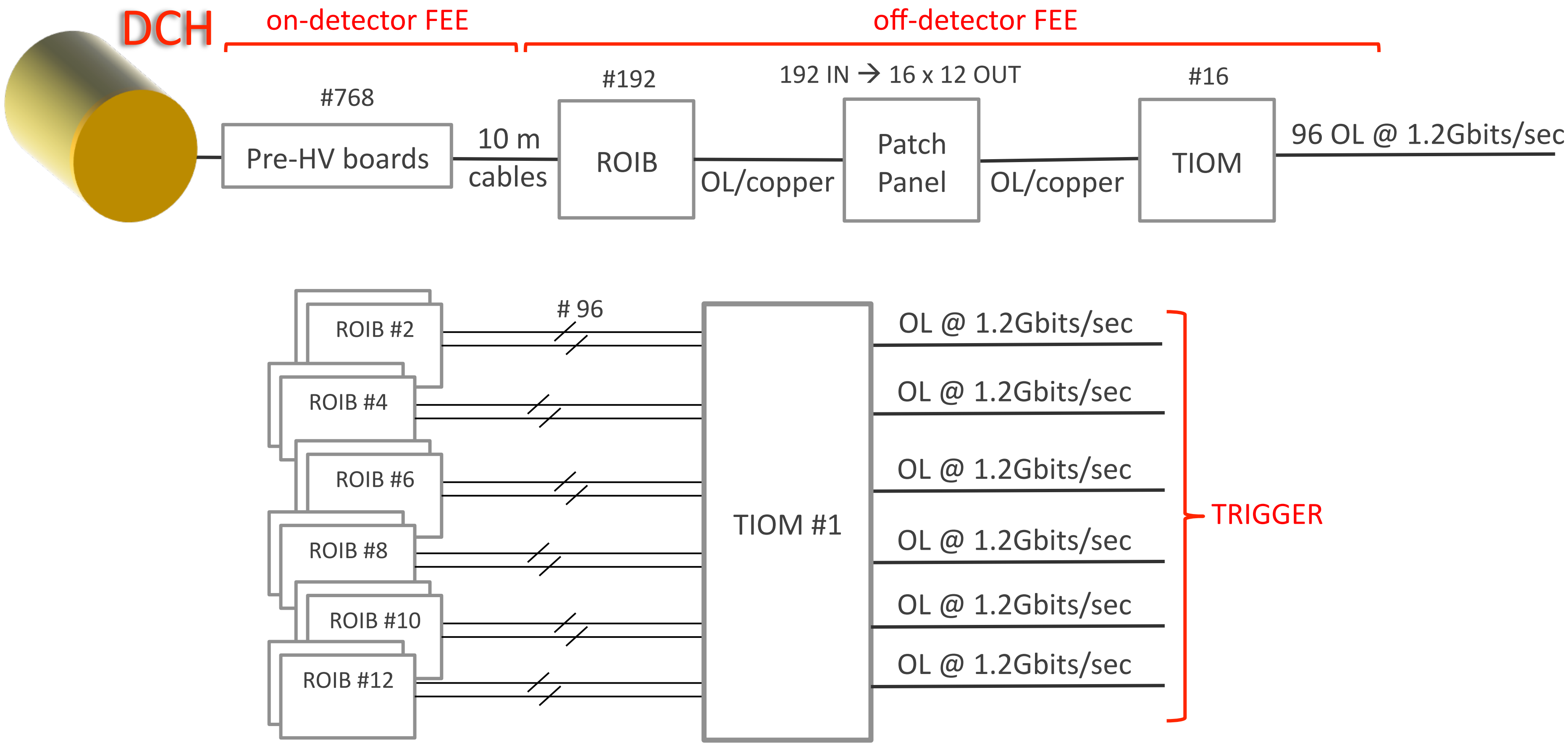
- Data size : 12 channel/ADB - 25% occupancy - 4 ADB
  - 3 (chs) x 4 (ADB) x 8 (bytes (FEX)) x 8 (bits) ≈ 768 bits
- 224 Mbits/sec data link (*using both edges of the 56 MHz clk – 2 bits bus)*
- RO time @ 224 Mbits/sec ≈ 3.4 μs

DIOM → DAQ

- 12 ROIB/DIOM (2 x 6 ROIB)
- Data size : 768 bits (ROIB event data out) x 6 (ROIBs) ≈ 4608 bits

DIOM data RO (2 Gbits/sec) = 2.9 μs (25% overhead included)

DCH FEE – KLOE like scenario : off-detector electronics (III)

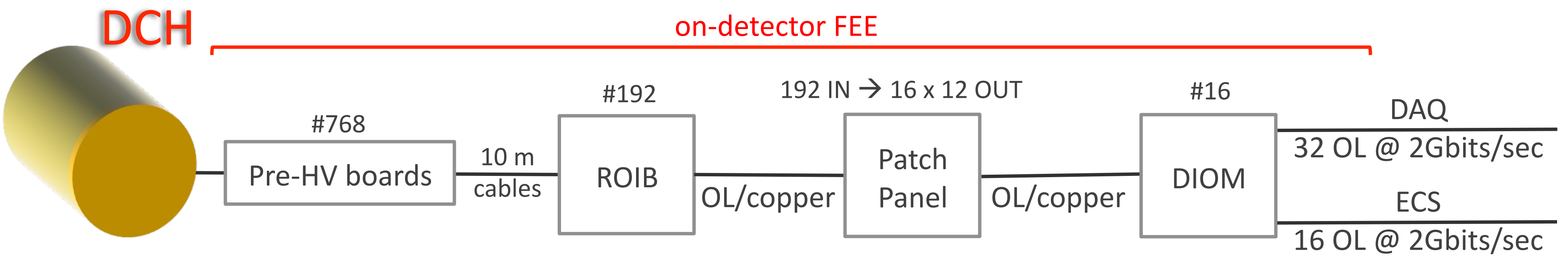


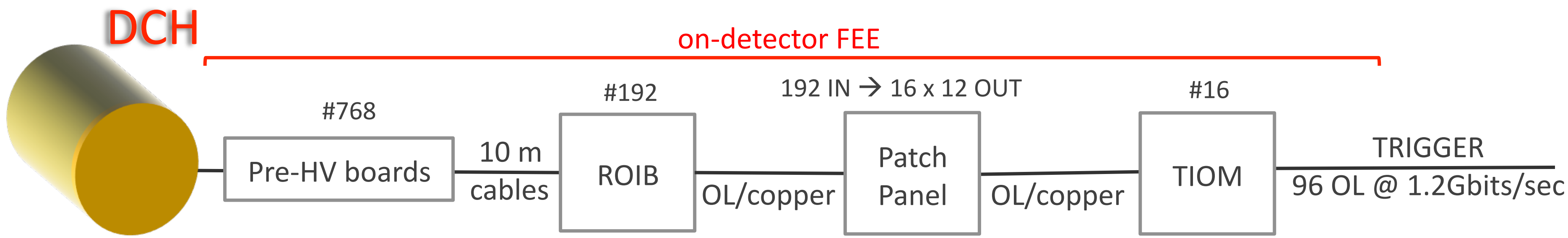
ADB → ROIB
- 12 channels/ADB
  - 12 (chs) x 1 (bit) = 12 bits
- 12 (bits) @ 7 MHz (56 MH/8) = 84 Mbits/sec

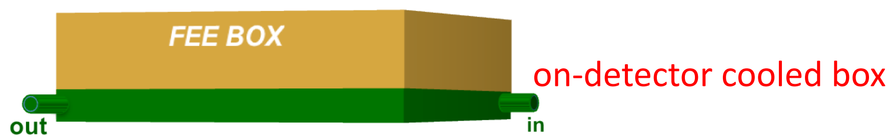
ROIB → TIOM
- 12 channel/ADB – 4 ADB
  - 12 (chs) x 4 (ADB) x 1 (bits) = 48 bits
- 48 (bits) @ 7 MHz (56 MHz/8) = 336 Mbits/sec
- 192 (ROIB) x 336 Mbits/sec ≈ 80.6 Gbits/sec (25% overhead included)

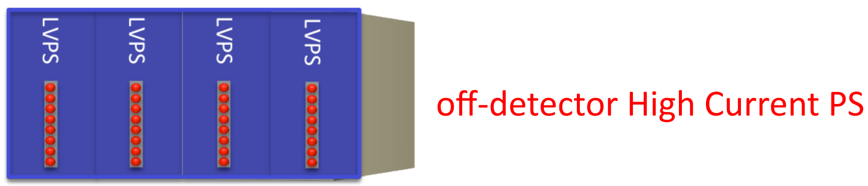
→ ***TIOM readout = 96 links @ 1.2 Gbits/sec***

DCH FEE – BaBar like scenario









Main concerns :

- Power Dissipation (≈ 1.5 kW)
- Material budget (boards/shielding/boxes/cooling/ support structure/LVPS cables)

Conclusions

- *DCH FEE layout has been outlined: 2 possible scenarios*
  - *Only Pre/Shaper on the end-plate*

    → We must foresee room for off-detector electronics (more than 20 crates)
  - *All FEE chain on end-plate*

    →Concerns about PD, material budget and radiation environment

- *To start real design some parameters (trigger average rate, trigger latency, minimum trigger spacing etc) must be defined*

- *As a huge amount of programmable logic will be used for apparatus readout a carefully (and hopefully common) study of FPGA devices behavior versus SEE & total dose should be carried out (LHC experiments experience + dedicated tests)*

- *Budget at this design stage is a guess more than an estimate ….*

Budget → KLOE like solution: on-detector electronics

1.7.2.1	*6-chs ASIC*	27,0	18,0	190,0	Preamplifier ASIC - 6/12 chs - (0.25u tech ?)
1.7.2.1.1	4 prototype runs ???? process	24	12	80	
1.7.2.1.2	Test bench setup	1	2	10	
1.7.2.1.3	Production - 2000 units	2	4	100	Time includes devices test
1.7.2.2	Preamplifier & HV distribution boards	4,0	8,0	61,0	4 layers preamplifier & HV distribution boards
1.7.2.2.1	Preamplifier & HV distribution board development	2	2	5	
1.7.2.2.2	Preamplifier & HV distribution board test bench	1	2	5	
1.7.2.2.3	Preamplifier & HV distribution boards production - 768 (+ 82 spares) units - 12 chs	1	4	51	60€/board - 10% spares included -Time includes device test
1.7.2.11	Cables to ADS (10 mt - microcoax)	1,0	2,0	34,6	18€/m - 12 signals
1.7.2.15	HV distribution	3	3	12	Cables + filters/distributors box
1.7.2.15.1	HV cables	1	1	5,4	18€/m - (16 cables + 4 spares) - 15 mt
1.7.2.15.2	HV connectors (multi-pin)	1	1	2	50€/connector - (2 connectors/cable) - (16 + 4 spares)
1.7.2.15.3	HV box filters - distributors (on-chamber)	1	1	4,2	16 filters/distributors box + 4 spares
1.7.2.16	Cables and PreHV board support structure	2	2	15	

Total ≈ 312 k€

Budget → KLOE like solution: off-detector electronics (I)

1.7.2.3	ADS boards	7,0	8,0	521,0	receives preamplifier analog signals and provides time, charge and trigger information - Daughter board for ROIB boards - ASIC development could be required - 8 layers board
1.7.2.3.1	ADS board development	4	2	6	
1.7.2.3.2	ADS board test bench	2	2	5	
1.7.2.3.3	ADS board production - 768 (+ 82 spares) units - 12 chs	1	4	510	600€/board - 10% spares included - Time includes device test
1.7.2.4	ReadOut Interface Board (ROIB)	7,0	8,0	266,0	Manages 4 ADS boards - Extract data from ADS if L1 is delivered - Send them to DATAIO boards and to TIOM modules - serial link (copper or optical) - manages ECS section (pulsing/ thresholds/sparse data scan etc) - 10 layers VME 9U board
1.7.2.4.1	ROIB development	4	2	8	
1.7.2.4.2	Test bench	2	2	6	
1.7.2.4.3	ROIB production - 192 (+ 18 spares) units - 48 chs	1	4	252	1200€/board - Each ROIB hosts 4 ADS - 10% spares included -Time includes device test
1.7.2.5	Trigger IO Module (TIOM)	6,0	7,0	31,0	Receives trigger primitive from 12 ROIB through serial link (copper or optical) - send them to Trigger System through 3 OL @ 1.2 Gbits/sec OL - 10 layers VME 6U board
1.7.2.5.1	TIOM development	4	2	6	
1.7.2.5.2	Test bench	1	1	5	
1.7.2.5.3	Production - 16 (+ 4 spares) units - 12 IN (48x12 chs) - 4 OUT (48x12 chs)	1	4	20	1000€/board - 10% spares included - Each TIOM manages trigger signals from 3 ROIB - Time includes device test
1.7.2.6	DATA Patch Panel	3,0	5,0	27,0	Groups single ROIB outputs connectors (copper or optical) - 192 in - 16(x12 chs) out
1.7.2.6.1	Patch panel development	1	2	5	
1.7.2.6.2	Test bench	1	1	2	
1.7.2.6.3	Production - 2 units	1	2	20	Data + ECS path

Budget → KLOE like solution: off-detector electronics (II)

1.7.2.7	Data IO Board (DIOM)	6,0	6,0	27,0	Receives data from 12 ROIB boards through serial link (copper or optical) - send data to DAQ - 2 Gbits/sec OL - 10 layers VME board
1.7.2.7.1	DIOM development	4	2	6	
1.7.2.7.2	Test bench	1	1	5	
1.7.2.7.3	DIOM production - 16 (+ 4 spares) units - 48x12 chs	1	3	16	1000€/board - 10% spares included - Each DIOM manages data signals from 12 ROIB - Time includes device test
1.7.2.8	Crates VME 9U - ROIB - 12 units	2,0	3,0	66,0	5500€/crate - custom backplane
1.7.2.9	Crates VME 6U - TIOM - 1 (+ 1 spare) unit	1,0	1,0	13,0	6500€/crate - standard
1.7.2.10	Crates VME 6U - DIOM - 1 (+ 1 spare) unit	1,0	1,0	13,0	6500€/crate - standard
1.7.2.11	Cables to ADS (10 mt - microcoax)	1,0	2,0	34,6	18€/m - 12 signals
1.7.2.12	HV System	2	2	112	3 crates + 20 boards (24 chas)
1.7.2.12.1	SY1527 (NO display - 16 slots)	1	1	18	6000€/m - 3 crates (2 + 1 spares)
1.7.2.12.2	A1535(like) board - 16 boards (+4 spares)	1	1	94	5000€/board
1.7.2.13	Optical Fibers	2	2	14,8	22€/fiber (5 m)
1.7.2.13.1	192			4,2	IN/Out ROIB - data path
1.7.2.13.2	192			4,2	IN/Out ROIB - trigger path
1.7.2.13.3	96			2.1	IN/Out TIOM - trigger path
1.7.2.13.4	32			0,7	IN/Out DIOM - data path
1.7.2.13.5	16			0,4	IN/Out DIOM - ECS path
1.7.2.13.6	192			4,2	IN/Out ROIB - ECS path

Total ≈ 1091 k€

Grand Total ≈ 1403 k€