PID summary

J. Va'vra, SLAC

Talks

• FDIRC:

- J. Va'vra: FDIRC status Towards TDR
- Massimo Benettoni: FDIRC mechanics, design and modeling
- Douglas Roberts: Barrel MC simulation status
- Christophe Beigbeder: FEE architecture update on the SNATS chip
- Vanessa Tocut & Herve Lebbolo: Front End chip

• Forward PID:

- Jihame Maalmi: Evaluation of waveform digitizing electronics "WaveCatcher"
- Leonid Burmistrov: Simulation of DIRC-like TOF detector
- Ganna Dolinska: K/ π separation with DIRC-like TOF
- Eugeniy Kravchenko: FARICH cost optimization
- J. Va'vra: Simplified tile TOF ?

Barrel FDIRC

Bottom line:

- a good progress on design, simulation, mechanics, electronics
- see a light at the end of tunnel in terms of a real practical solution
- manpower very limited

FDIRC: R&D issues to be decided for TDR

J. Va'vra

- Tweak camera optics ?
- MC simulation
- Micro-wedge ?
- Photodetector choice
- Magnetic shielding
- Electronics concept
- Photodetector holder
- Laser Calibration Concept
- Mechanical design of the new camera
- **D&D**
- Real engineering budget.
- **Background** (Riccardo Cenci: ~150kHz/6x12mm pixel with shielding & ~800kHz without shielding)
- Due to limited manpower, <u>not</u> included: scanning of MaPMTs, rate and aging studies of MaPMTs, beam tests (all tests will be in CRT), etc.

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H-8500 sensitivity to magnetic field



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DIRC tube (from NIM paper): Orientation X Orientation Y O Gauss O Gauss 2 Gauss 1 Gauss (b) TTS 0.8 ns/Gauss • X • Y • Z 4 Gauss 2 Gauss 6 Gauss 3 Gauss _2 -4 <u>-</u>20 -15 -10 -5 -5 10 15 20 Magnetic field (Gauss) ADC (c)

- **DIRC PMT tube was much more sensitive to magnetic field (~1 Gauss is a very visible effect).** \bullet
- H-8500: edge pixels are more sensitive than center pixels: • up to $\sim 20\%$ amplitude loss at ~ 20 Gauss; up to $\sim 60\%$ amplitude loss at ~ 50 Gauss
- We will need a magnetic shield, but it may not need to be as massive as in BaBar. \mathbf{O}
- We may be able to tolerate a field up to ~10 Gauss, so we may have gained a factor of ~10x. • 3/19/10 J. Va'vra, PID summary 5

Detector matrix in one camera

J. Va'vra

Detector precision is determined by a holding screw (H-8500):



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- Number of H-8500 detectors: 48 = 8 x 6 per camera
- Total number of detectors: 576 = 48 x 12 per entire system
- Total number of pixels (H-8500): 18,432 = 12 x 48 x 32 per entire system
- If we short two neighboring pads, it has to be done via equal delay path.
- Detectors must be oriented right way for shorting of pads to work properly.
- Doug Roberts: Should we stagger columns by 2-3 mm to avoid possible cracks between MaPMTs ? 3/19/10 J. Va'vra, PID summary

Mechanical design: putting it all together

Massimo Benettoni



- Rail structure enabling the RTV gluing of FBLOCK to bar box some distance away, where we have access. Once that is done, FBLOCK will be pushed into proper z-position.
- A viewer available: I can make the same pictures ~5,000 miles away

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Mechanical design: light sealing, access

Massimo Benettoni



- Light sealing must be simple to allow easy access to the electronics.
- Magnetic door may be smaller than what we have in BaBar. On the other hand, the BaBar door would work and it exists !

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FDIRC in FullSim

Doug Roberts







- Very impressive work !!

Ring image at 4 GeV/c with 3mm x 3mm pixels



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FDIRC MC simulation: chromatic corrections

Doug Roberts

Solution with the micro-wedge in:



6mm x 12mm pixels (H-8500):



- Results consistent with the FDIRC prototype beam test results.
- Could gain more than ~0.5 mrads in θ_c resolution.
- Added JV's lab measurements of the TTS resolution with the two tubes.

FDIRC TDC/ADC electronics

Christophe Beigbeder

Overall concept:



16-channel chip (takes care of one MaPMT connector):



• FDIRC electronics is split in two parts:

- one directly mounted on the PMT receiving signals and processing it with TDC/ADC
- the other one concentrates and pack all the channels to send data to the DAQ

• Issues to solve:

- chip design, mechanical packaging on the detector, cooling (water or air ?), etc.
- Max rate capability: ~2.5 MHz/pixel
- Double hit resolving time: ~ 50 ns
- SuperB version of two chips availability: first quarter 2011.
- CRT test will be done with already existing earlier version, which is available now.

FDIRC Front end electronics

Vanessa Tocut & Herve Lebbolo

PID Front End Chip



- Low walk discriminator < 70ps
- Time-to-Digital Convertor lsb 200ps 100ps resolution
- Charge measurement
- <u>Great idea: Add a waveform digitization inside the chip to be able to select a</u> <u>random channel by software !!! This is for diagnostic purposes.</u>
- 0.18µmTechno only available by the end of 2010 at MPC.
- 1st proto submitted by the end of 2011.

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Forward PID

Bottom line:

- We do not have yet a solution at hand, which would clearly satisfy a coincidence: Low cost * Robustness (N_{pe}≥10) * Background resistance
- People are working very hard to make progress on these issues.
- We should not forget that this device covers only 5-10% of solid angle.
- Manpower is very limited.

FARICH - cost saving proposal

E. Kravchenko

Original proposal: FARICH with 3 mm pixels



- **Presented cost saving proposal:** ightarrow
 - increase the pixel size from 3mm to 6mm => FARICH will have 28,800 pixels
- Preparing a prototype for the beam test. \mathbf{O}

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Performance with 6mm pixels:



WaveCatcher chip evaluation

Jihane Maalmi

WaveCatcher 2-channel board (3.3GSa/s):



Laser test setup:



WaveCatcher pulses: Scope:



Comparison of various electronics schemes:



- Evaluate the chip in the test setup used for pixilated TOF tests, mainly because we had a lot of previous measurements for comparison.
- WaveCatcher came up as a real winner.
- It will be the electronics used in many experiments in future.
- Could be used for either TOF or cluster counting applications.
 - Writing a NIM paper on overall comparison.

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DIRC-like TOF Geant4 study: geometry

Leonid Burmistrov



- Magnetic field: 1.5 Tesla.
- Hamamatsu MCP-PMT SL-10 pixel size: 22mm x 5.5mm
- 12 quartz sectors, 9 MCP-PMTs/sector => <u>36 pixels per sector</u>
- Quartz tile thickness in the simulation so far: 1.2 cm
- Quartz tilt angle: ~5° => need ~5cm extra space
- Not yet in the simulation: realistic background.
- <u>Variables to tune to increase Npe</u>: (a) tilt angle, (b) tile thickness (1.2cm -> 2.4cm ?),
 (c) photon absorber around the tile edges, (d) QE tuning (bialkali vs. GaAsP vs. multi-alkali photocathode), put detectors on both inside & outside diameter, etc.

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DIRC-like TOF MC study: Npe



• In some section of the phase space one deals with 3 photoelectrons only - that is clearly too low. The only variables one has to tweak: the radiator thickness, its tilt, or add more detectors at outer radius.

• Comment on the SL-10 MCP-PMT efficiency:

- 1. QE for multi-alkali photocathode at 350nm: ~20%
- 2. Geometrical collection efficiency of the 1-st MCP for in-time photoelectrons: 70%
- 3. Dead space between boundaries: 65%
- => Therefore the total fraction of in-time photons detected (a product of all above numbers): PDE ~9%.

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- Put photon detectors on both inner and outer side of quartz plate ightarrow
- This will increase the cost but one may get into a regime of Npe >10. 0
- Leonid is now studying this option. 0
- Other similar options investigated. We think Npe problem can be fixed. 0 3/19/10 J. Va'vra, PID summary 18



• Important point: background not yet included.

What should be a criteria for minimum requirements on acceptable performance ?

PID group discussion during the session

- A design with Npe ~ 3 is not good enough.
- A minimum of Npe ≥ 10 should be considered a "robust performance" (in principle Npe ~ 5 might be good enough, but if the aging effects cause a slow degradation, one may end up with Npe ~ 3).
- Background must be understood much more than presently. It might be difficult to understand neutrons at the end, but we should make sure that Bhabhas alone will not kill the detector's performance).
- Detector rate and aging effects must be understood.
- Cost should scale with the solid angle fraction.
- Not everything can be simulated. One needs measurements as well.
- Most of these issues will be addressed by the time of Elba meeting.

A simple pixilated TOF ?

J. Va'vra



- <u>Logic of this counter</u>: (a) must be cheap, (b) fill up the dE/dx hole near 1 GeV/c for K/ π separation, and (c) σ ~100-150ps resolution .
- Initial tests with LYSO crystal started. Likely to switch to a fast scintillator.
- Looking into some clever way to read out the scintillator tile with limited number of G-APDs.
- 1 pixel = 1 LYSO crystal footprint
- Electronics: could we use FDIRC TDC/ADC chip serving 16 LYSO crystal footprints ?
- Pulse height to be added to the EMC calorimeter pulse height.

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We were encouraged to make a decision within 6 months.