

XII SuperB General Meeting - LAPP - Annecy



Striplets, RO chips, DAQ:

Updates on Trieste activities

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Outline



- What are we involed in
 - Striplets & Strip detectors
 - FSSR2 chip
- Noise measurements
 - New effect observed in FSSR2; understood
 - Update on noise @ 2008 test-beam & comparison with benchmark
 - (mini) temperature scan
 - New setup
- Noise characterization: To do list
- Update on new DAQ chain
- Conclusion



Slim5



R&D Italian collaboration



- Mission: "Pushing thin tracking-devices state-of-the-art for High Energy Physics"
- Highlights:
 - MAPS → not in this talk!
 - Striplets
 - Double sided telescope
 - Data-driven DAQ-architecture
 - Test beam in 2008 @ CERN PS
- Paper ready for submission

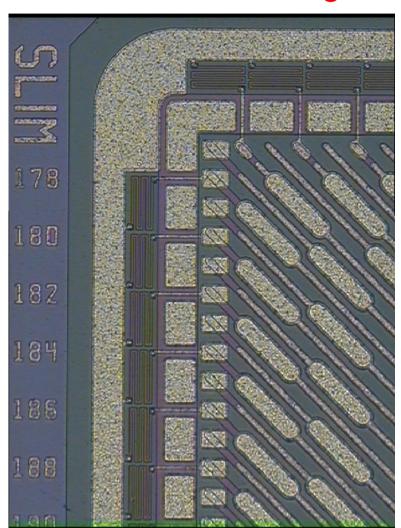


Slim5 – Striplets sensors



Designed sensor for L0 & inner layers



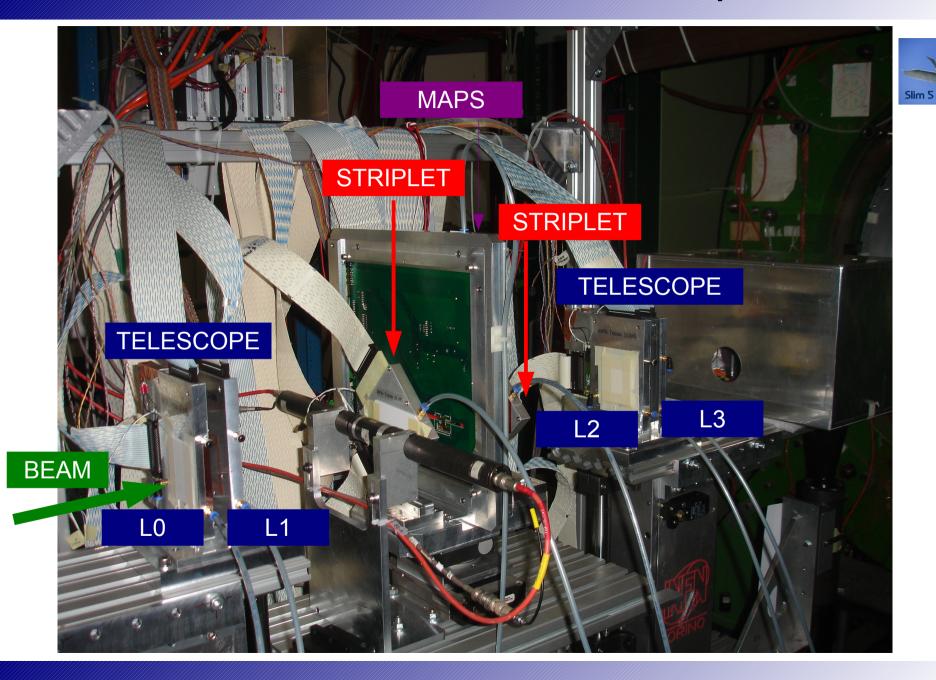


- 200 μm-thick double-sided strip detector
 - ± 45° oriented strips
- the design allows a long double-sided detector with short strips on both sides
- Active area = 27 x 12.9 mm²
- 50 μm pitch on p-side
- 50 μm pitch on n-side
- Strip capacitance ~ 4 pF
- Designed & fabricated at FBK-IRST



Slim5 – Test beam setup



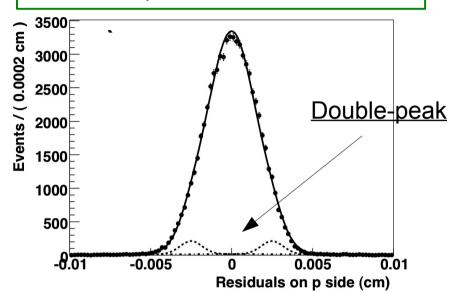




Slim5 – Results from Test beam



Spatial resolution

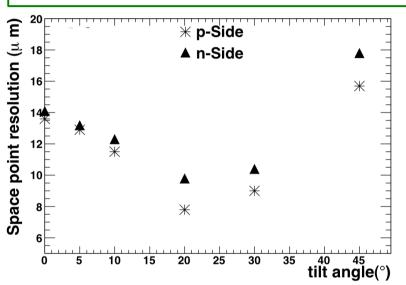


- <u>Double-peak effect in resolution plot</u>
- It helped in improving resolution of almost 10%

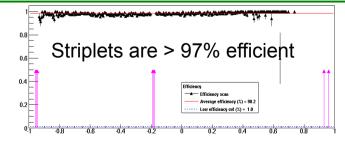
- p-Side: Space Point resolution: 13.6 μm
- n-Side: Space Point resolution: 14.1 μm
 - Pitch = 50 μ m on both sides







Efficiency along the detector



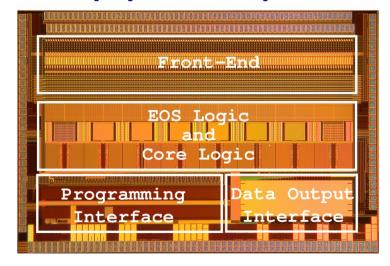


FSSR2 RO chip



- Fermilab Silicon Strip Readout chip v2
 - The chip has been developed by an INFN Pavia & Bergamo and Fermilab for the BTeV strip detectors
- 128 analog channels, with address and time information for all hits
- Self-triggered readout architecture, with digital output only
- Read out up to 70 MHz
 - Operated at 20 MHz @ testbeam

Input pads with 50 um pitch





FSSR2- cont'd



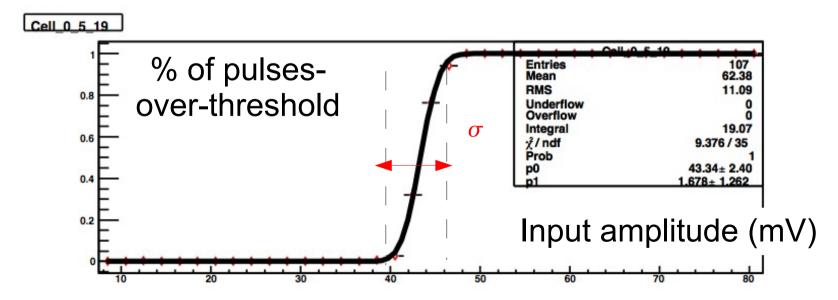
- 8 programmable thresholds, with the 0th one acting as hit/no hit discriminator
 - Each channel has its own set of 8 comparators
- 3-bit ADC information is provided for each hit
- Programmable gain and peaking time
- Baseline restorer available
- Optimized for positive signals
 - Limited dynamic range for n-side: just hit/no hit information for negative signals



FSSR2 calibration



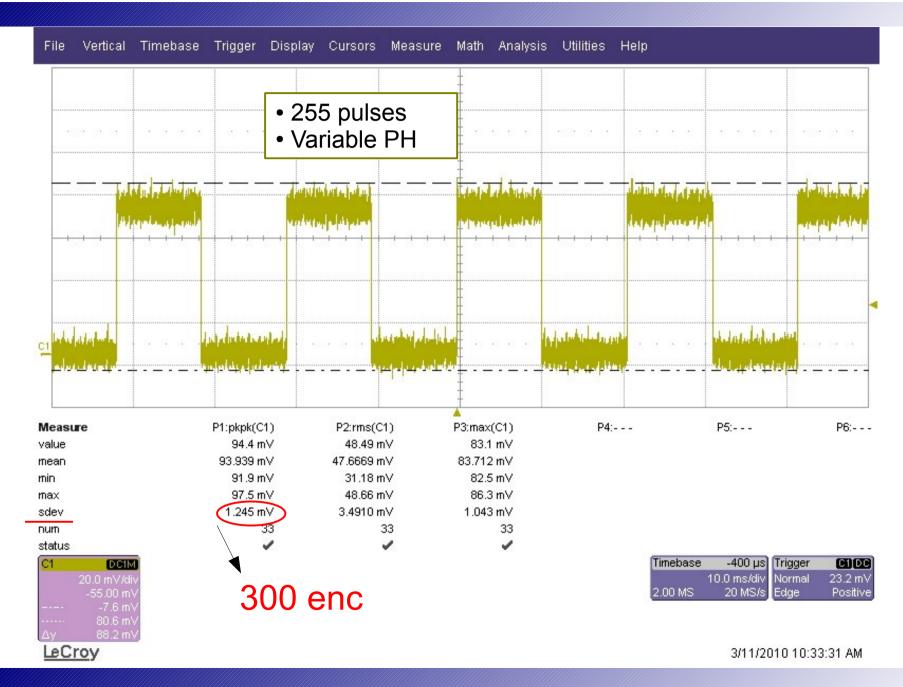
- Noise was estimated using FSSR2 internal-calibrator, during beam test
- At fixed threshold, input amplitude was increased, and fraction of pulses-over-threshold recorded
- The result is fitted with an erf function, where σ is the estimated noise





NEW: Internal pulser oscillations





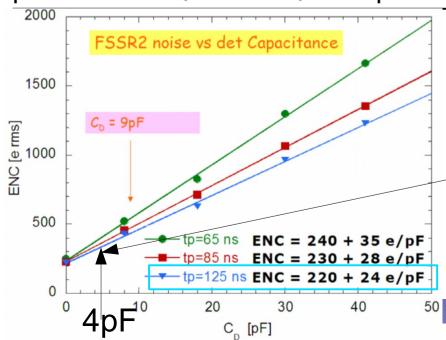


Noise measured @ 2008 test-beam



- The pulser-induced noise has to be subtracted
- So we re-interpreted the results obtained:

Detector	Striplets		Telescope	
Polarity	p side	n side	p side	n side
Noise (e ⁻ RMS)	560	978	400	742
S/N	29	16	60	32
Gain (mV/fC)	96	67	97	67



About 316 enc*

At test-beam we were very close to benchmark for telescope detector on p-Side

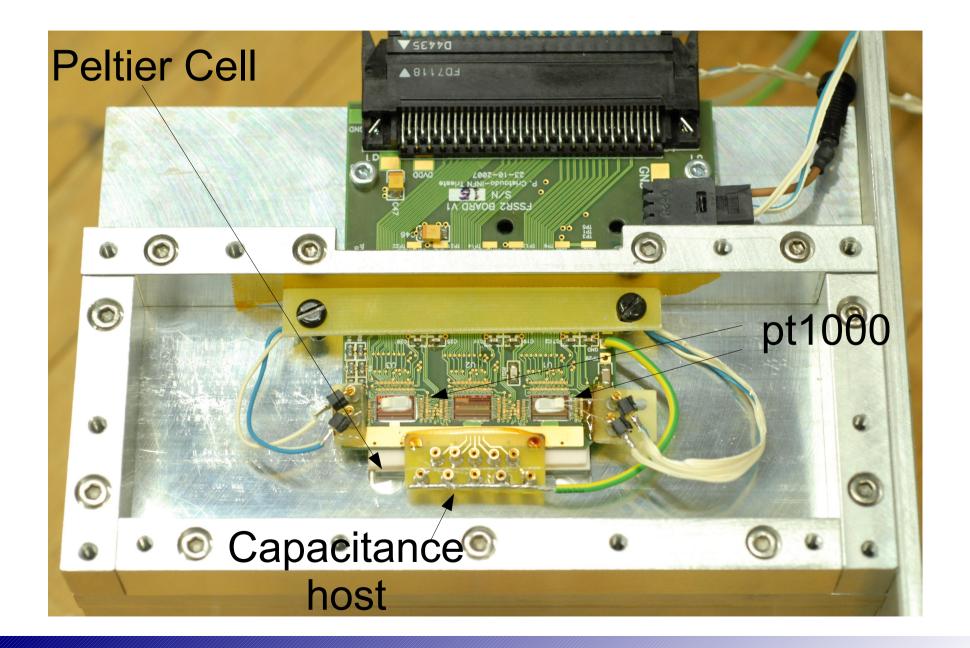
*= expected for p-Side of telescope

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New setup in Trieste lab





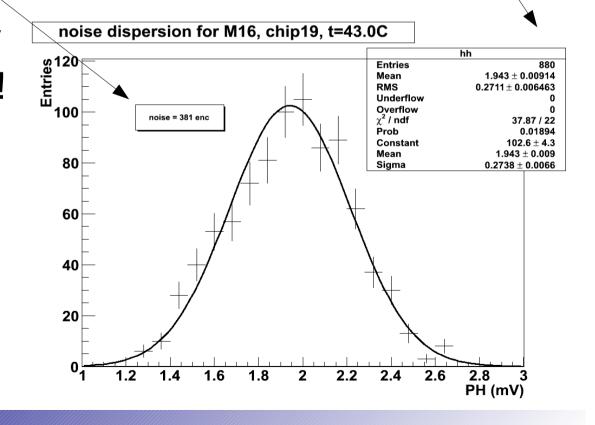


New noise measurements in Trieste



- (mini) temperature scan
- 33° C → 360 enc
- 43° C → 381 enc
- 44.4° C → 385 enc
 - Positive signals only
- ... more data to come!!!

- Calibration performed with FSSR2 internal pulser and old BTeV test-beam DAQ chain
- 8 (thresholds) x 128 (channels) injected
 - Not all fits do converge
 - Some extra-counts enter the fit

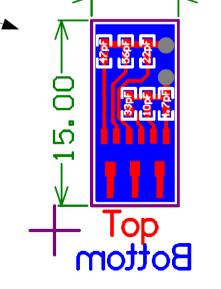




To Do list



- More temperature points
- Change shaper parameters
- Measure striplets-module capacitance
 - Sensor + fanout + ecc
- Bond FSSR2 channels to capacitors to measure noise as a function of capacitance
- A new DAQ... (see next slide)





New DAQ



- All we have shown so far was realized using the BTeV test-beam DAQ "Pomone"
- It's a one-piece-in-the-world, which comes with no warranty and no spares
 - But we received invaluable help from former BTeV Milan group
- So we are developing a new DAQ, which is based on a CAEN board which has FPGAs
- We will program chips and read data through a VME-USB bridge and a Labview-based acquisition program
- Status: FPGA is programmed (many thanks to Mauro Villa); ready to start some tests



Conclusions



- There is a lot of activity about striplets and the FSSR2 RO-chip in Trieste
- Oscillation of FSSR2 internal pulser has been identified as a non-negligible source of noise
- We started a study of noise versus
 - Temperature
 - Load capacitance
 - Shaper parameters
- New DAQ for strips + FSSR2 is under development



That's it





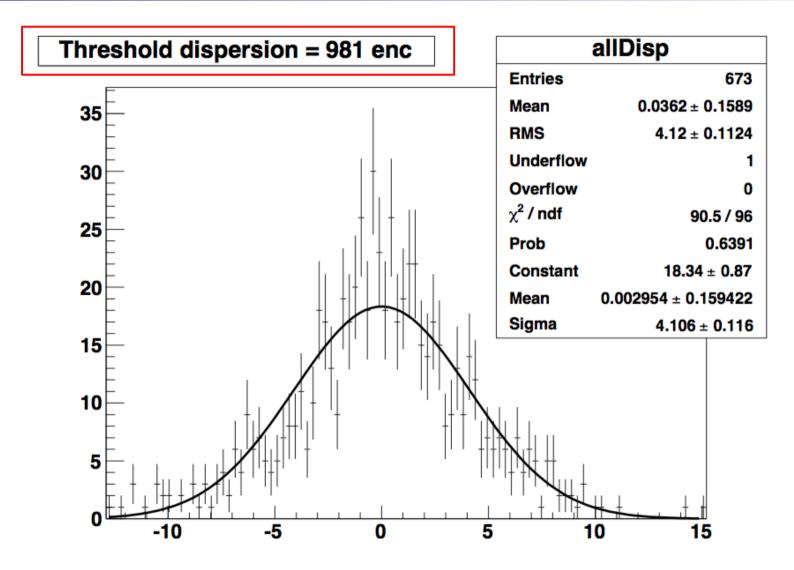
Backup slides





Threshold dispersion





We strongly suspect its a POMONE related feature