DNW MAPS and pixel front-end in vertical integration technology for the SuperB SVT

L. Ratti

Università degli Studi di Pavia and INFN Pavia

XII SuperB General Meeting

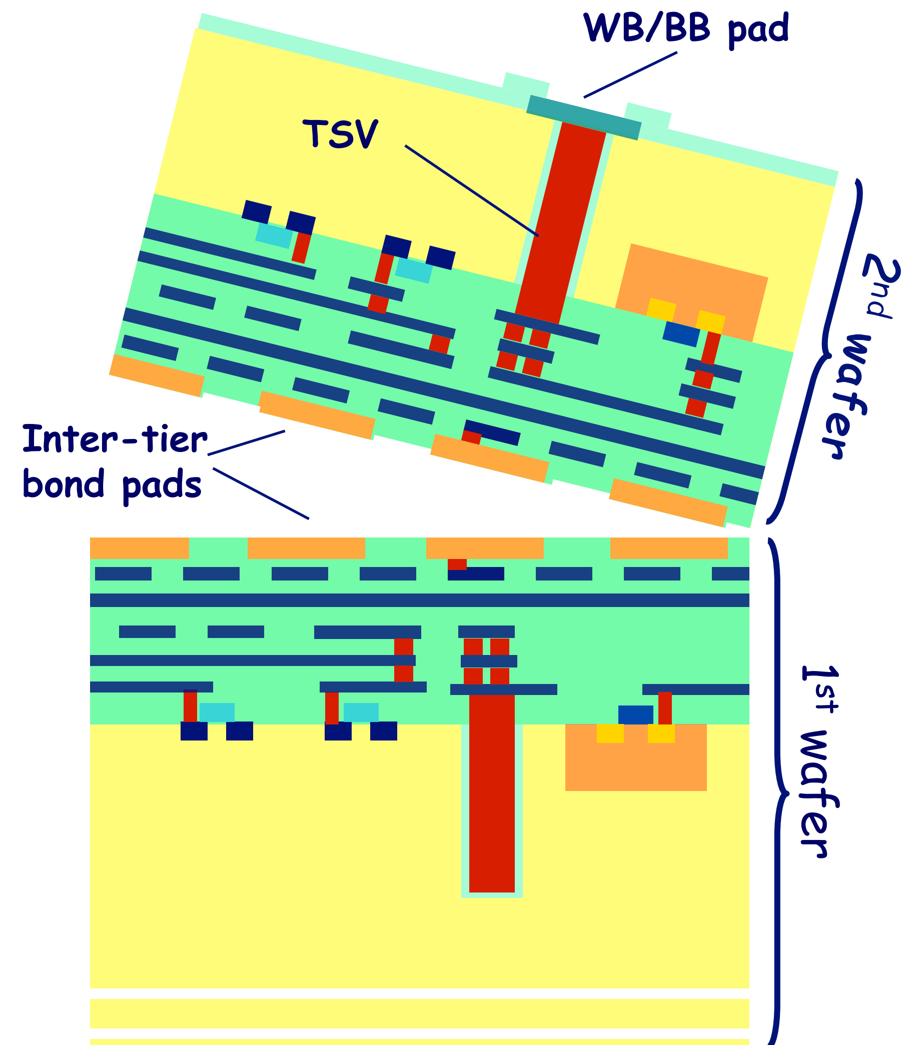
March 16-19 2010
Annecy, France

3D technology options for the SuperB SVT

- **Design of the SVT layer0 at SuperB has to comply with severe requirements**
  - large background, >5 MHz/cm^2, small thickness, <0.5% X_0
- **Two options made available by vertical integration technologies (3D) are being pursued**
- **Hybrid pixel detectors**
  - vertically integrated, mixed-signal circuit to read out a standard pixel detector in high resistivity silicon (size of the chip to be submitted is 32x128)
  - fine pitch (50 μm) bump bonding (IZM, Munich), other technologies (direct bonding by Ziptronix) might be investigated in the future
- **Deep N-well CMOS monolithic sensors (DNW-MAPS)**
  - innovative approach (deep N-well sensor) proposed to enable fast readout through pixel-level sparsification and time stamping (a 16 kpixel chip is being considered for the next submission)
  - based on extensive R&D in planar 130 nm CMOS technology
  - DNW sensor in an undepleted substrate, analog front-end for capacitive detectors, analog and digital blocks integrated in separate layers

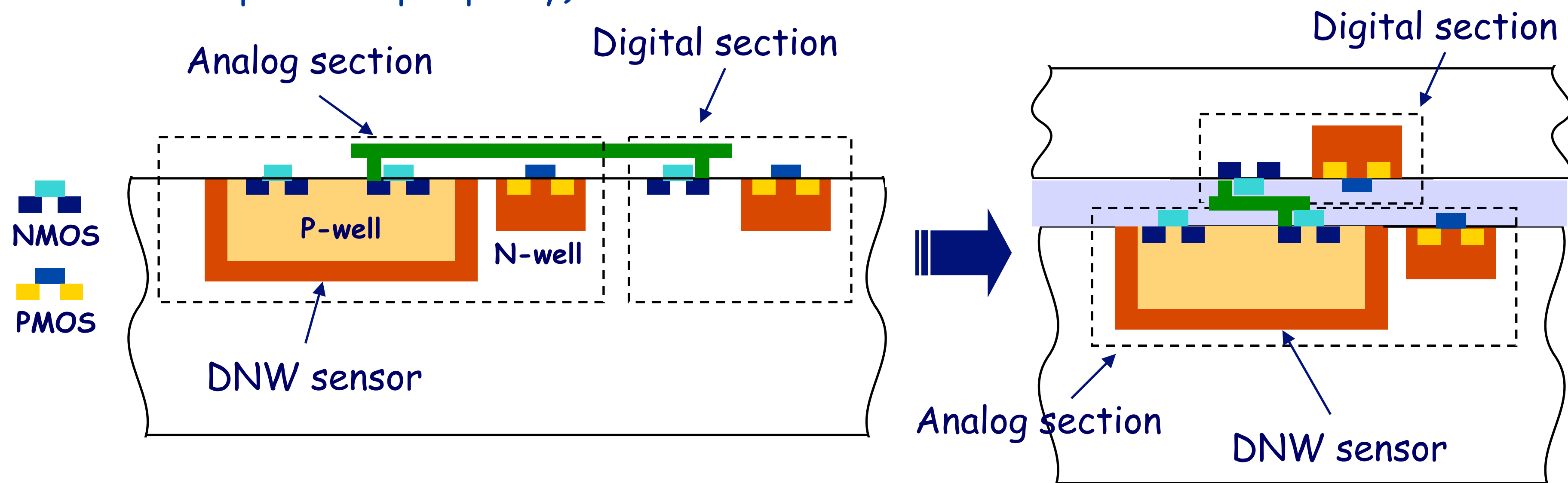
Vertical integration (3D) technologies

- In wafer-level, three-dimensional processes, multiple strata of planar devices are stacked and interconnected using through silicon vias (TSV)
- 3D processes rely upon the following enabling technologies
  - Fabrication of electrically isolated connections through the silicon substrate (TSV formation)
  - Substrate thinning (below 50 μm)
  - Inter-layer alignment and mechanical/ electrical bonding
- Tezzaron Semiconductor technology (via first approach) can be used to vertically integrate two layers specifically processed by Chartered Semiconductor (130 nm CMOS, 1 poly, 6 metal layers, 2 top metals, dual gate option, N- and PMOS available with different V_{th})



From 2D to 3D MAPS

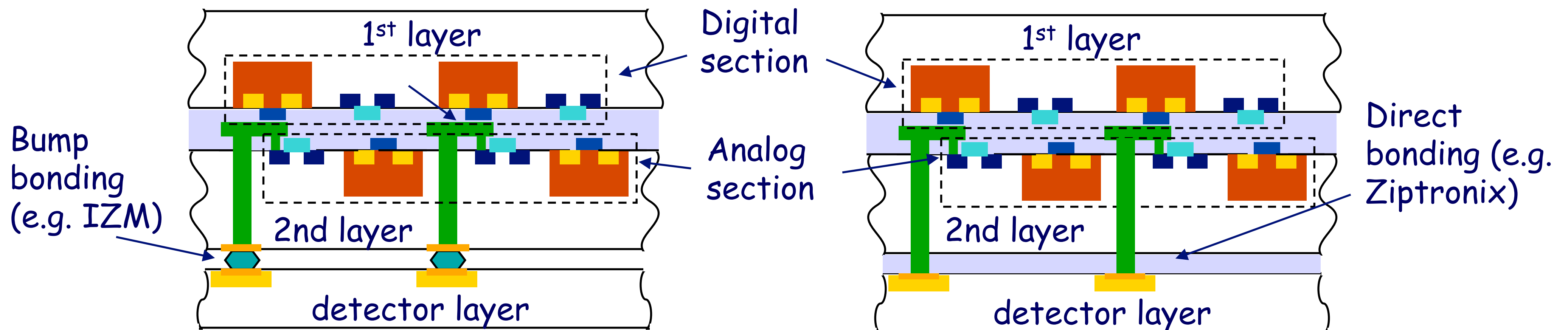
- Analog and digital blocks integrated in separate layers to minimize cross-talk between digital blocks and sensor/analog circuits
  - less PMOS in the sensor layer → improved collection efficiency
  - more room for both analog and digital power and signal routing (in planar CMOS MAPS scaling to suitably large matrices is forbidden by the need for point-to-point lines from macropixels to periphery)



- Tier 1: collecting electrode and analog front-end and part of the discriminator
- Tier 2: part of the discriminator, digital front-end and peripheral digital readout electronics

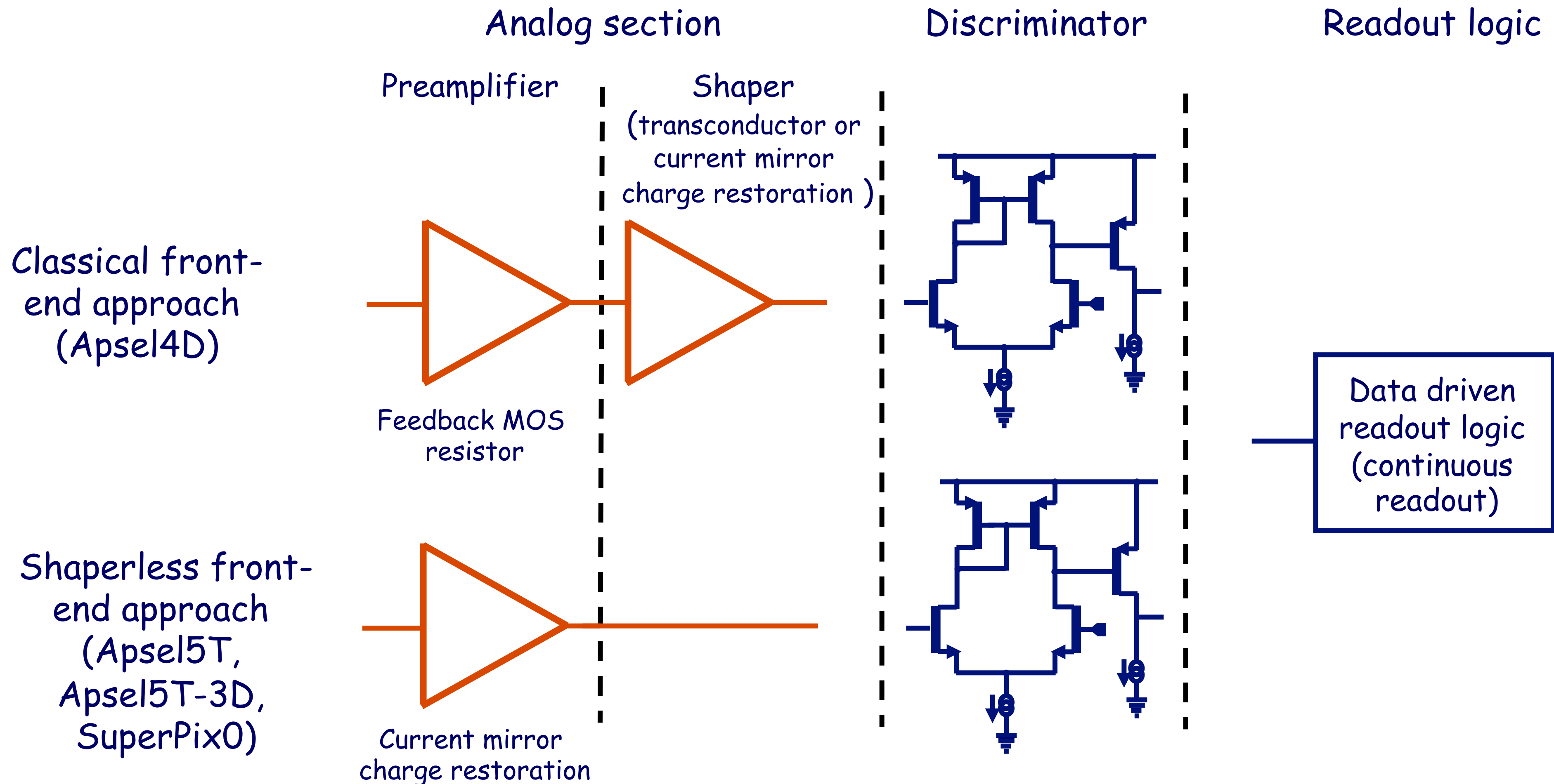
3D hybrid pixels

- Development of a 3D front-end chip to be vertically integrated with fully depleted detectors through some more (bump bonding) or less (direct bonding) standard technique



- Larger signal available from the detector
- More advantageous trade-off between S/N and dissipated power

Front-end design approach



XII SuperB Project Workshop
LAPP - France
from March 16th to 19th 2010

Comparison

Classical front-end

- Larger power dissipation
- Larger area (also MIM capacitors may be required)*

- Can reliably achieve large charge sensitivity**
- Noise and threshold dispersion can be optimized independently

Shaperless front-end

- Smaller power dissipation
- Smaller area (MIM capacitors not required)

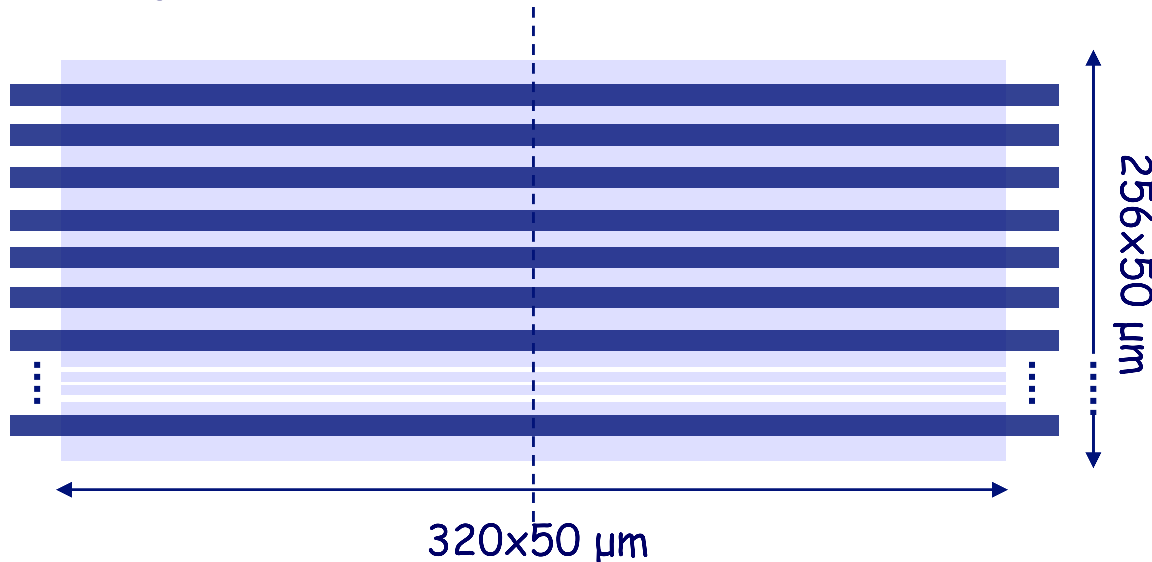
- Not suitable for large charge sensitivity**
- Depending on the feedback network , noise optimization may affect threshold dispersion minimization

*Might be less of a problem in 3D processes

**Large charge sensitivity= 600/800 mV/fC

Bias voltage drop

- May be an issue with large matrices of relatively current-hungry detectors (e.g. DNW MAPS)



- Power distribution with a single thick metal layer (M5 in Chartered CMOS tech)

•AVDD width=AGND width=24 µm

•Max density=80%→ eq. width≈19 µm

•I_{cell}=30 µA

•M5 sheet resistance=25/35 mΩ/□ (typ/max)
→R_{cell}≈65/90 mΩ (typ/max)

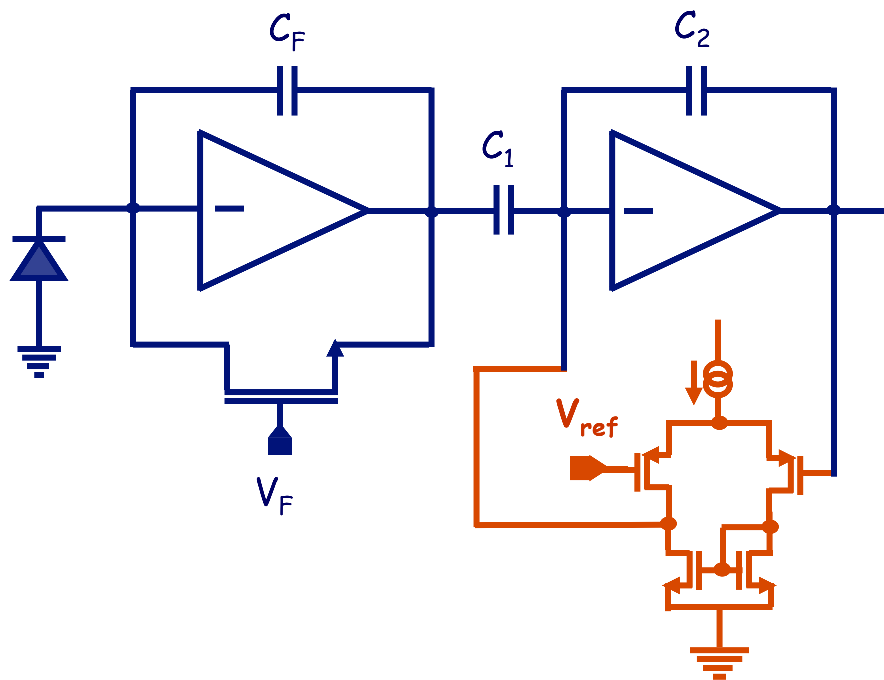
ΔV_{max}=25/35 mV (typ/max)

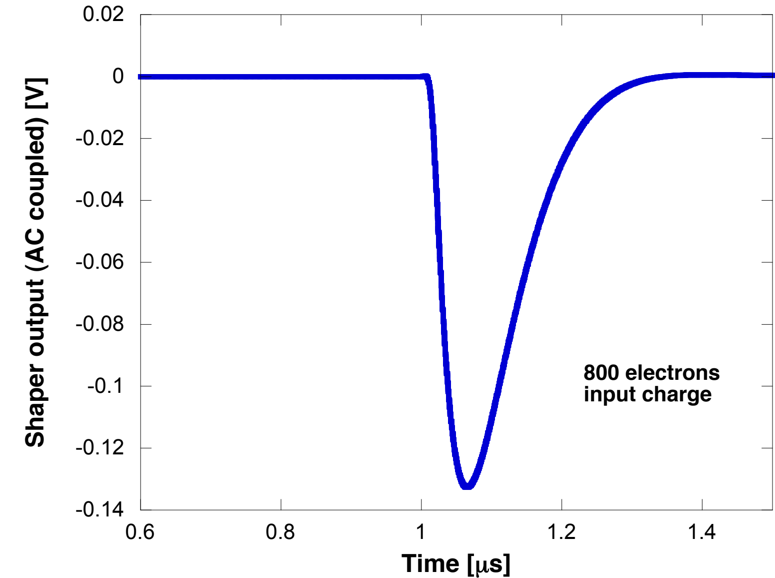
- Availability of other metal layers (M4, M6) can make things better (but not much better)
- Total current ~2.5 A → at least 80 AVDD PADS and 80 AGND PADS required to have ~30 mA/pad or less
- 1.8 W/cm² @ AVDD=1.5 V

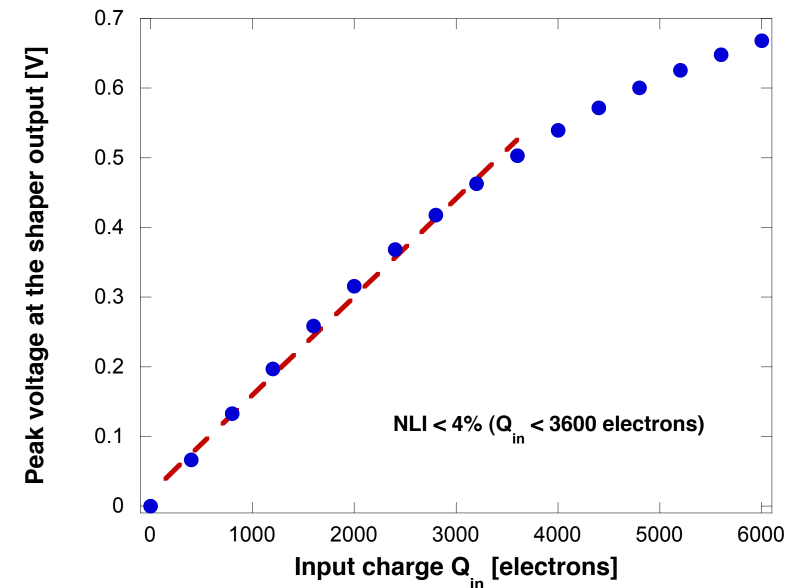
Front-end for 3D MAPS

Main design features and simulation results

- W/L=28/0.25
- I_D=26 µA, power dissipation=40 µW
- C_D=300 fF
- 70 ns peaking time
- Charge sensitivity (G_Q): 950 mV/fC
- Equivalent noise charge (ENC): 60 electrons





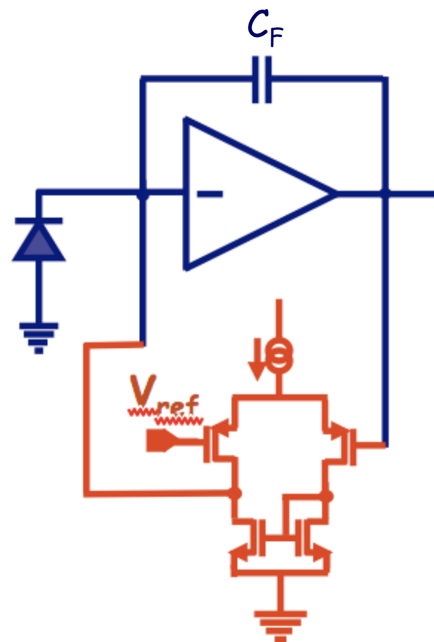


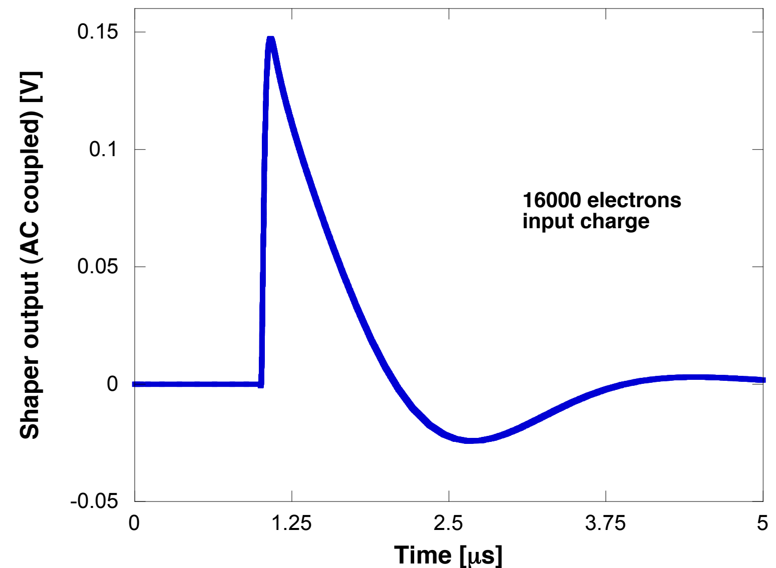
L. Ratti, "DNW MAPS and pixel front-end in vertical integration technology", SuperB General Meeting XII

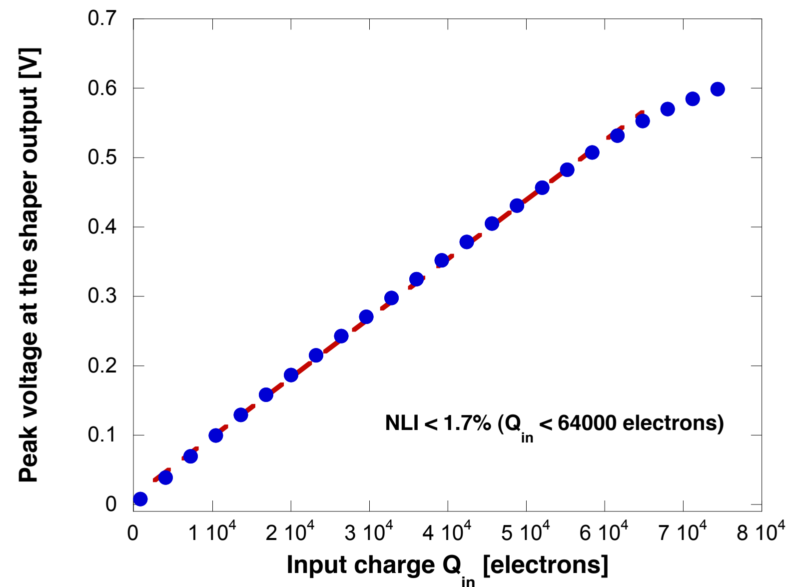
Front-end for hybrid pixels

Main design features and simulation results

- W/L=30/0.35
- I_D=4.4 μA, power dissipation=6.6 μW
- C_D=150 fF
- 80 ns peaking time
- Charge sensitivity (G_Q): 55 mV/fC
- Equivalent noise charge (ENC): 170 electrons





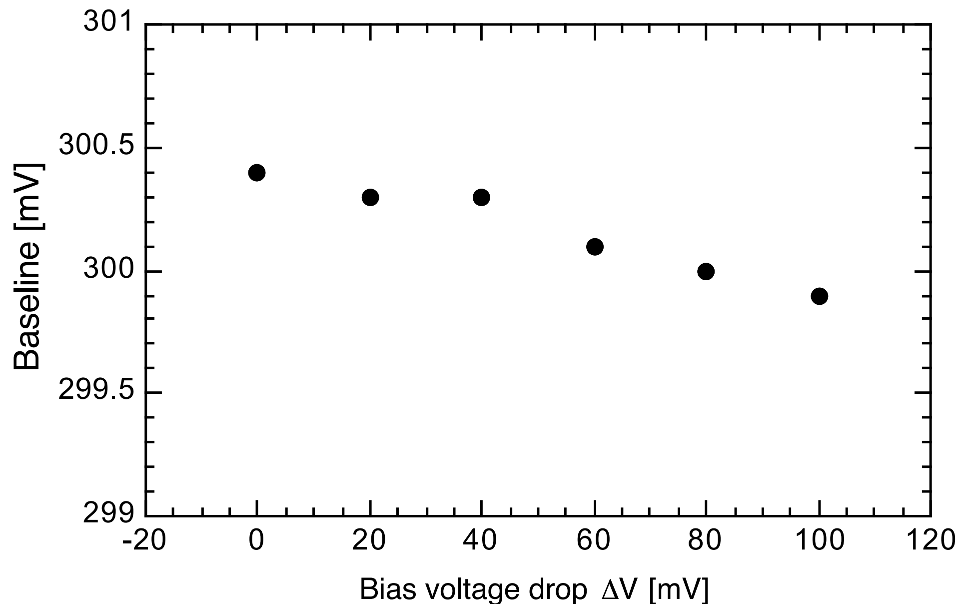


Baseline change due to bias voltage drop

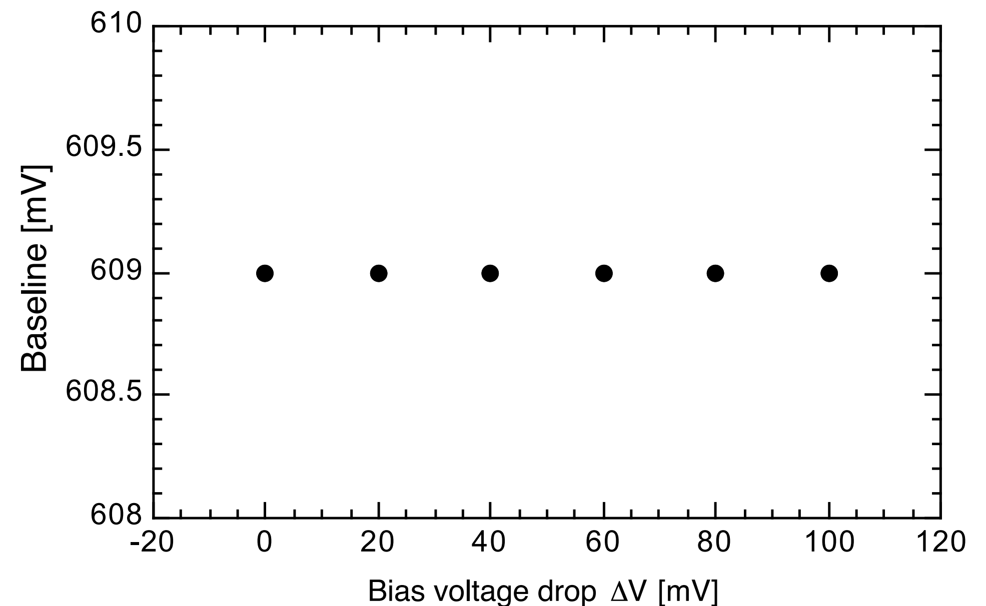
- Circuit simulations were performed at varying values of the bias voltage drop ΔV to study its effect on the baseline level, the charge sensitivity and the equivalent noise charge

AVDD=1.2 V-ΔV, AGND=ΔV

Front-end for hybrid pixels



Front-end for MAPS

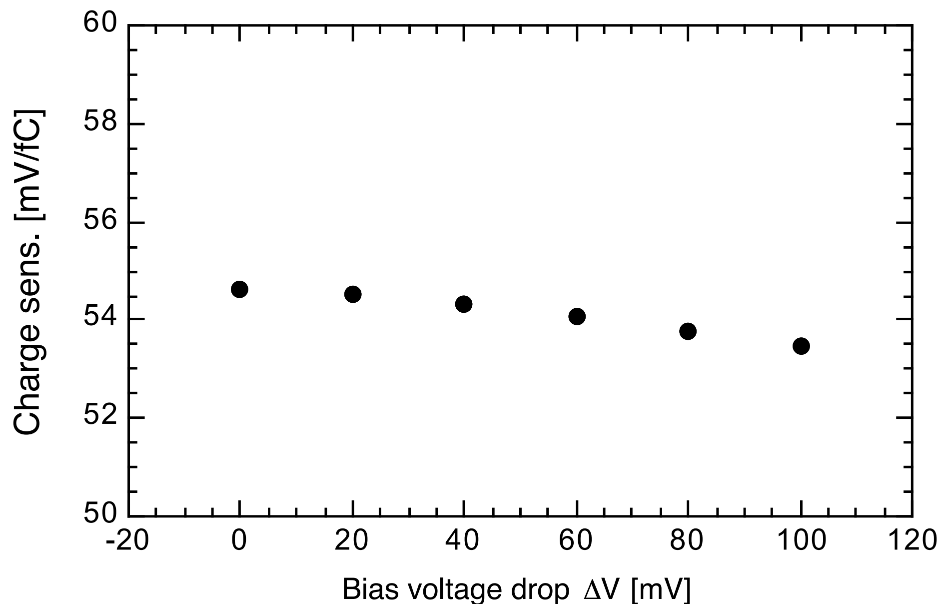


Charge sensitivity change due to bias voltage drop

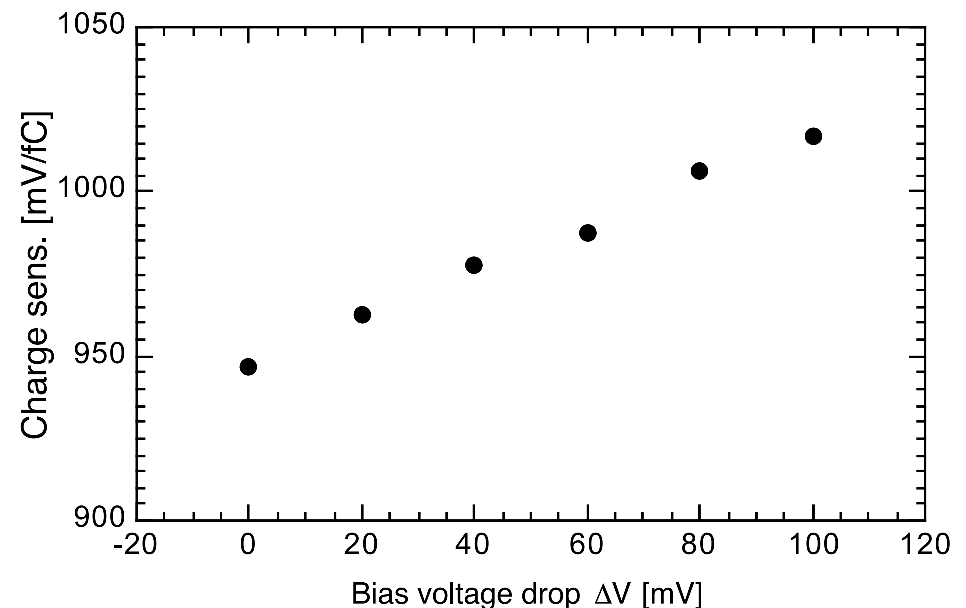
- Circuit simulations were performed at varying values of the bias voltage drop ΔV to study its effect on the baseline level, charge sensitivity and equivalent noise charge

AVDD=1.2 V-ΔV, AGND=ΔV

Front-end for hybrid pixels



Front-end for MAPS

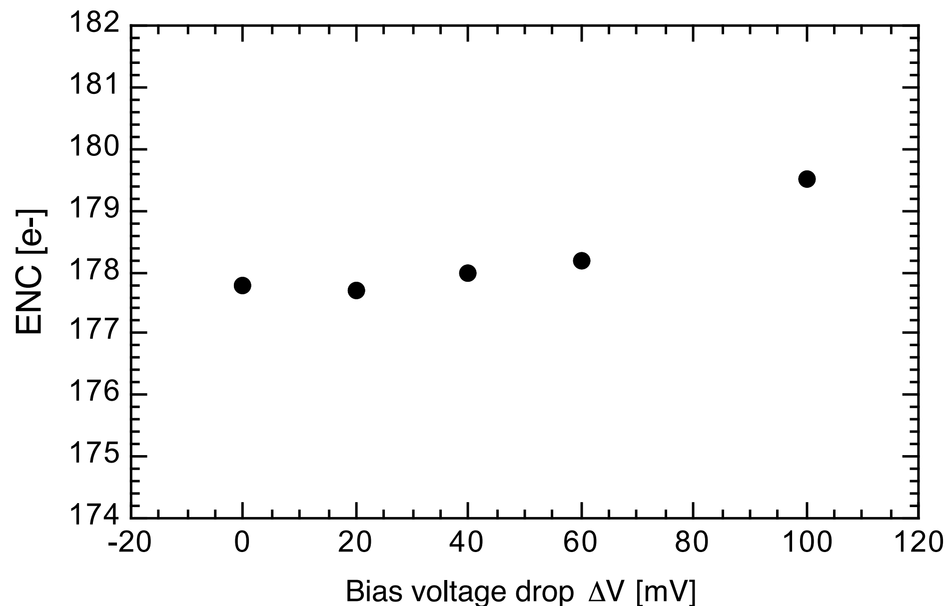


ENC change due to bias voltage drop

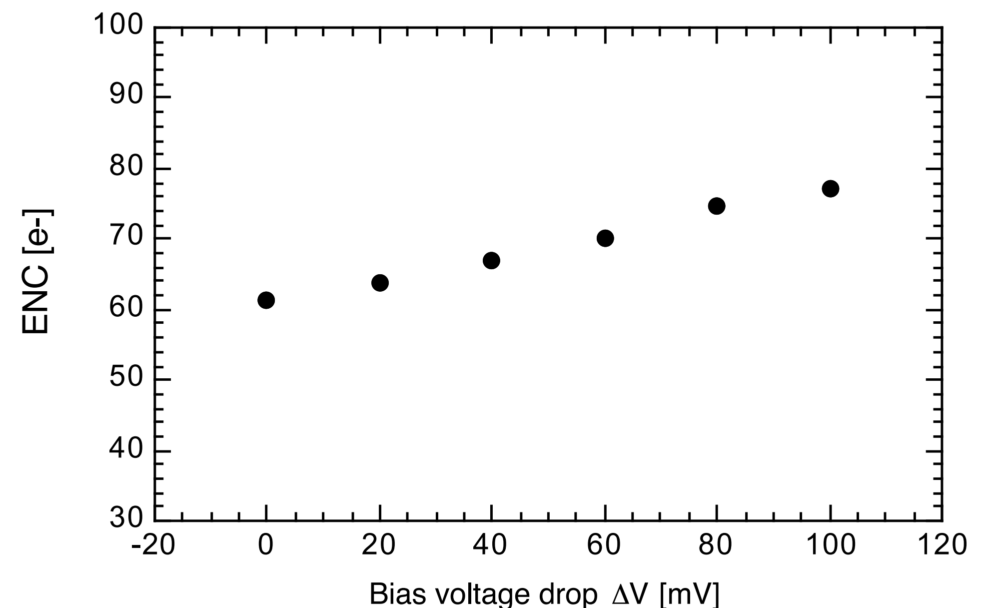
- Circuit simulations were performed at varying values of the bias voltage drop ΔV to study its effect on the baseline level, the charge sensitivity and the equivalent noise charge

AVDD=1.2 V-ΔV, AGND=ΔV

Front-end for hybrid pixels



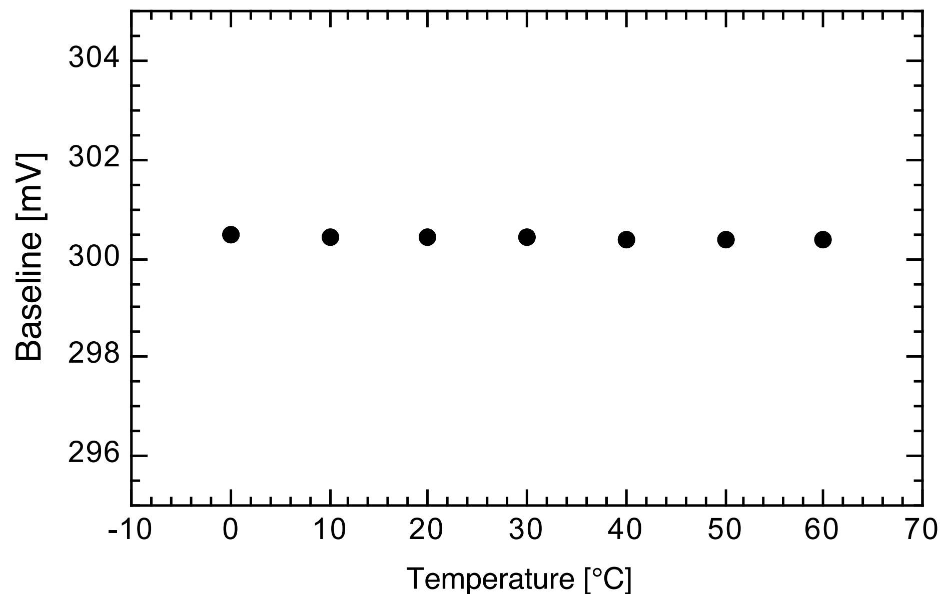
Front-end for MAPS



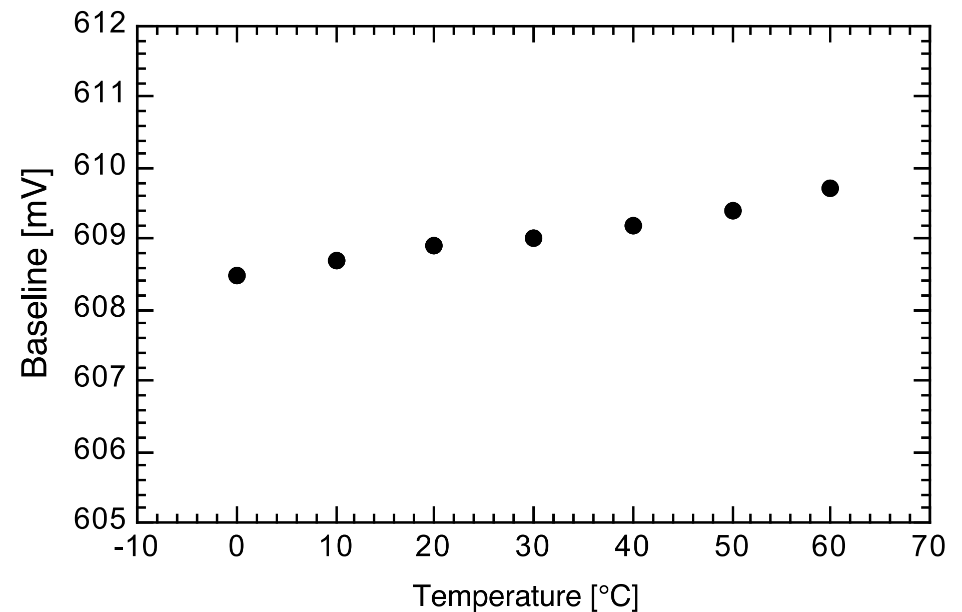
Baseline change due to temperature variation

- Circuit simulations were also performed at varying temperature to study its effect again on the baseline level, the charge sensitivity and the equivalent noise charge

Front-end for hybrid pixels



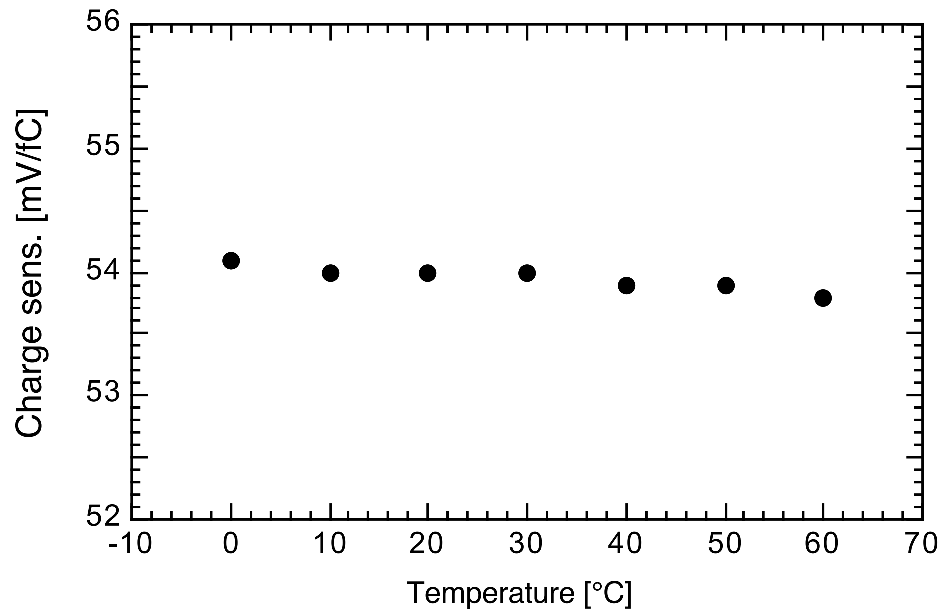
Front-end for MAPS



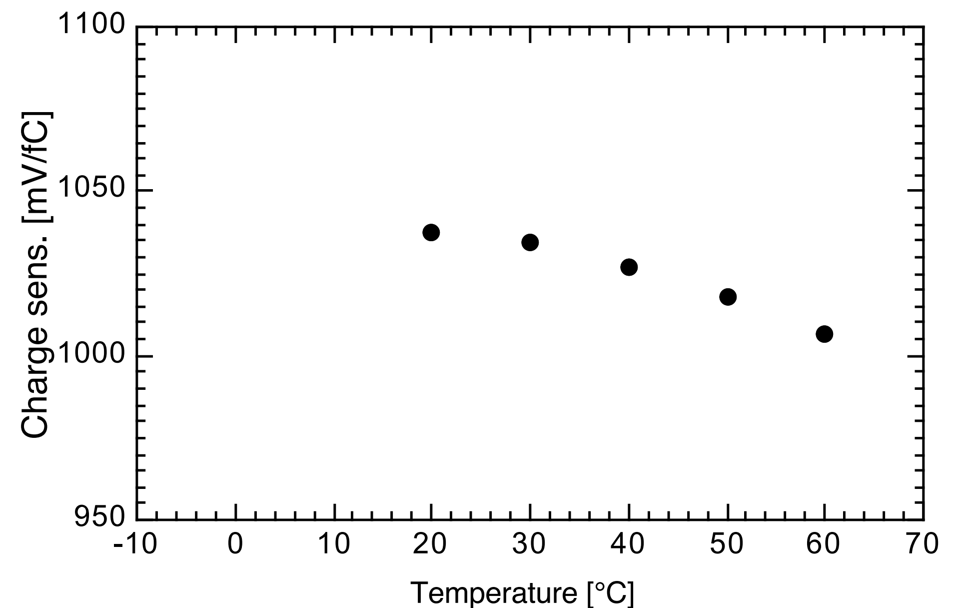
Charge sensitivity change due to temperature variation

- Circuit simulations were also performed at varying temperature to study its effect again on the baseline level, the charge sensitivity and the equivalent noise charge

Front-end for hybrid pixels



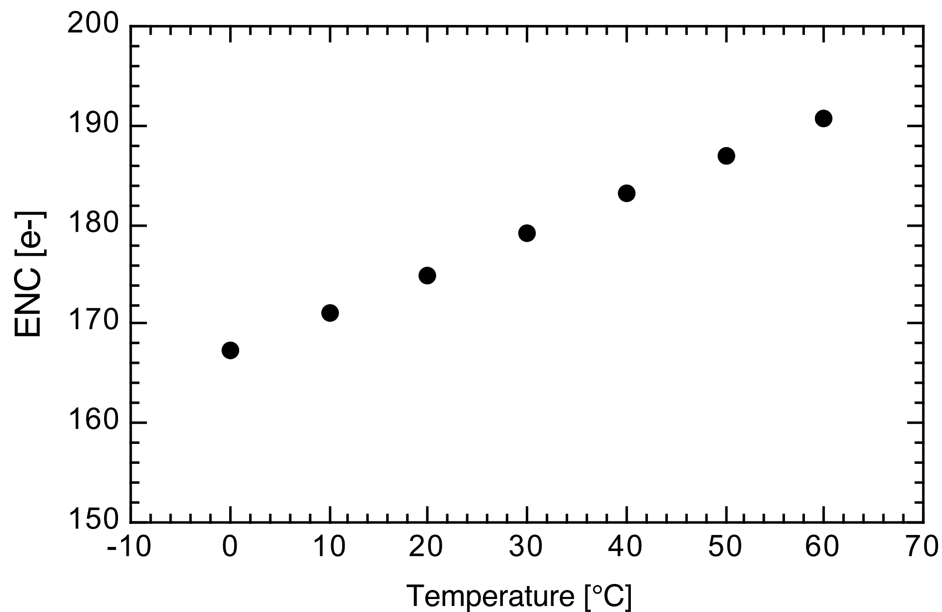
Front-end for MAPS



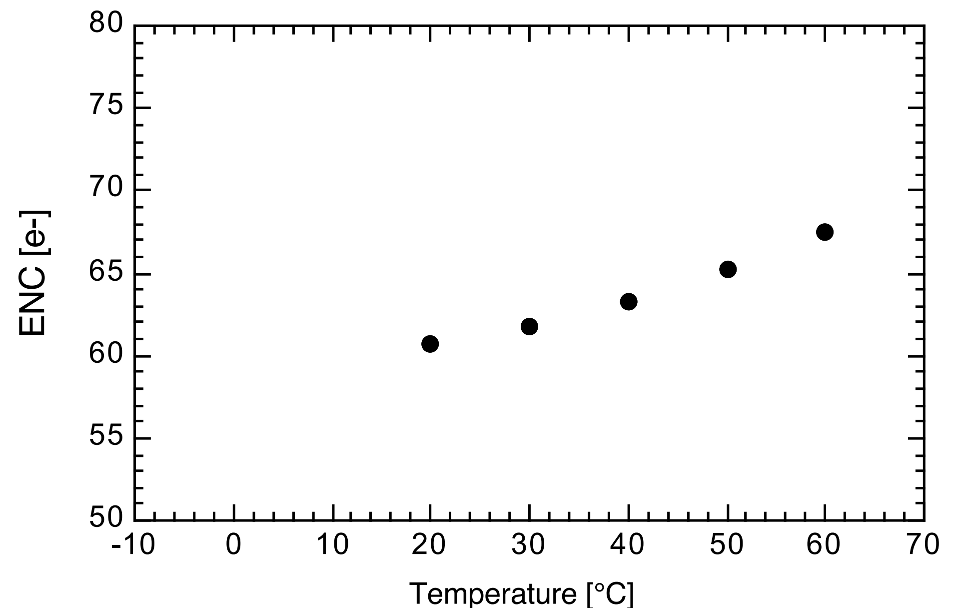
ENC change due to temperature variation

- Circuit simulations were also performed at varying temperature to study its effect again on the baseline level, the charge sensitivity and the equivalent noise charge

Front-end for hybrid pixels



Front-end for MAPS



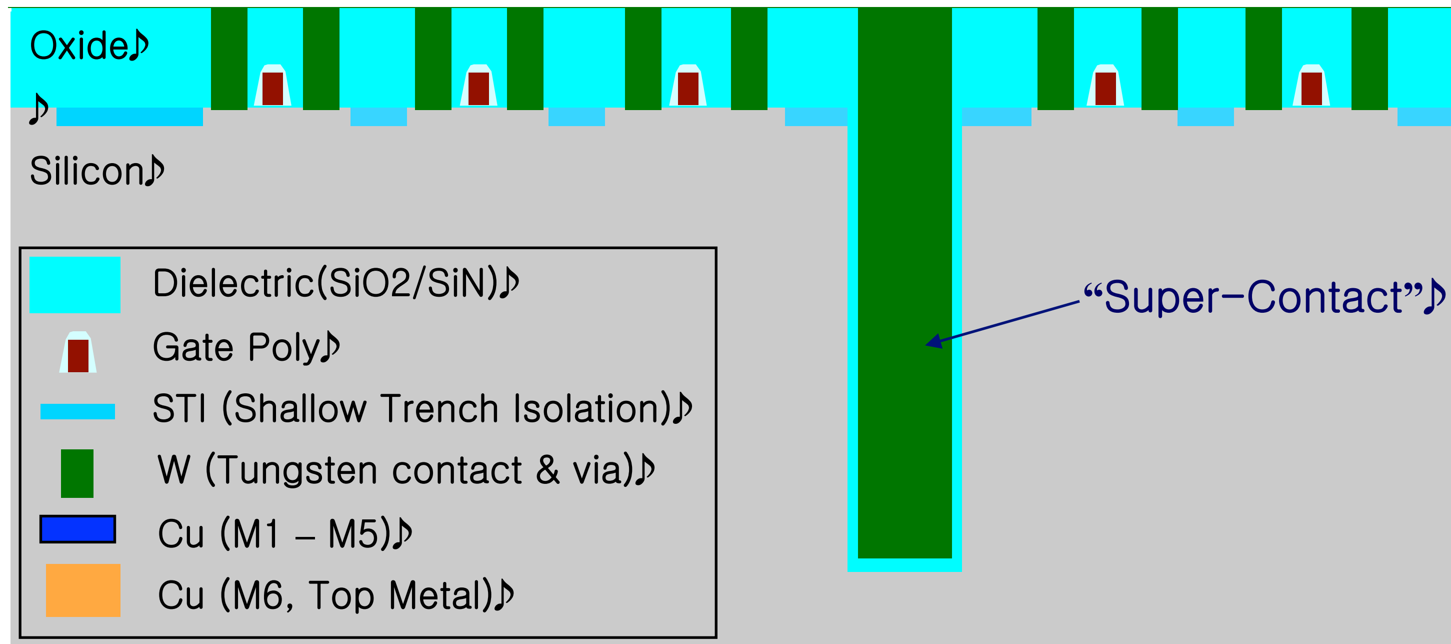
Conclusion and future plans

- Two different 3D solutions are being investigated for the SVT layer0 at SuperB through extensive R&D programs, namely hybrid pixel detectors (shaperless front-end approach) and DNW MAPS (classical front-end approach), both in 130 nm CMOS technology
- Both MAPS and hybrid pixels can gain significant benefits from going 3D
  - increase in charge collection efficiency
  - immunity from (or reduction of) cross-talk phenomena between digital blocks and sensor/analog circuits
  - scalability to large sensor matrices
  - better trade-off between point resolution and functional density
- Use of a transconductor in the feedback network can make the analog processor more robust against possible bias voltage drop in large sensor matrices and temperature changes
- In-pixel DAC for threshold tuning, blocks for gain calibration and pixel masking under development
- After solving a few problems, which have been preventing the run from starting for several months, the first 3D MAPS structures (from the 2009 submission) may be available at the end of May/beginning of June

Backup slides

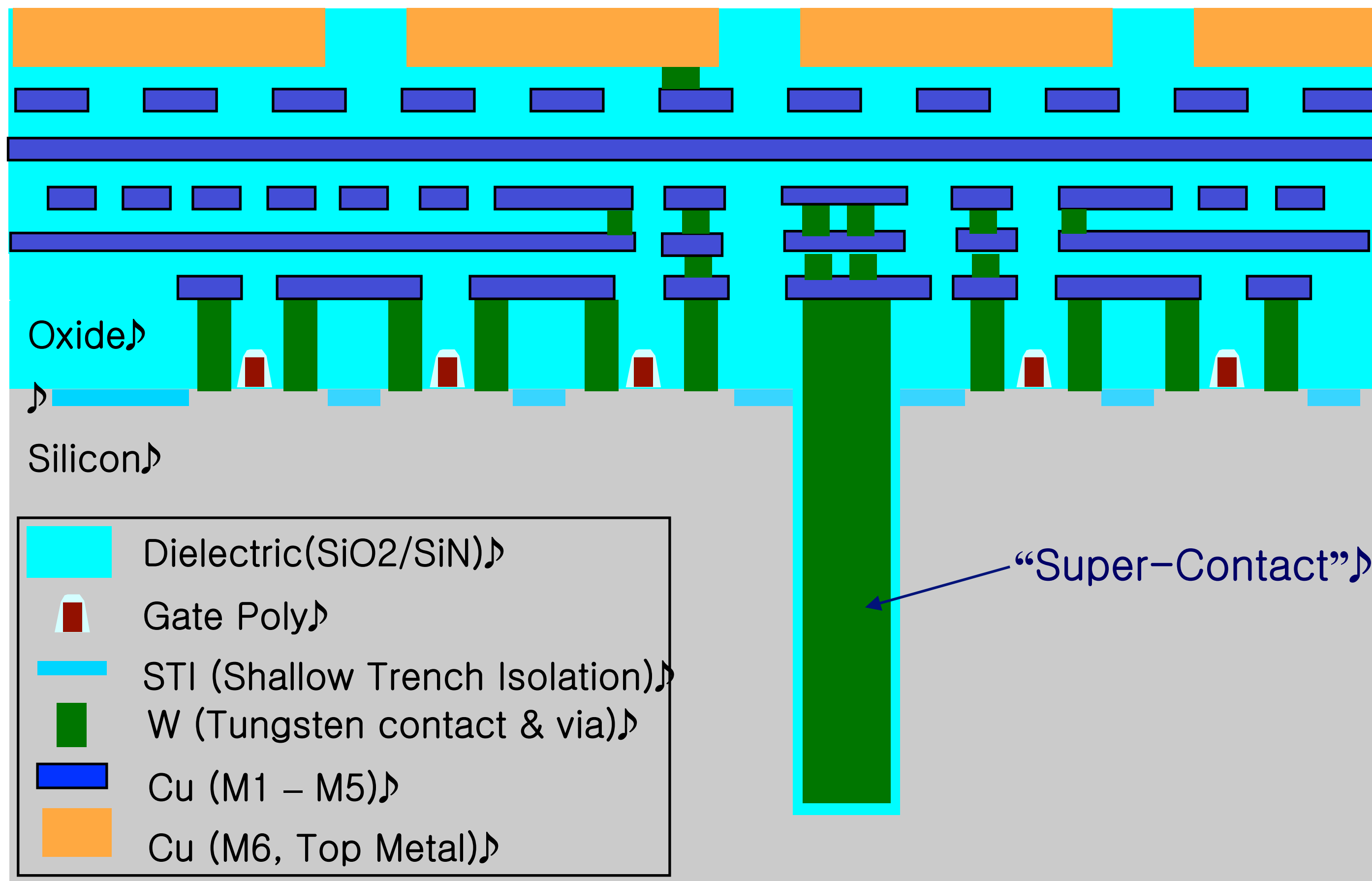
Tezzaron vertical integration process

- Complete transistor fabrication on all wafer to be stacked
- Form super via (TSV) on all wafer to be stacked
- Fill super via at the same time connections are made to transistors



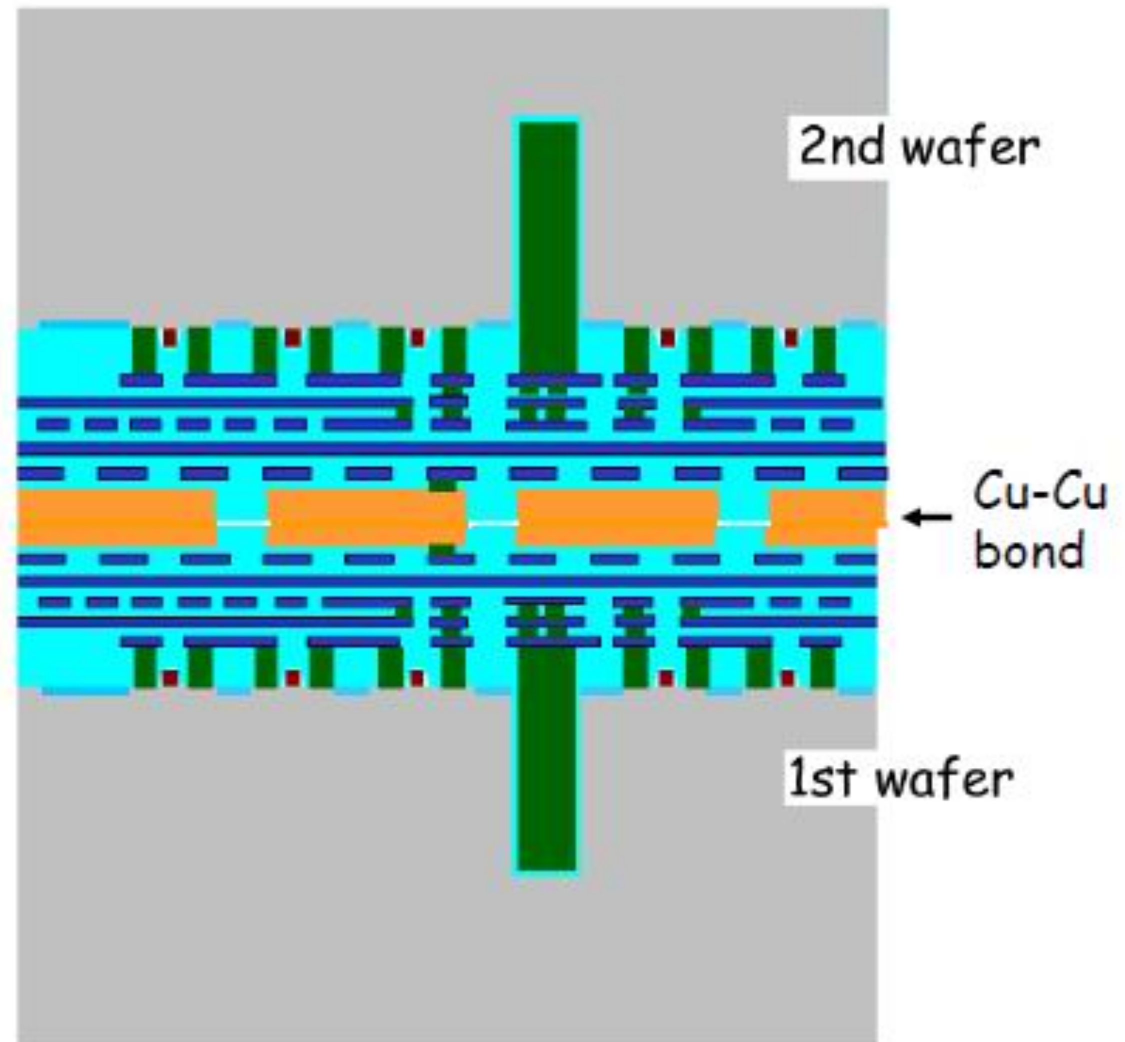
Tezzaron vertical integration process

- Complete back end of line (BEOL) processing by adding Cu metal layers and top Cu metal



Tezzaron vertical integration process

- Bond first layer to second layer using Cu-Cu thermo-compression bond

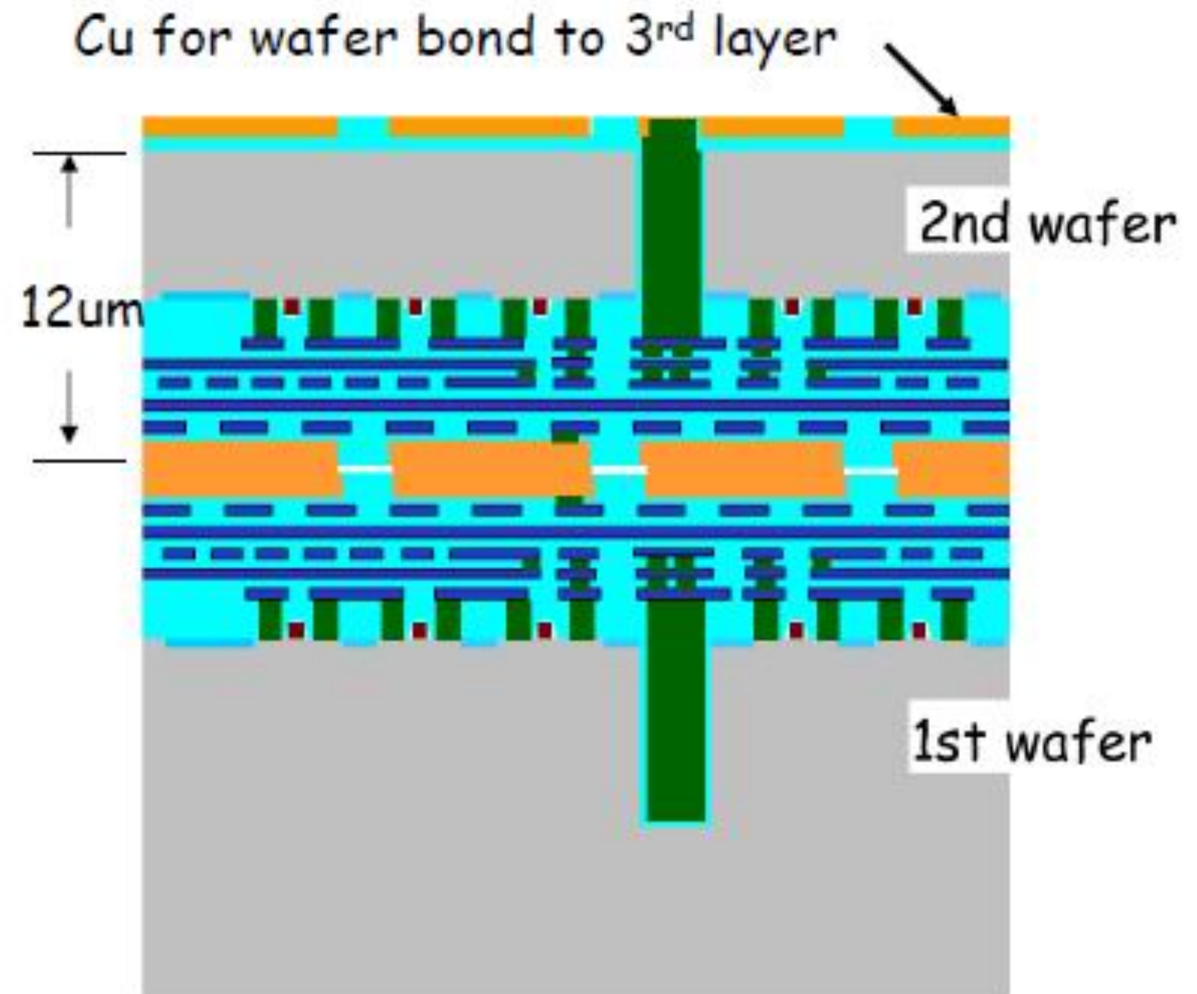


Tezzaron vertical integration process

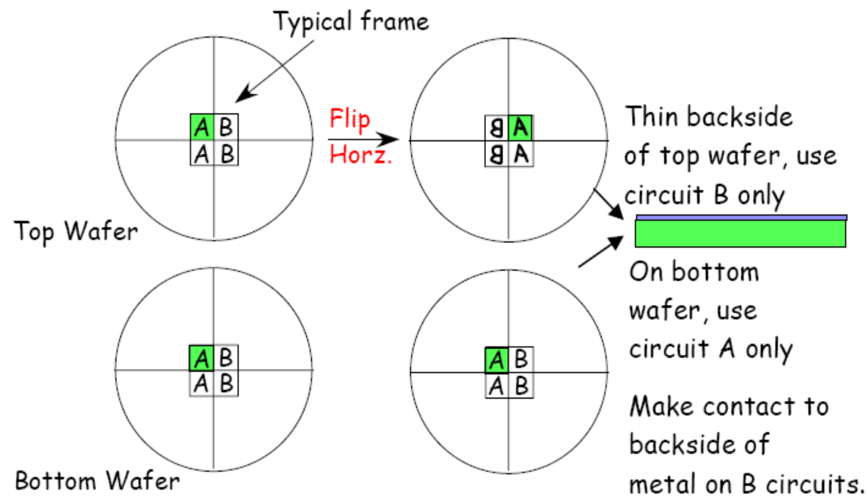
- Thin the second wafer to about 12 µm total thickness to expose super via
- Add Cu to back of second wafer to bond second wafer to third wafer

  OR

  add metallization on back of second wafer for bump bond or wire bond

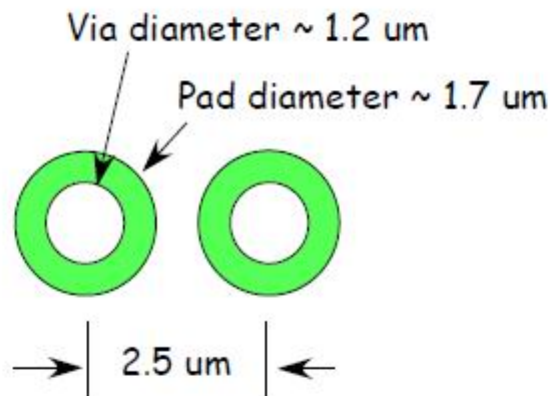


Tezzaron vertical integration process



Note: top and bottom wafers are identical.

Face to Face Bonding



- 3σ alignment=1 μm, missing bond connections=0.1 PPM
- Via size plays an important role in high density pixel arrays
- Tezzaron can place vias very close together