SuperB IFR electronics: update on prototype electronics and IFR_DAQ

Summary

(a) IFR subdetector update since last workshop
(b) update on the development of the IFR prototype electronics and DAQ system
(c) conclusions

IFR subdetector update since last workshop :
• an estimate of the manpower required for writing the TDR and bulding the IFR electronics has been prepared, based on the baseline design schematically represented in the diagram below:
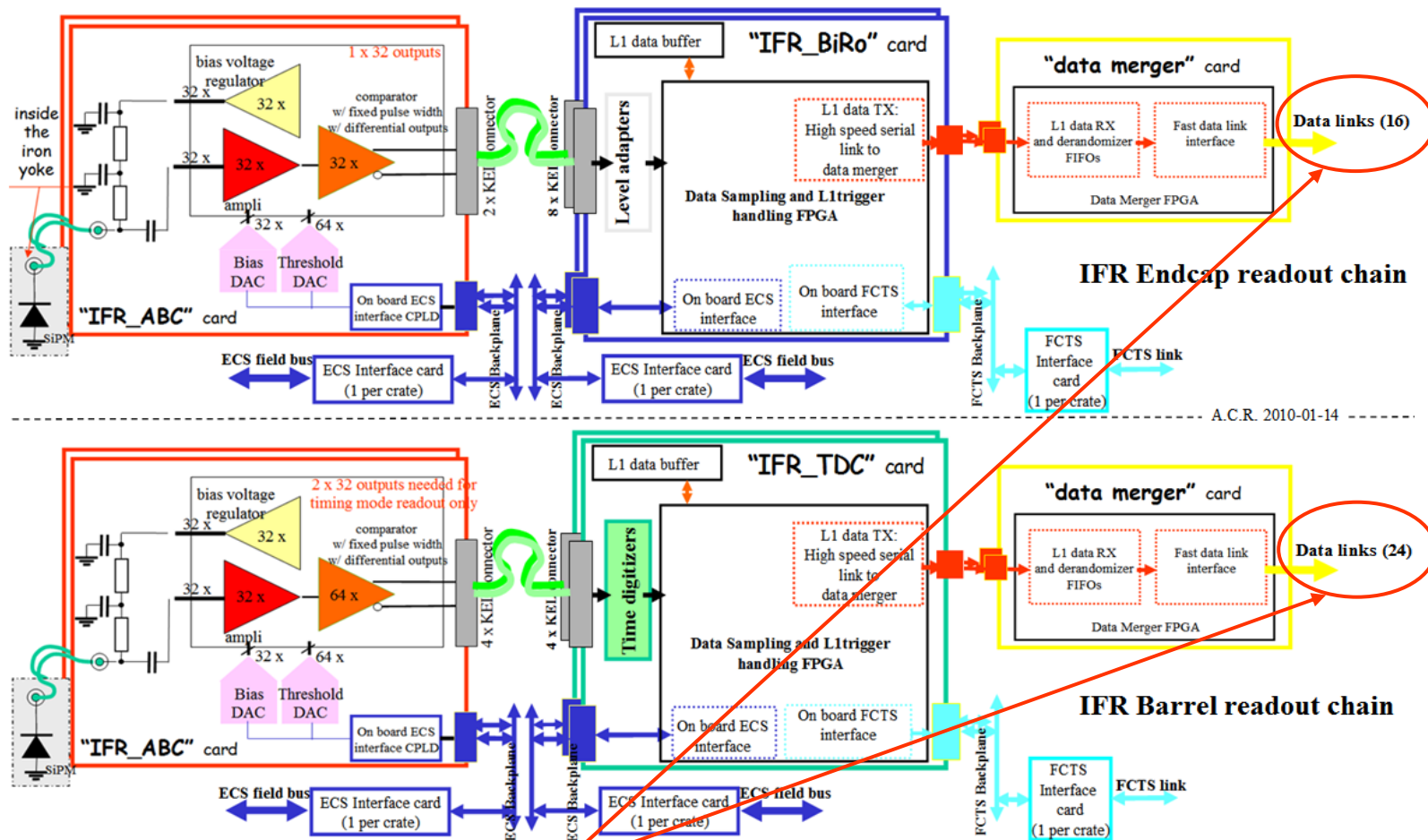
The numbers of high speed data links follow from the estimates already presented at previous workshops and depend upon:
-the current SiPM dark count estimates (more data after the test of the prototype)
-a trigger rate of 150kHz and a trigger extraction window of 150ns

The manpower estimate, while accounting also for some effort devoted to finding alternative solutions for the front end electronics and the TDCs, assumes, for the production phase that the system is built accordingly to the baseline design.

The assumption is made, in particular, that the digitizer crates could be placed in a moderately hostile area (distance? shield?). Low loss cables are foreseen to connect the differential output of the discriminators on the front end cards ("IFR_ABC") to the digitizers.

"IFR_ABC" crates
12 x in the barrel

"IFR_ABC" crates
8 x in the endcaps

"IFR_BiRO"crates
4 x in the endcaps

"IFR_TDC' crates
12 x in the barrel

A.C.R. 2010 Jan 13

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In order to evaluate the performance of ACAM's TDC-GPX under a neutron flux we are preparing a test setup based on the ATMD_GPX development kit.

The AM-GPX box contains (besides regulators and oscillator) a TDC-GPX chip, a local controller implemented in a flash-based Pro-ASIC APA075 FPGA and a set of transceiver chips. The ancillary devices interface the TDC-GPX digitizer to the PCI card installed in a desktop PC located out of the neutron beam.

The AM-GPX box could be put in the neutron beam in a "parasitic" fashion and we would try to evaluate the occurrence of data corruption due to single event upsets or the degradation in performance related to the integrated dose.
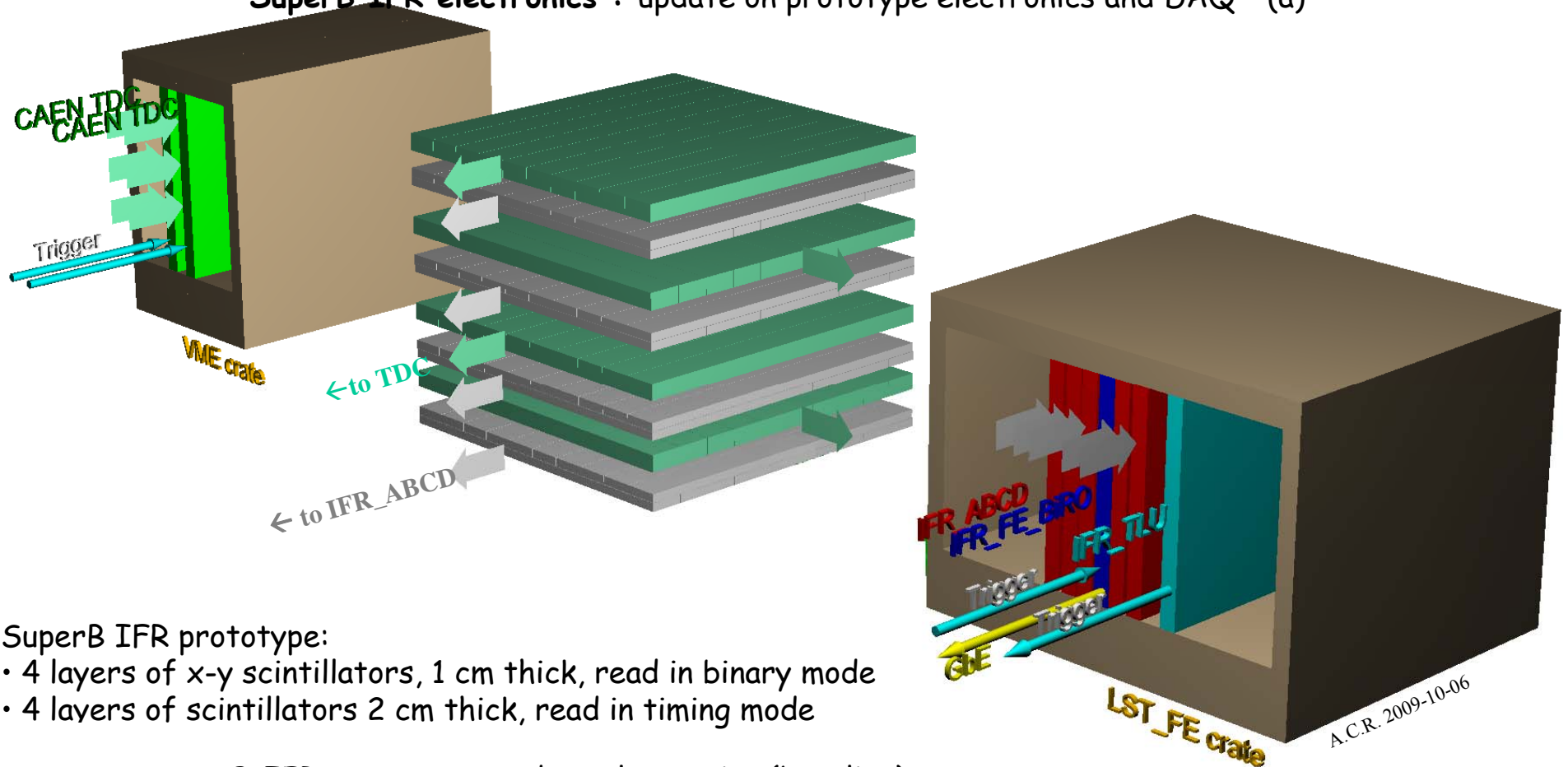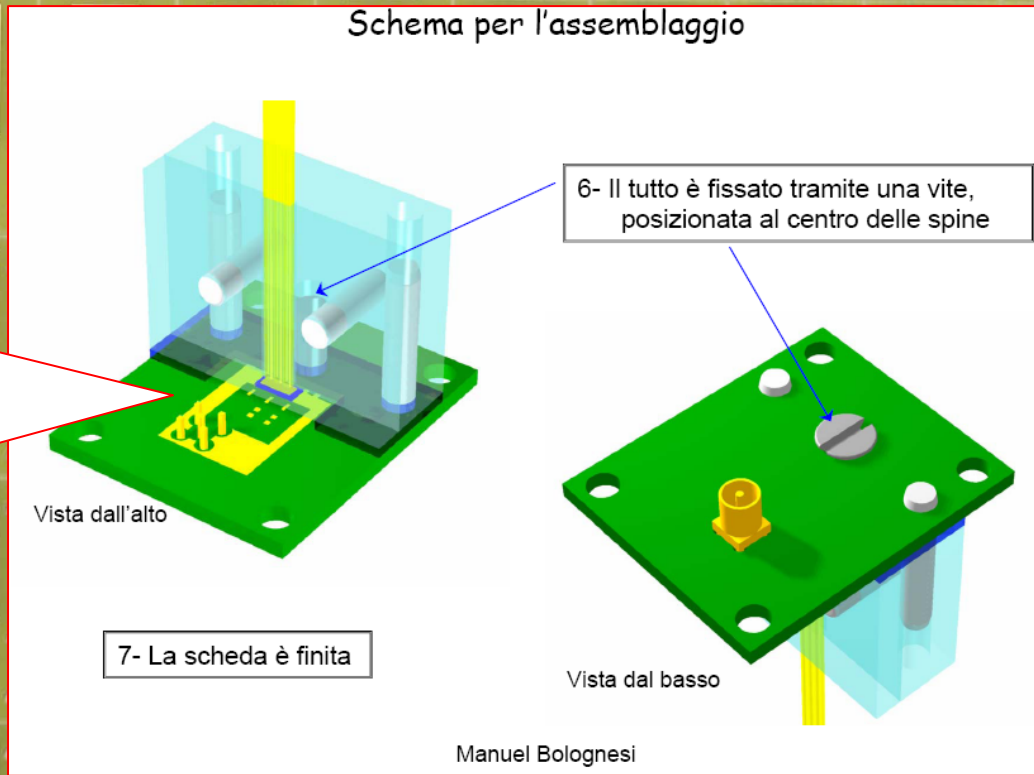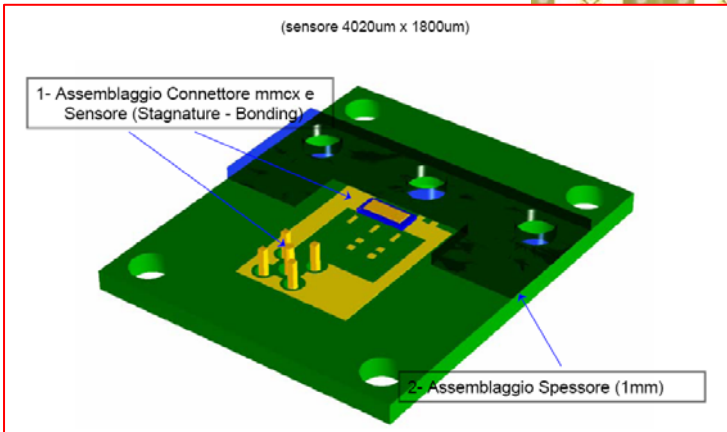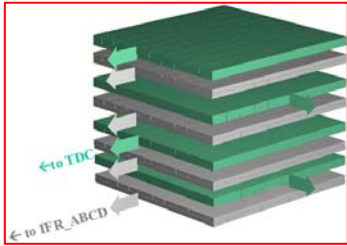
SuperB IFR prototype:
• 4 layers of x-y scintillators, 1 cm thick, read in binary mode
• 4 layers of scintillators 2 cm thick, read in timing mode

SuperB-IFR prototype readout electronics (baseline):
• "IFR_ABCD": sensor Amplification, Bias-conditioning, Comparators, (new!) Data processing:
it samples the level of the comparators outputs @ >= 80MHz and stores it, pending the trigger request
• "IFR_FE_BiRO": collects data from IFR_ABCD cards upon trigger request and sends it to DAQ PC (via GbE)
• "CAEN_TDC": a multi-hit TDC design based on CERN HP-TDC; hosted in a VME crate and read out via a VME CPU or via a VME-PCI bridge to the DAQ PC
• "IFR_TLU": a module (Trigger Logic Unit) to generate a fixed latency trigger based on primitives from the IFR prototype itself or from external sources

SiPM carrier PCB

Schema per l'assemblaggio

6- Il tutto è fissato tramite una vite, posizionata al centro delle spine

Vista dall'alto

7- La scheda è finita

Vista dal basso

Manuel Bolognesi

(sensore 4020um x 1800um)

1- Assemblaggio Connettore mmcx e Sensore (Stagnature - Bonding)

2- Assemblaggio Spessore (1mm)

SiPM carrier PCB with NiAu plating for bonding: fits all three type of sensors being manufactured by FBK-Trento.
Sensor die glueing position is determined by a removable countermask.

Agreement exist with Dr. Giovanni Ambrosi INFN-Pg for SiPM bonding

←to TDC

← to IFR_ABCD

IFR_ABCD

dimensions: VME 6U x 220mm

"IFR_ABCD" card features:

• ampli: two stage w/discrete components: BGA2748 + BGA2716

• discri: ADCMP562BRQ (PECL out, dual) or ADCMP563BRQ (ECL out, dual)

Programmable bias voltage
32 x

2 x 32 output needed for timing mode readout only

For the readout in timing mode of the SuperB IFR prototype it is foreseen to use two comparators at different thresholds (2.5 pe and 1.5 pe for instance) for each sensor

32 x

32 x

32 x
ampli

64 x

comparator
w/ programmable threshold
w/ fixed pulse width
w/ diff ECL outputs

4 x KEL connector

signal connector compatible with BaBar IFR signal cables (re-usable): KEL 8831E-034-170LD

• DAC: LTC2625CGN#PBF (I^2C, 12bit, octal)
• FPGA: Cyclone III ALTERA EP3C25Q240C8

SiPM

32 x   64 x

Bias DAC   Threshold DAC

CycloneIII FPGA based daughter card

A.C.R. 2009-10-06

CONNECTOR TO THE "LST_FE " CRATE BACKPLANE

inside the prototype "pizza box"

Outline of the **"IFR_ABCD"** card

(**A**mplifier, **B**ias, **C**omparator, **D**ataProcessing)

"IFR_ABCD" needed for prototype readout :

1 for each of 4 BiR0 planes (readout at only one end of scintillator) +

1 for each of 4 planes read with TDCs (readout at both ends of scintillator)

TOTAL "IFR_ABCD" cards: 8

"IFR_ABCD" status update :

• schematics submitted for layout; prototypes due in 6 wks

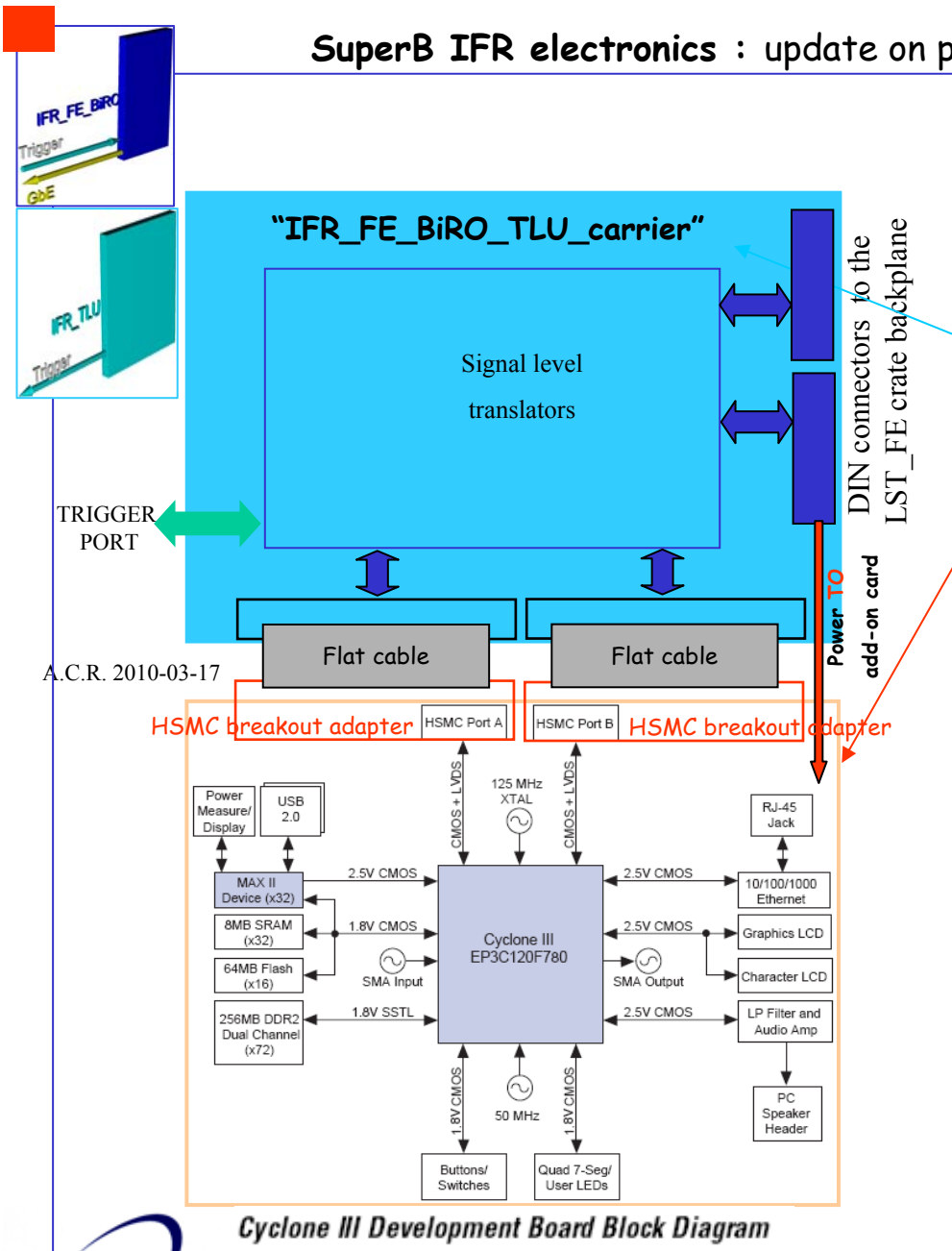• VHDL coded firmware ready; C-language routines for the NIOS-II microcontroller being coded

IFR_ABCD card: MMIC ampli design & test, schematics, and layout pre-placement by R. Malaguti, INFN-Ferrara

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"IFR_FE_BiRO_TLU_carrier"

Signal level translators

DIN connectors to the LST_FE crate backplane

TRIGGER PORT

A.C.R. 2010-03-17

Flat cable   Flat cable

Power TO add-on card

HSMC breakout adapter | HSMC Port A | HSMC Port B | HSMC breakout adapter

Power Measure/ Display | USB 2.0

125 MHz XTAL

RJ-45 Jack

CMOS + LVDS   CMOS + LVDS

MAX II Device (x32) — 2.5V CMOS — Cyclone III EP3C120F780 — 2.5V CMOS — 10/100/1000 Ethernet

8MB SRAM (x32) — 1.8V CMOS — SMA Input — 2.5V CMOS — Graphics LCD

64MB Flash (x16) — SMA Output — Character LCD

256MB DDR2 Dual Channel (x72) — 1.8V SSTL — 2.5V CMOS — LP Filter and Audio Amp

1.8V CMOS   50 MHz   1.8V CMOS

PC Speaker Header

Buttons/ Switches   Quad 7-Seg/ User LEDs

Cyclone III Development Board Block Diagram

Outline of the "**IFR_FE_BiRO_TLU**" module

"IFR_FE_BiRO_TLU" module features **(new)**:

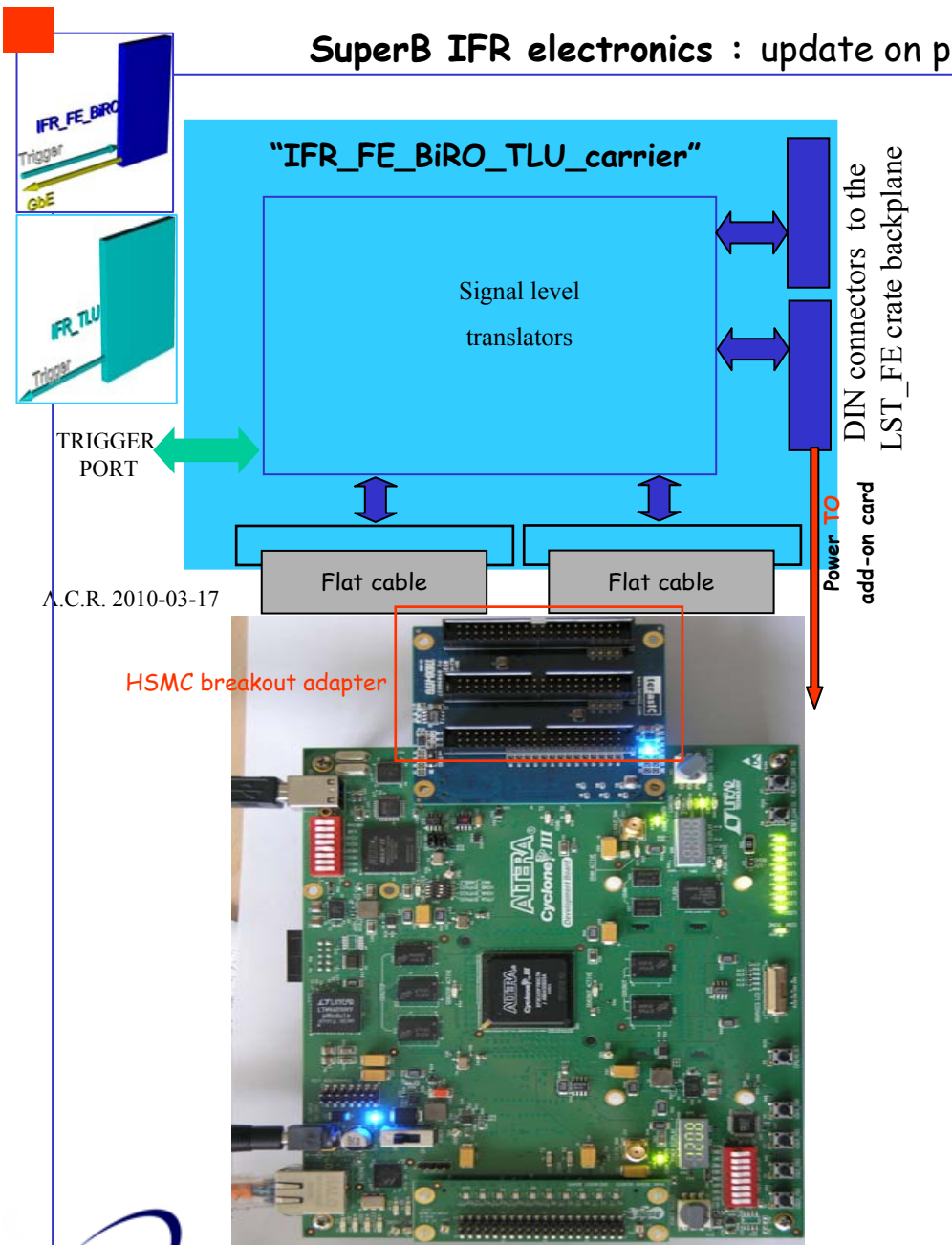The functions of the **IFR_FE_BiRO** and of the **IFR_FE_TLU** cards are combined into a single system made of

• a **carrier** card which fits in the "LST_FE" crate (6U x 220mm depth)

• an **add-on** card : it's simply the ALTERA Cyclone III development kit (**DK-DEV-3C120N**) equipped with breakout adapters for the kit's HSMC connectors

The **carrier** card hosts level adaptors and application specific I/O ports which allow the **add-on** card to:

• receive power
• receive the "fast OR" signals from the "ABCD" cards to generate triggers from
• generate and distribute triggers (also to the TDC system)
• generate and distribute clock and reset signals (also to the TDC system)
• poll data from the "ABCD" cards
• configure the programmable resources on the "ABCD" cards
• connect to the host PC running the DAQ software via ethernet (tcp/ip)

Total "**IFR_FE_BiRO_TLU**" needed for the prototype readout: 1

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"IFR_FE_BiRO_TLU_carrier"

Signal level

translators

DIN connectors to the LST_FE crate backplane

TRIGGER PORT

Power TO add-on card

A.C.R. 2010-03-17

Flat cable

Flat cable

HSMC breakout adapter

IFR_FE_BiRO

Trigger

GbE

IFR_TLU

Trigger

Outline of the **"IFR_FE_BiRO_TLU"** module

"IFR_FE_BiRO_TLU" module features: (continues)

The FPGA on board the **add-on** card is connected to the RUN CONTROL/DAQ PC of the prototype test setup via an Ethernet port.

The FPGA features a NIOS-II microcontroller which implements the full TCP/IP stack.

The NIOS-II receives commands (i.e. START, STOP, INIT) from the RUN CONTROL/DAQ PC on a TCP server socket and sends data to a TCP server socket on the PC. Data is collected through the LST_FE backplane from the "ABCD" cards upon a trigger request. The data collection section of the FPGA is coded in VHDL.

The FPGA of the add-on card generates the timing (clock and reset) for all the digitizers and handles the trigger distribution as well.

"IFR_FE_BiRO_TLU" status update :
• schematics of the "carrier card" is almost finished (pending FPGA pin assignment)
• "carrier card" layout turn around time expected to be ~3 wks
• "carrier card" PCB production and stuffing expected to be ~3 wks
•C-language routines for the NIOS-II microcontroller are coded and tested; VHDL coded firmware is being developed;

SuperB IFR electronics : update on prototype electronics and DAQ – (b)
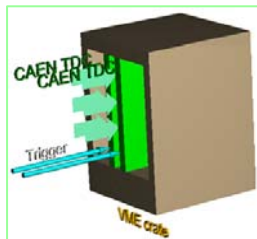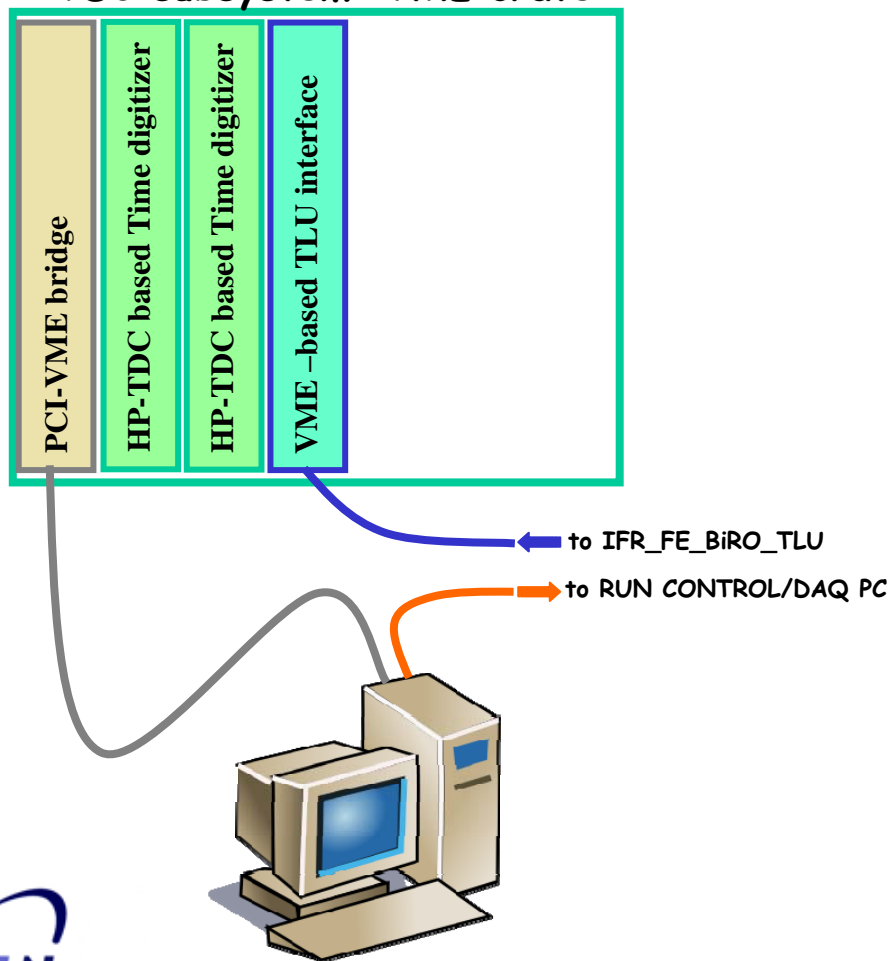
"TDC subsystem" features:

The **TDC subsystem** uses 2 commercial TDC modules based on CERN's HP-TDC to digitze the time of arrival of the pulses from the "ABCD" boards.

The **TDC subsystem** will also use a VME-based module to interface to the **"IFR_FE_BiRO_TLU"** and receive trigger/timing signals

The **TDC subsystem** VME crate will be controlled and read out by the "TDC-PC" via a PCI-VME bridge.

The TDC_PC will then send the triggered data to the RUN CONTROL/DAQ PC via a TCP/IP connection.
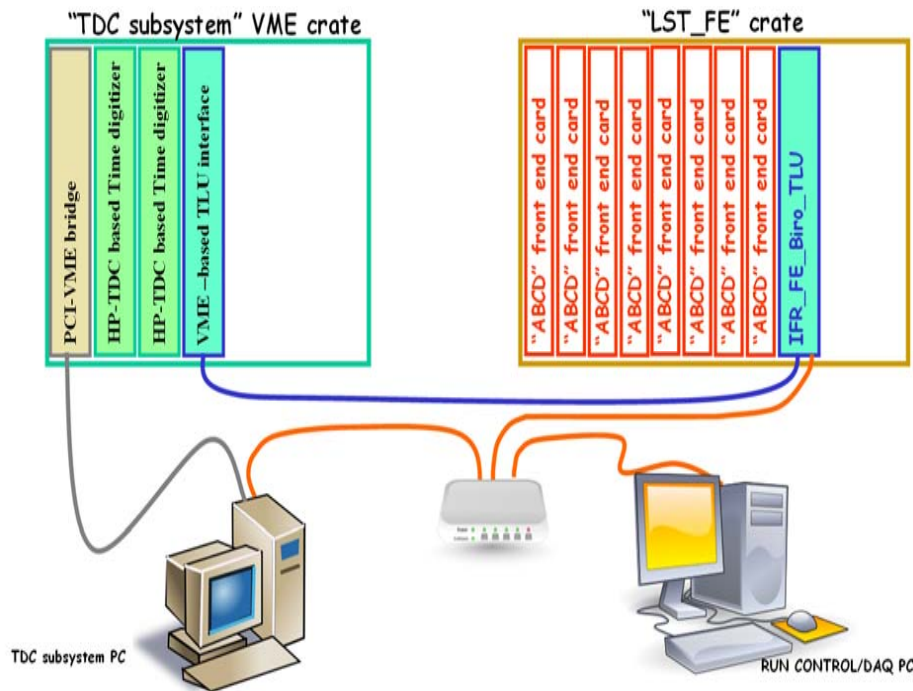
"TDC subsystem" VME crate

PCI-VME bridge

HP-TDC based Time digitizer

HP-TDC based Time digitizer

VME –based TLU interface

to IFR_FE_BiRO_TLU

to RUN CONTROL/DAQ PC

"TDC subsystem" status update :

• the readout of a VME TDC is operating
• code must be written to format the TDC measurements into formatted events
• the VME based – TLU interface module exists but needs a simple firmware upgrading

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SuperB IFR electronics : update on prototype electronics and DAQ – (b)

outline of the run control / daq system for the IFR prototype

"TDC subsystem" VME crate

PCI-VME bridge | HP-TDC based Time digitizer | HP-TDC based Time digitizer | VME –based TLU interface

"LST_FE" crate

"ABCD" front end card ×8 | IFR_FE_Biro_TLU

TDC subsystem PC

RUN CONTROL/DAQ PC

During the run initialization phase (INIT) the RUN CONTROL / DAQ PC sends commands and configuration parameters over Ethernet to the TDC-PC and the "IFR_FE_BIRO_TLU" to properly configure the programmable features of the system.

The "**IFR_ABCD**" cards generate trigger primitives which are:
• the OR of all "high threshold" channels from a plane read out in "timing" mode
• either the (OR of the X-view) OR (OR of the Y-view) or (choice made during INIT phase)
  the (OR of the X-view) AND (OR of the Y-view) for the channels from a plane readout in binary mode
These primitives are collected by the "IFR_FE_BIRO_TLU" over the backplane of the "LST_FE" crate.

The "**IFR_FE_BiRO_TLU**" card generates a trigger if the primitives and the LUT loaded during the INIT phase require so. The trigger is sent also to the **VME_based TLU interface** and from that to the TDCs. A **TDC_BUSY** signal is set in the **VME_based TLU interface** and returned to the **IFR_FE_BiRO_TLU**, which uses it, together with its own **BiRO_BUSY**, to block further triggers.
When the TDC-PC and the **IFR_FE_BiRO_TLU** systems have readout the digitizers the BUSY bits are cleared and a new trigger can be generated and served as the data from the previous one is being transferred over the Ethernet port to the RUN CONTROL/DAQ PC.

Each event data block is framed by an HEADER and a TRAILER containing a local trigger count, incrementing with each new trigger served **and a trigger time-stamp locally generated; this should be sufficient**, being the whole system synchronous, **to guarantee the right matching of events from the two subsystems**. Eventually an additional **trigger_ID** tag could be distributed by the **IFR_FE_BiRO_TLU** to the **VME_based TLU interface** and from that be added to the TDC data packet

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Conclusions:

At the moment the electronic shop of INFN Ferrara is focused on completing the readout electronics / DAQ for the prototype in time for the delivery of the SiPM sensors.

Todo list (in the short period):

• study the issue of radiation tolerance of one of the key elements, the time digitizer, in the IFR electronic chain.
• follow up the request of the ETD/Online team with an update of our estimates of data rates after the next SiPM irradiation test and an estimate of the setup time.

Points to think of for the parallel sessions (2)

• Safety factors on dataflow:
  • We would like to get the safety factors used for the readout link calculations for each subsystem and to understand what they are based on.
  • Subsystems shouldn't apply general safety margins like that on trigger rate
      => that one will be common to the whole experiment
  • But they should for what concerns their channel occupancy (based on channel hit rate and trigger window width)

• Derandomizer depth:
  • Should we ensure that no data could be lost after throttling in the derandomizer buffer even in the case of worst size events ?

• ECS bandwidth:
  • Subdetectors should think of the bandwidth they need to set up the FEE at startup or reload it because of radiation policy
  • Set up time has to be reasonable (seconds)
  • This is a key factor in defining the number of ECS links needed (10Mbits/s per links)

D. Breton - SuperB Annecy Workshop - March 2010

Spare slides

What is a moderately hostile environment ?

From:

Compact data acquisition and power supply system designed for hostile environment condition concerning radiation and magnetic field

L. Colombini, M. Lippi, A. Mati, G. Passuello, S. Petrucci[*], M. Pieracci, G. Selmi, C. Tintori

CAEN S.p.A., Via Vetraia 11, Viareggio, Italy
s.petrucci@caen.it

"IFR ABC" crates
12 x in the barrel

"IFR_ABC" crates
8 x in the endcaps

"IFR_BiRO"crates
4 x in the endcaps

"IFR_TDC' crates
12 x in the barrel

A.C.R. 2010 Jan 13

A. Radiation Tolerance

The crate will operate in a moderate hostile environment for what concerns total levels of radiation (Table 1) [8]. If damages for total integrated dose are likely to be negligible, protections for latchups are needed, as well as an adequate SEU protection/detection.

Table 1: The expected doses and hadron fluences for 10 years

Total dose	1.2 Gy
Neutron fluence (>20 MeV):	$2.1 \ 10^9 \ cm^{-2}$
Max Charged hadron/neutron (>20MeV) fluence rate	$89 \ Hz/cm^2$

The SEL protection is achieved by dividing each board in sections with separate power supply. Each section is independently monitored and "protected" by a current-limiting device (MAX893L), while an Atmel µC handles the section ON/OFF status: if SEL faults are signalled by the relevant indicators, the Atmel µC detects them and switches off the sections with SEL faults in order to correct the SEL condition and to avoid permanent damages.

The SEU protection/detection architecture is based on radiation tests carried on the key components of the ALICE TOF readout modules [9]. Such tests reported an esteem of the SEU rates and helped to select the proposed components. The implemented solution was then the following: Flash based FPGA Actel ProAsic Plus (APA 750), which are substantially immune to SEU in the configuration bits, are used for vital sections, while other sections use RAM based ALTERA FPGA (reprogrammed after a CRC error). The SRAM implements a CRC check in order to identify NOT valid data. No SEE effect was observed in the Flash and in the Atmel µC (ATMEGA). The HPTDC look-up tables will be periodically monitored via CRC and require reload from Flash memory.
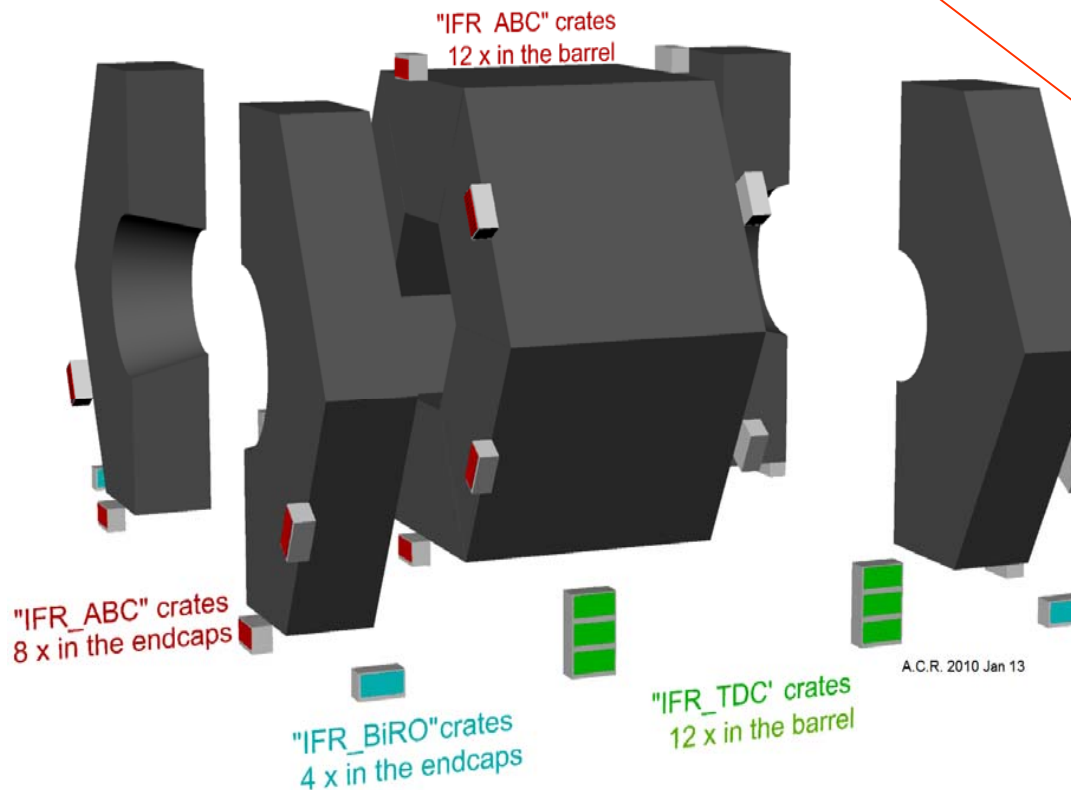
outline of the IFR DAQ electronics: data bandwidth estimates

SuperB-IFR numerology:

• Barrel: N_Barrel   = 3600 scintillator bars
(quoting G. Cibinetto)

Assuming:

• readout in TIMING mode with N_th (=2) thresholds:
both the high threshold (2.5 p.e. for instance) and the low threshold
(1.5 p.e. for instance) crossing times are acquired by the F.E., the
second threshold crossing validating the first for better noise
rejection.

• each scintillator is readout from N_sides (=2) ends
  -> total number of TDC channels: N_TDC_ch

N_TDC_ch = (N_Barrel) * N_sides * N_th = 14.400

N_TDC_board = N_TDC_ch / 64 = 225

W.Sands., Princeton Univ., 2003

Hopefully the tests on the prototype will show that it will be possible to keep:
N_th = 1
but in the meantime it is better to brace for the worst!
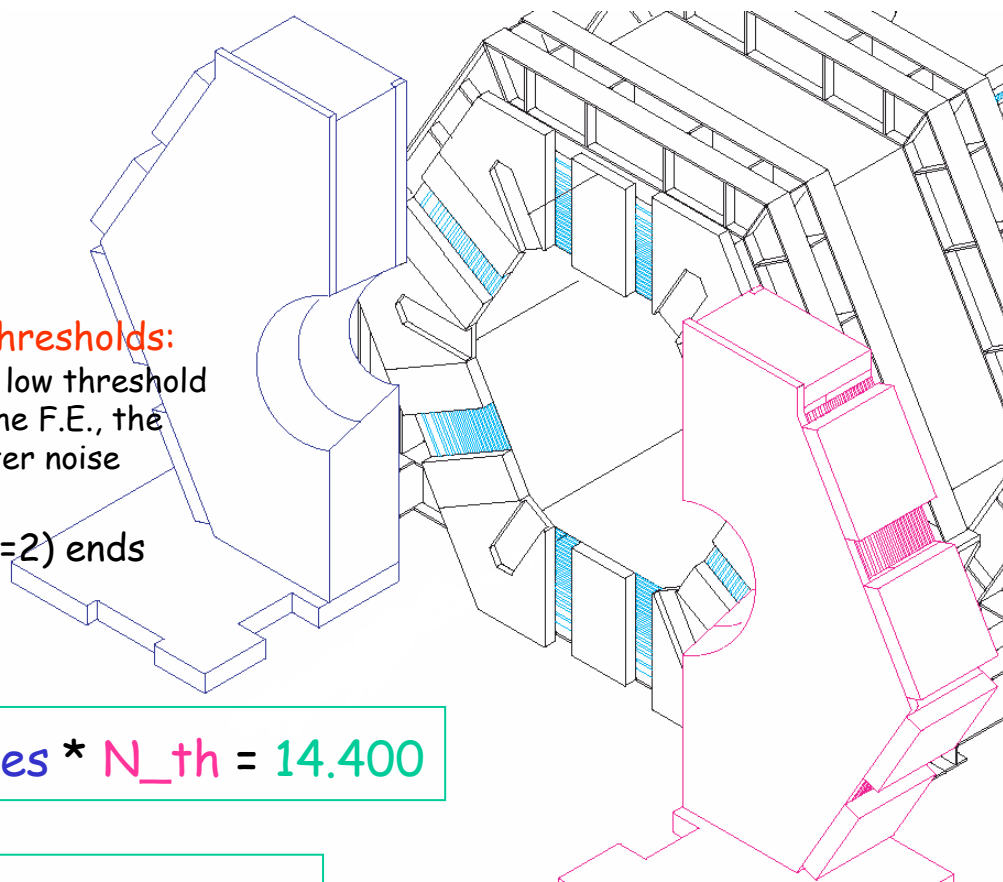
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outline of the IFR DAQ electronics: data bandwidth estimates WITH TIMING READOUT FOR BARREL

SuperB-IFR numerology:

"Physics" rate : **500kHz**/channel, <u>in the hottest region</u>, arising from:

      - particle rate : O(100Hz) / cm^2 (including background)

      - dimensions of a detector element : < 400cm x 4cm (thickness 20mm)

(quoting R.Calabrese, W.Baldini, G.Cibinetto)

"Dark count" rate   : **for a 1mm^2 SiPM by FBK**:

(quoting R.Malaguti, L.Milano test results in Ferrara)

@ 0.5pe threshold	**@ 2.5pe threshold**
- @ 25°C, 34.4V: ≈ 360kHz	- @ 25°C, 35V: ≈ 20kHz
- @ 5°C, 33.8V: ≈ 128kHz	- @ 5°C, 34V: ≈ 6.3kHz

!!! The "dark count" rate scales with the sensor's area and we don't know yet which would be the final area of the sensor of choice (a 4mm^2 is also being considered)

!!! We need to have, on each processing channel, one comparator with a low threshold (0.5pe? 1.5pe? Only prototype test will tell) → it's TDC input will see the highest rate.

Let's consider a "Hit" rate of:

Hit_rate = physics_rate + dark count_rate ≤ 1MHz per TDC input !!!

it is compatible with the TDC-GPX maximum sustained input rate

outline of the IFR DAQ electronics: data bandwidth estimates WITH TIMING READOUT FOR BARREL

> if we do L1 trigger matching on board

--- BARREL

- assuming a 150ns trigger window

- assuming that trigger matching is performed at the front end cards

- assuming a "hit rate per scintillating element" of 1MHz per channel in the barrel (500Khz of "physics" + 500KHz of dark count rate because of the low threshold needed to improve timing precision)

- assuming that an event from an "IFR_TDC" board is built like outlined below:

- Header = Board ID + Frame ID (allows to reconstruct <u>ABSOLUTE</u> timing for hit records) : 12 Byte

- Channel ID + hit timing information <u>RELATIVE</u> to beginning of frame : 4 Byte per Hit

- Trailer = L1_Trigger_Data + WordCount + error code: 12 Byte

- assuming that on each TDC half of the channels has a 1MHz input rate and half has a 500KHz input rate →

The TDC event size and data rates can be estimated as follows:

<"IFR_TDC" event size> = 12 + [(0.15us * 1MHz) hit * 32 + (0.15us * 0.5MHz) hit * 32] * 4 + 12 ≈ 12 + 8 * 4 + 12 ≈ **0.06kB**

and thus the "**<u>trigger matched</u>**" data rate produced by each "IFR_TDC" is:

<"IFR_TDC" data rate> = 150KHz * 0.06kB ≈ **9MB/s**

outline of the IFR DAQ electronics: data bandwidth estimates WITH TIMING READOUT FOR BARREL

if we do L1 trigger matching on board

BARREL summary

- Number of "IFR_TDC"s = 225

- Numbers per "IFR_TDC" board:
  <"IFR_TDC" event size> = 0.06kB
  <"IFR_TDC" data rate> = 9MB/s
- Average event size for the whole Barrel read in timing mode:
  <Event size Barrel> = 0.06kB * 225 ≈ 13.5kB
- Total data rate produced by the Barrel:
  <Event data rate Barrel> = 9MB/s * 225 ≈ 2,025MB/s
- Tentative calculation of the number of links required (assuming the "concentration" of 10 "IFR_TDC" output links into 1 link at 2Gbps):
  Number_of_data_links_barrel = 225 / 10 ≈ 24
  (i.e. 2 links per digitizer crate)

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outline of the IFR DAQ electronics: data bandwidth estimates WITH BINARY READOUT FOR ENDCAP

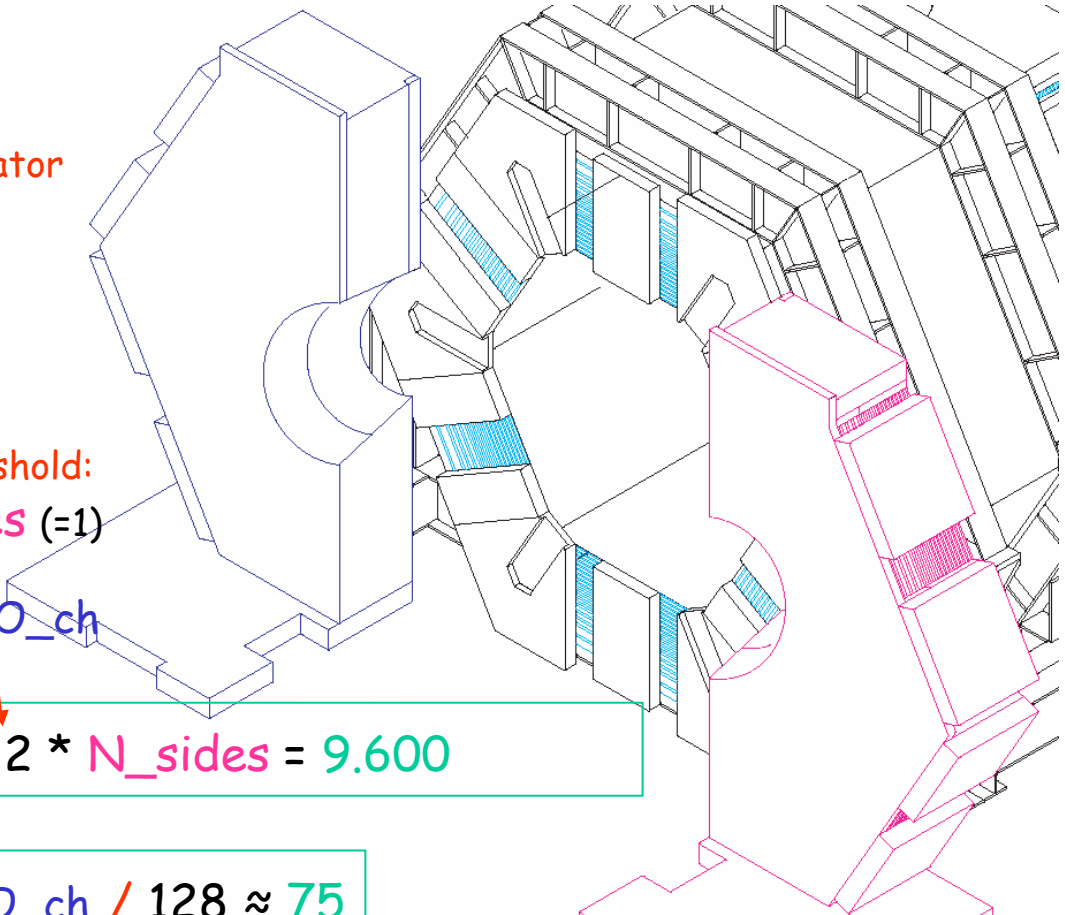SuperB-IFR numerology:

• EndCaps: N_EndCap = 2400 + 2400 scintillator bars
(quoting G. Cibinetto)

Assuming:
• the number of (thin) scintillators doubles
  (for X-Y readout; it's a coarse estimate)
• readout in BINARY mode with **single** threshold:
• each scintillator is readout from N_sides (=1) ends

    -> total number of BiRO channels: N_BiRO_ch

$$\text{N\_BiRO\_ch} = (\text{N\_EndCap}) * 2 * \text{N\_sides} = 9.600$$

$$\text{N\_BiRO\_Board} = \text{N\_BiRO\_ch} \; / \; 128 \approx 75$$

W.Sands., Princeton Univ., 2003

For bars read out in "binary" mode N_sides has settled to: 1

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outline of the IFR DAQ electronics: data bandwidth estimates WITH BINARY READOUT FOR ENDCAP

SuperB-IFR numerology:

"Physics" rate : **500kHz**/channel, <u>in the hottest region</u>, arising from:

- particle rate : $O(100Hz) / cm^2$ (including background)
- dimensions of a detector element : < 400cm x 4cm (thickness 20mm)

(quoting R.Calabrese, W.Baldini, G.Cibinetto)

"Dark count" rate : **for a 1mm^2 SiPM by FBK**:

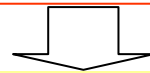(quoting R.Malaguti, L.Milano test results in Ferrara)

@ 0.5pe threshold	**@ 2.5pe threshold**
- @ 25°C, 34.4V: ≈ 360kHz	- @ 25°C, 35V: ≈ 20kHz
- @ 5°C, 33.8V: ≈ 128kHz	- @ 5°C, 34V: ≈ 6.3kHz

!!! The "dark count" rate scales with the sensor's area and we don't know yet which would be the final area of the sensor of choice (a 4mm^2 is also being considered)

!!! We need to have, on each processing channel, just one comparator with a 2.5pe threshold
→ The dark count rate @ 2.5pe threshold is just a fraction of the physics rate

Let's consider a "Hit" rate of:

Hit_rate = physics_rate + dark count_rate ≈ 600kHz per BiRO input

outline of the IFR DAQ electronics: data bandwidth estimates WITH BINARY READOUT FOR ENDCAP

if we do L1 trigger matching on board

- **assuming a 150ns trigger window**
- **assuming that trigger matching is performed at the front end cards**
- assuming a "hit rate per scintillating element" of 600kHz per channel in the endcaps (500Khz of "physics" + 100KHz of dark count rate because in the endcap we can set a higher threshold w.r.t the barrel)
- assuming that an event from an "IFR_BiRO" board is built like outlined below:

- Header = Board ID + Frame ID (allows to reconstruct <u>ABSOLUTE</u> timing for hit records) : 12 Byte
- 8 samples within the trigger window for all 128 inputs → 8 * (128/8) = 128 Byte
- Trailer = L1_Trigger_Data + WordCount + error code: 12 Byte

The "IFR_BiRO" event size and data rates can be estimated as follows:

<"IFR_BiRO" event size> = 12 + 128 + 12 ≈ **0.152kB**

and thus the "**trigger matched**" data rate produced by each "IFR_BiRO" is:

<"IFR_BiRO" data rate> = 150KHz * 0.152kB ≈ **22.8MB/s**

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outline of the IFR DAQ electronics: data bandwidth estimates WITH BINARY READOUT FOR ENDCAP

if we do L1 trigger matching on board

ENDCAP summary

- **Number of "IFR_BiRO"s = 75**

- Numbers per "IFR_BiRO" board:
  - **<"IFR_BiRO" event size> = 0.152kB**
  - **<"IFR_BiRO" data rate> = 22.8MB/s**
- Average event size for the whole Endcap read in binary mode:
- **<Event size Endcap> = 0.152kB * 75 ≈ 11.4kB**
- Total data rate produced by the Endcap:
- **<Event data rate Endcap> = 22.8MB/s * 75 ≈ 1,710MB/s**
  - Tentative calculation of the number of links required (assuming the "concentration" of 5 "IFR_BiRO" output links into 1 link at 2Gbps):
    - **Number_of_data_links_endcap = 75 / 5 ≈ 16**
    - **(i.e. 4 links per digitizer crate)**

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