

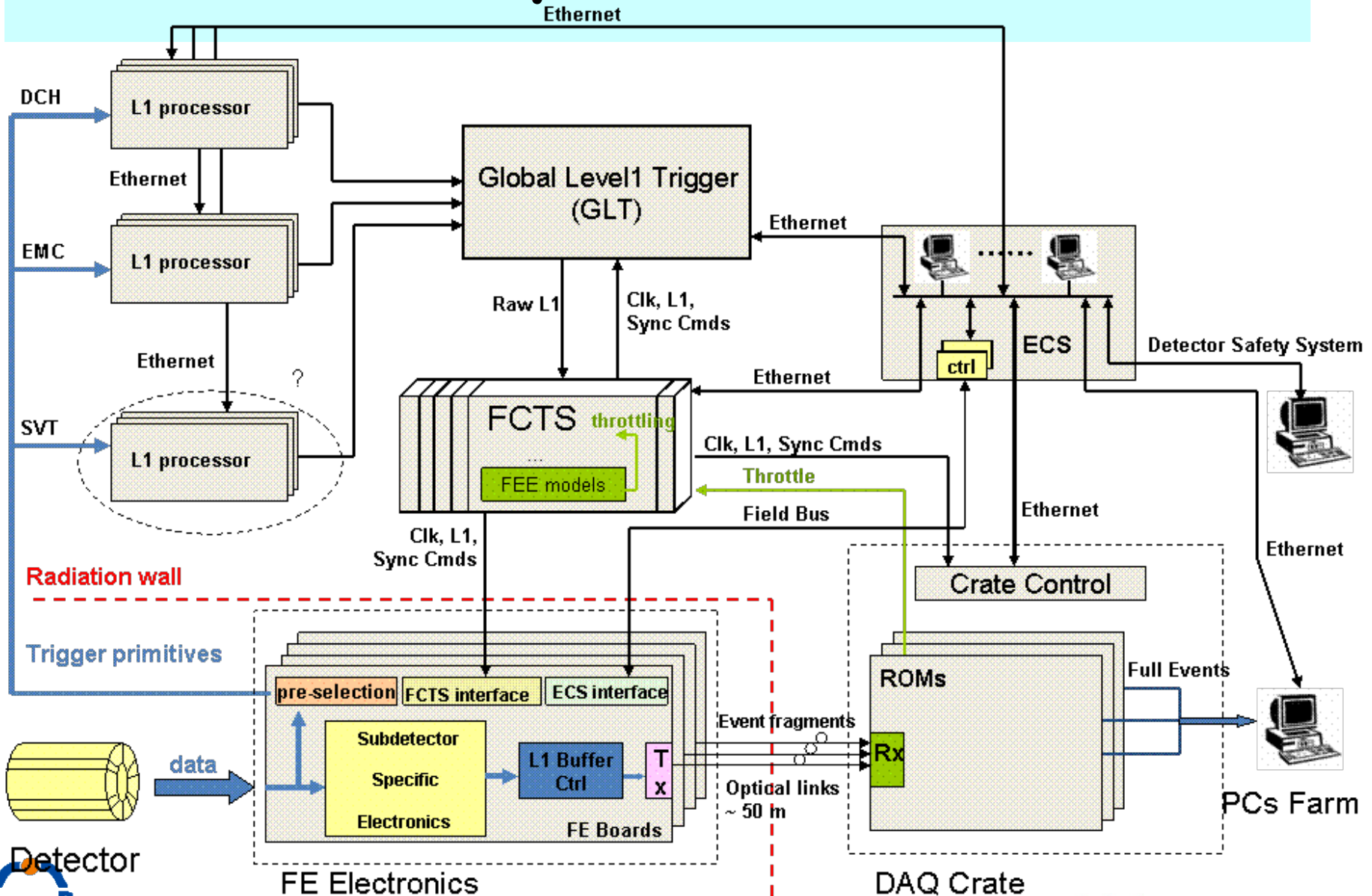


PROPOSAL FOR FTCS & ECS

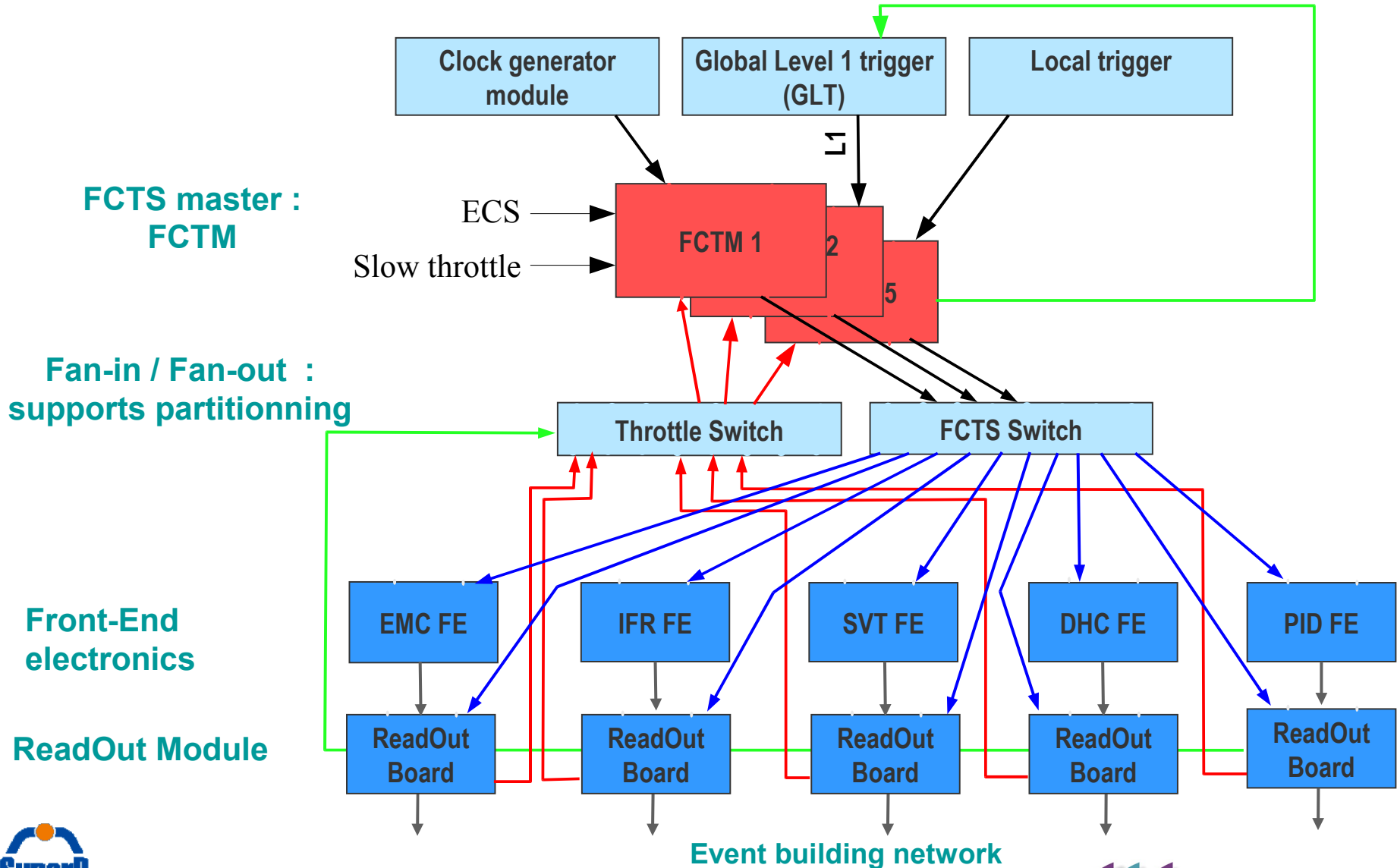
FCTS requirements

- Synchronizing the experiment with the machine.
- Delivering and buffering the clock to the experiment.
- Dealing with the raw L1 trigger decision.
- Throttling the latter.
- Permits the partitioning the system into independent subsystems or groups of subsystems.
- Generating programmable local trigger for calibration and commissioning.
- Generating different commands (calibration pulse, reset, BxID and event ID).
- Managing the stack of IP addresses for PC farm.
- Keeping trace of all event-linked data to put in the event readout

Overall system architecture

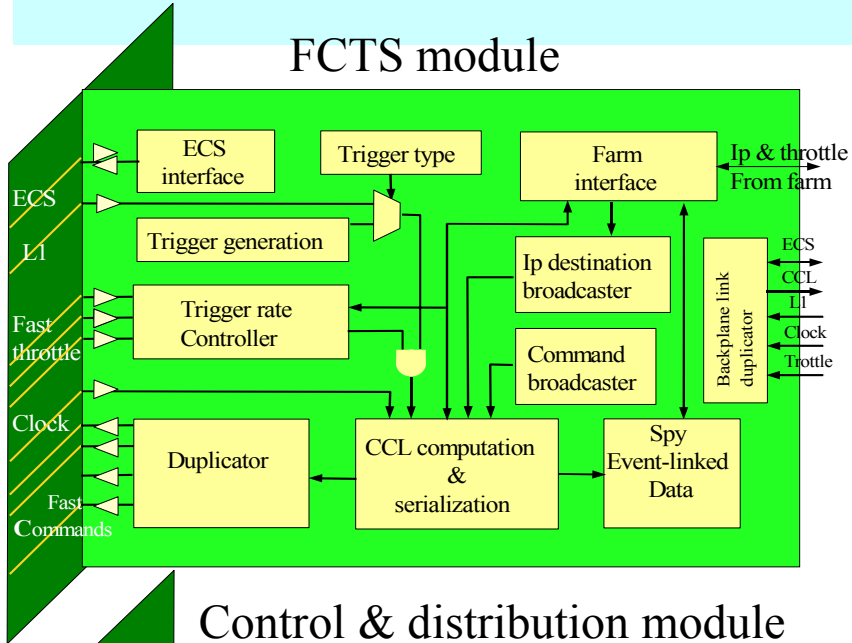


FCTS Architecture

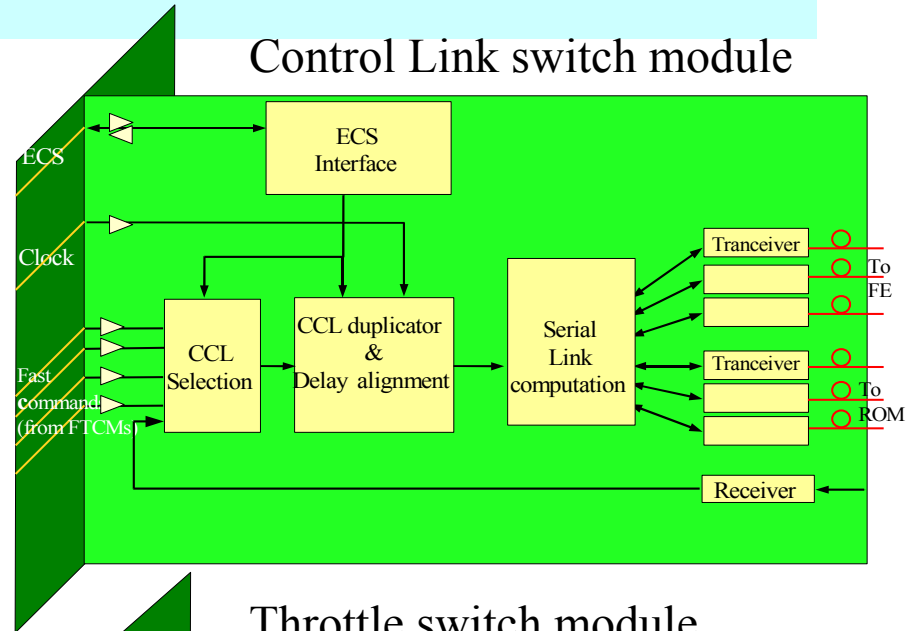


FCTS Boards

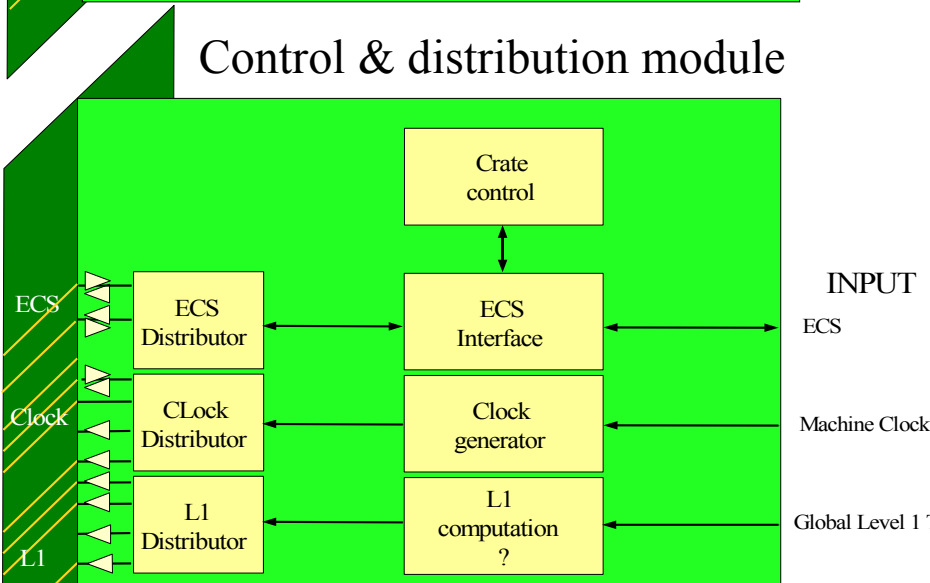
FCTS module



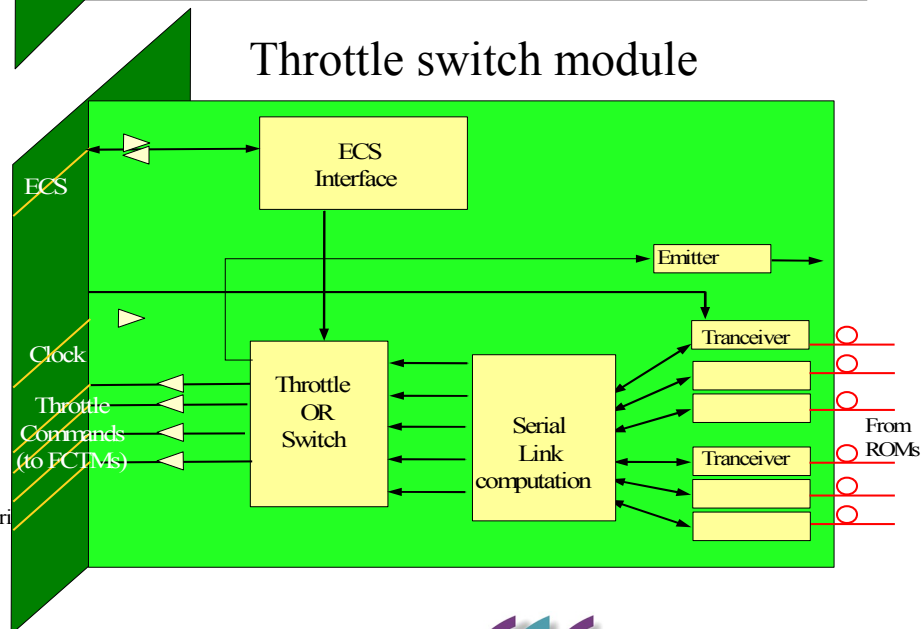
Control Link switch module



Control & distribution module

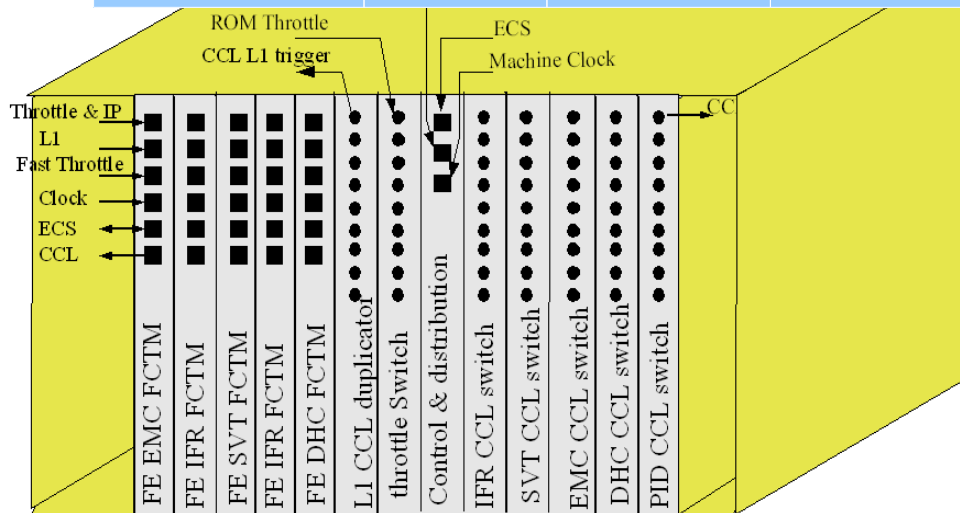


Throttle switch module



Crate version 1

Physical slot	1	2	3	4	5	6	7
Logical slot	7	6	5	1	2	3	4
Slot type	Ctrl. Swit.	FCTM	Thro. Swit.	Ctrl & distr	Ctrl. Swit.	FCTM	Thro. Swit.
		6 - 5	6 - 5	1 - 2	3 - 2	3 - 2	
	6 - 7	6 - 7		1 - 3		3 - 4	3 - 4
				1 - 4			
				1 - 5			
				1 - 6			
				1 - 7			



Custom crate:

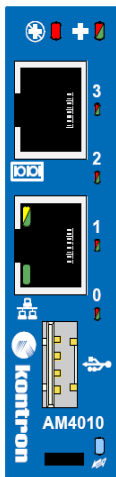
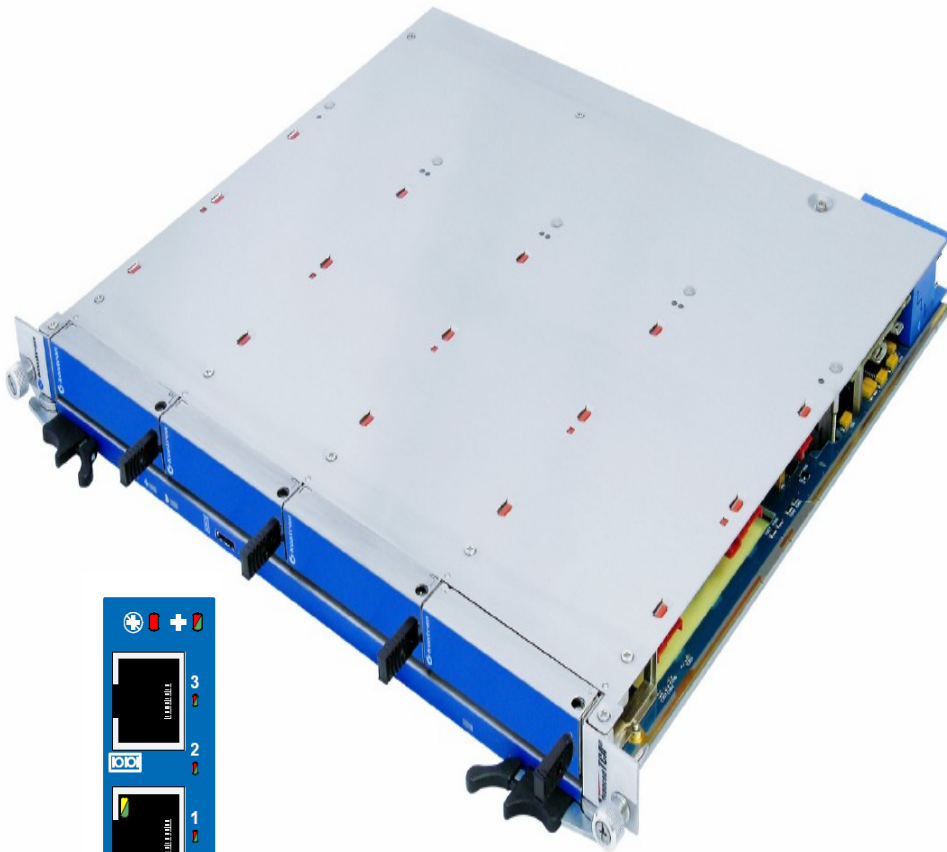
9U crate.

Custom backplane.

Easy board design.

Cost???

FCTS crate version 2



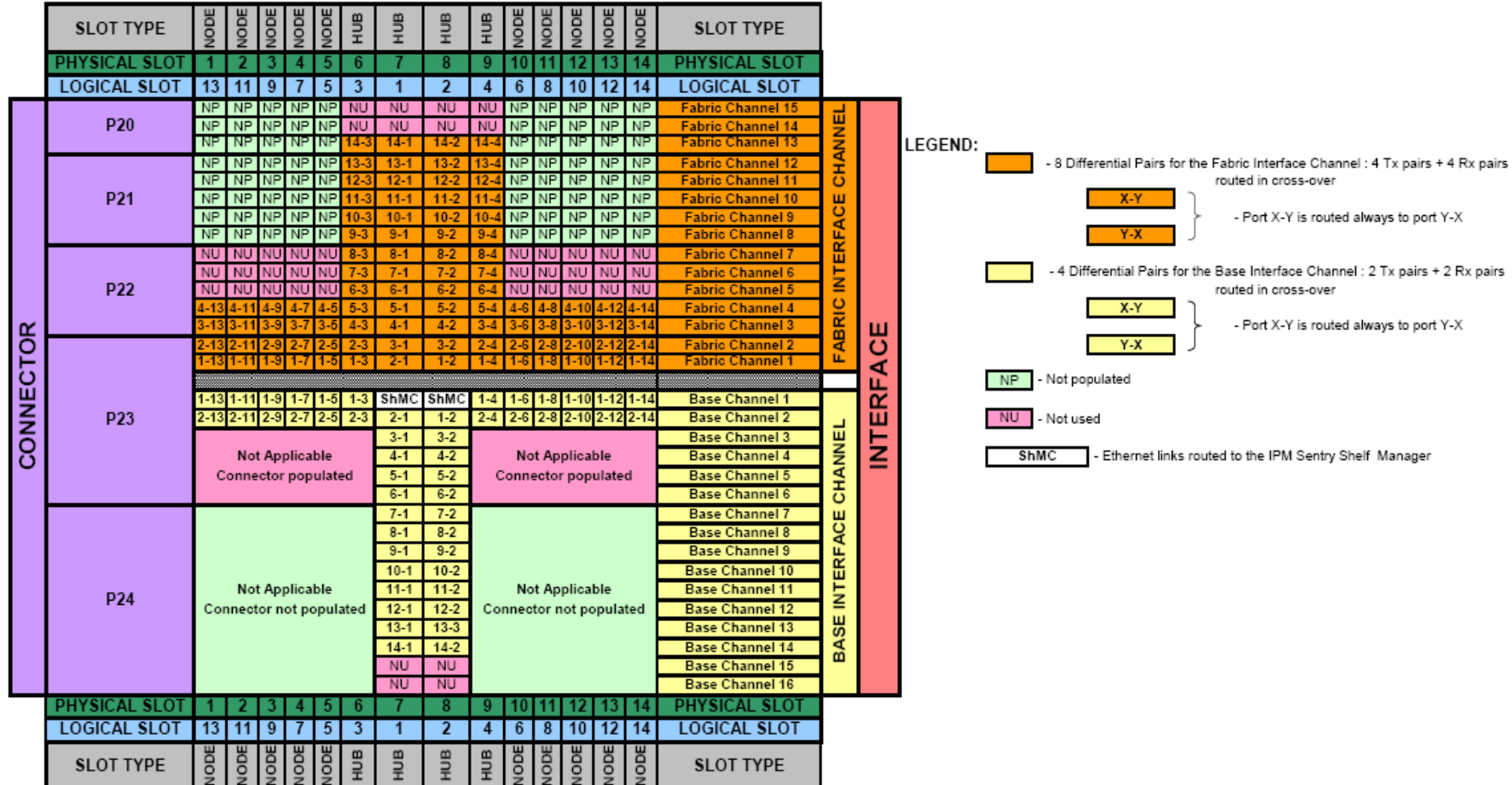
ATCA Standard: 2 solutions

- 1) “custom“ use.
- 2) Full standard compatibility

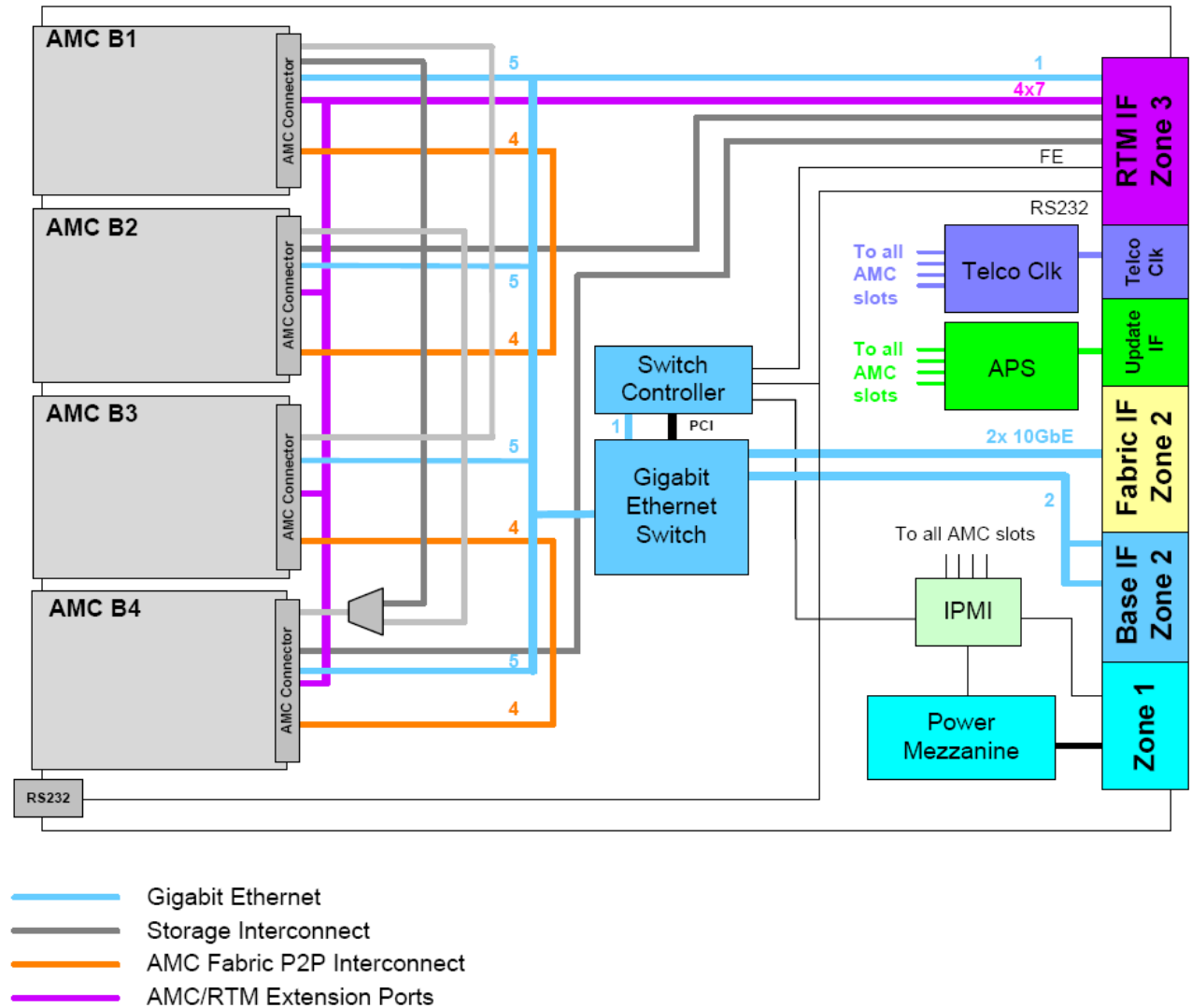
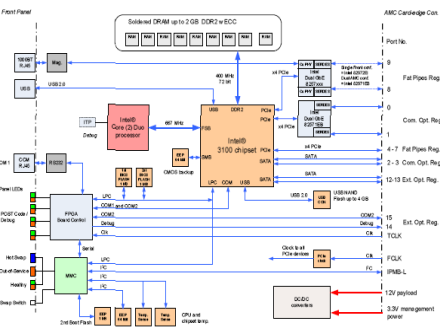
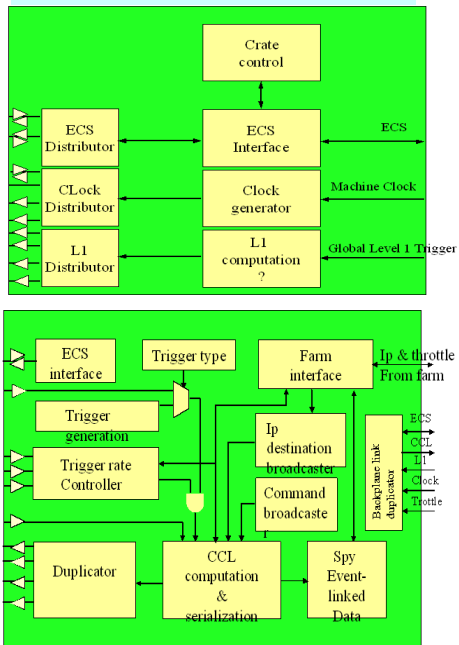
ATCA Backplane

Interconnection diagram for ATCA Dual-Dual Star 14 Slots Backplane:

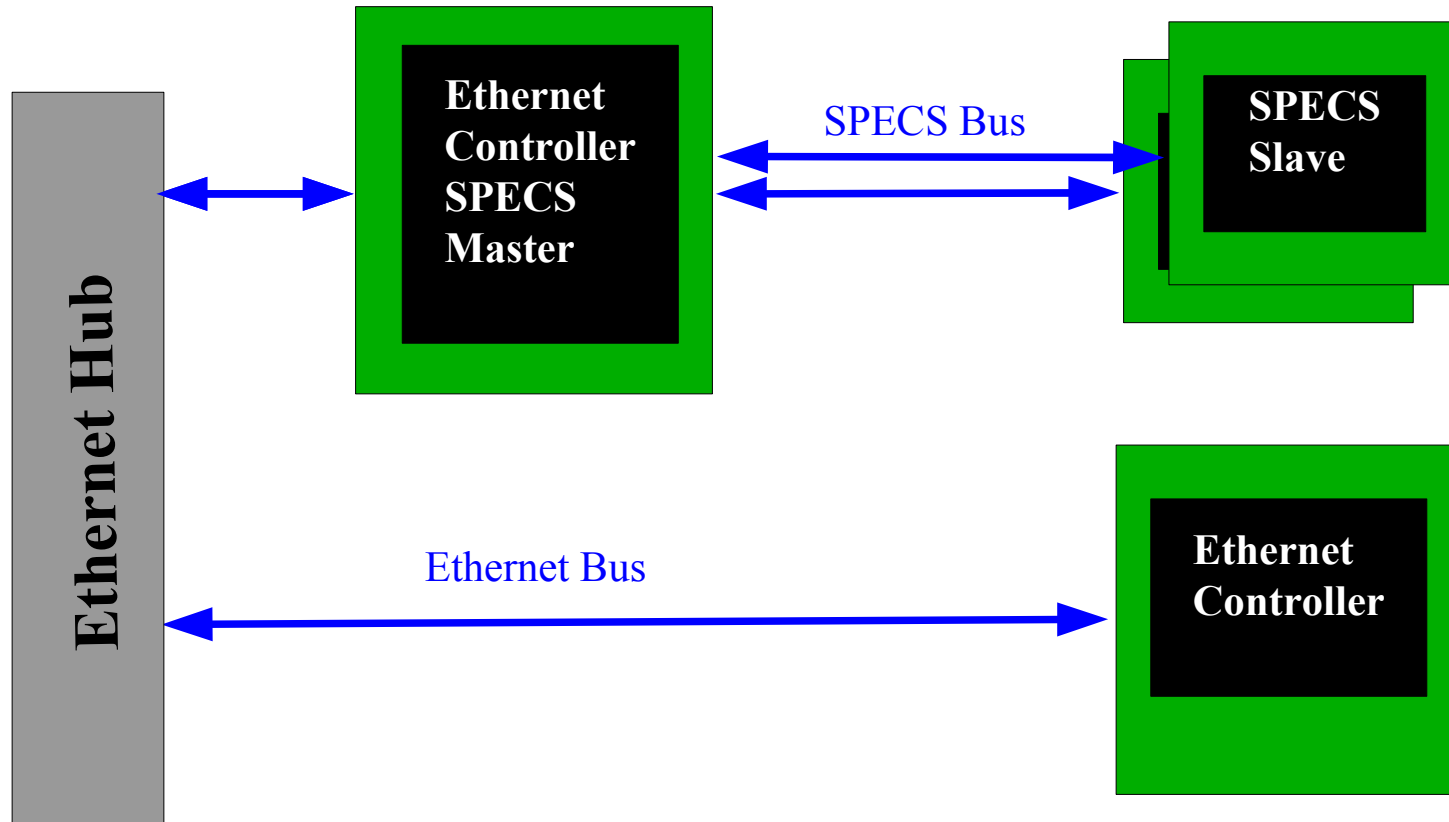
Dual Star BASIC INTERFACE & Dual-Dual Star FABRIC INTERFACE



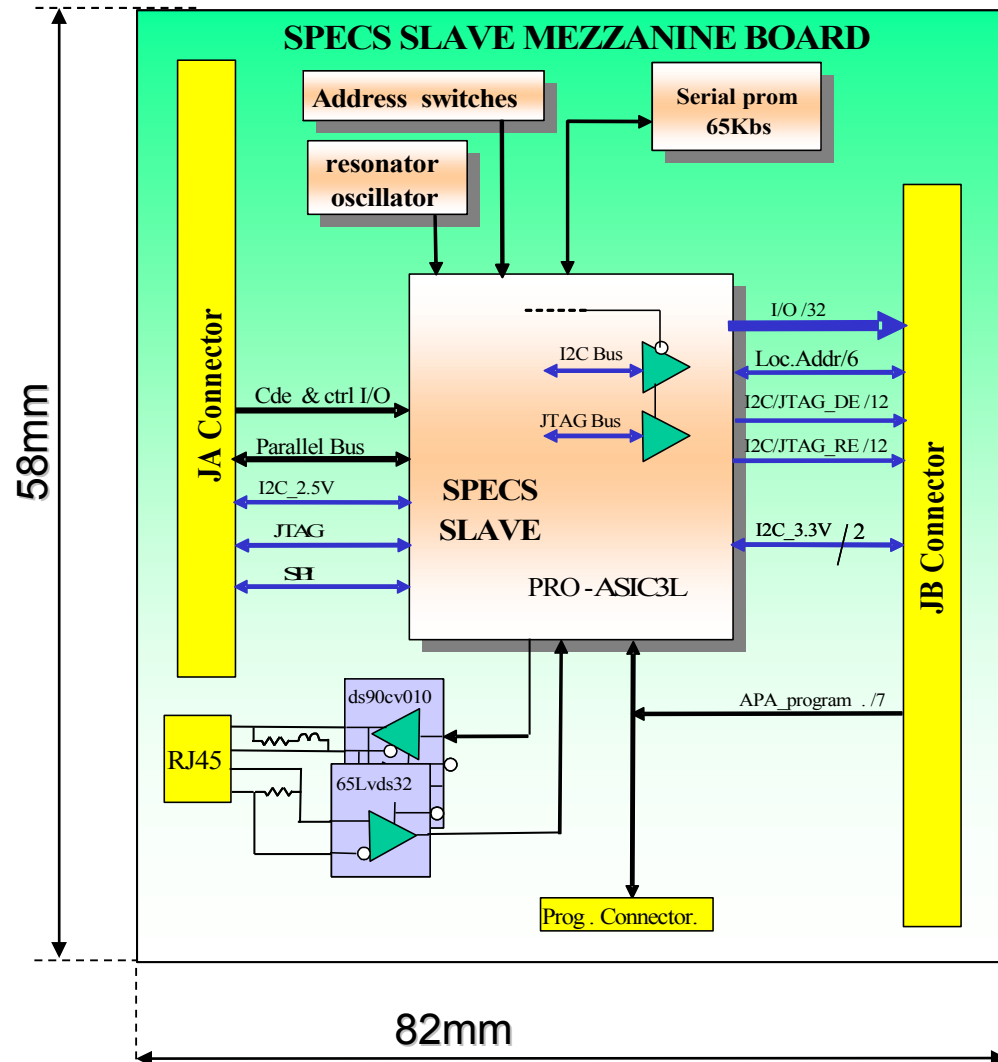
Kontron carrier board AT8404



SPECS system



SuperB SPECS slave implementation



FPGA ProASIC3L from ACTEL.
Triple voting register.

Transfert rate: 10Mbits/s

Address: Local address switch.
Broadcast address capability.

On board clock: Crystal resonator

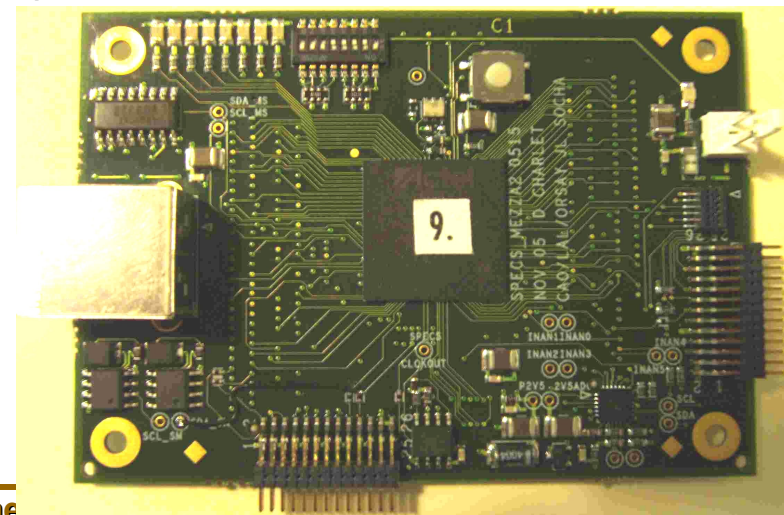
Programmable clock for SPECS readback:

Long distance capability: 120m cat6 cable

User Serial EEPROM: 65Kbits capacity

JTAG bus, I2C bus, SPI Bus

chip selects: Common to all serial busses.



Possible solution for off-detector area

Hardware

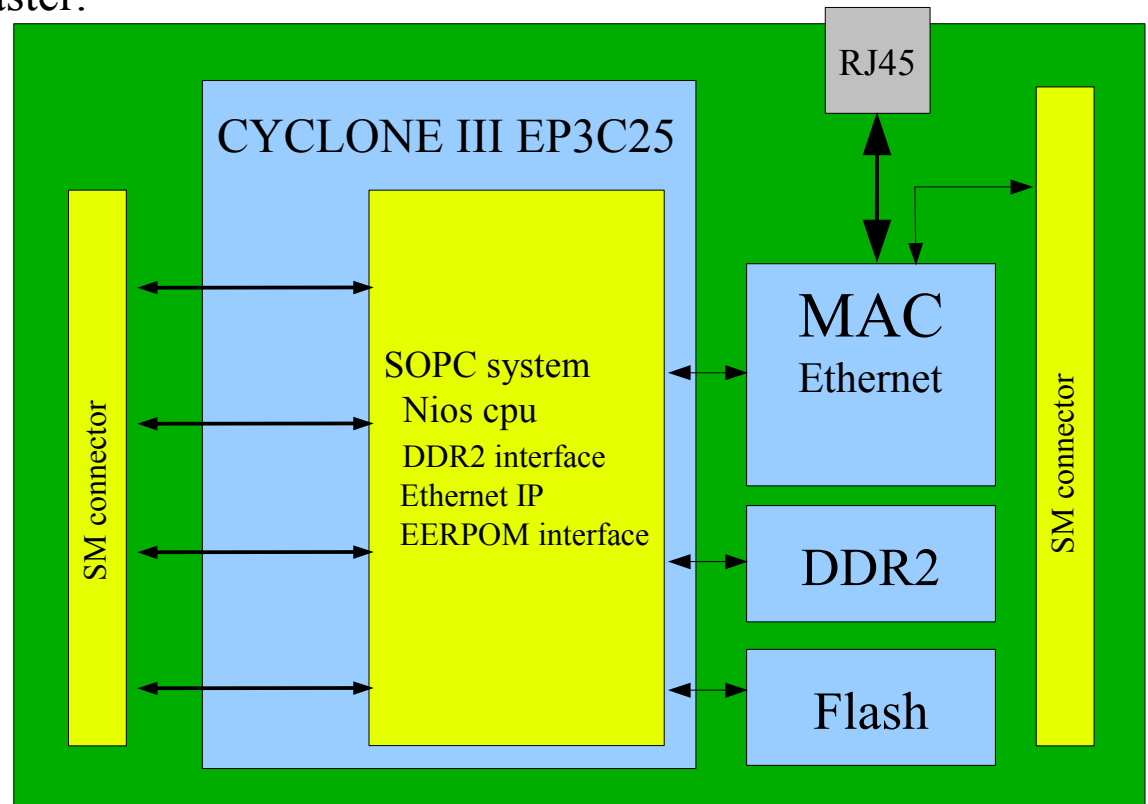
- Based on Ethernet SPECS master.
- SM connector.
 - Parallel bus,Configurable.
 - I/O ligne, I2C bus, SPI bus.
 - JTAG bus.
- 32MBytes DDR2 memory.
- 16MBytes Flash memory.

Firmware

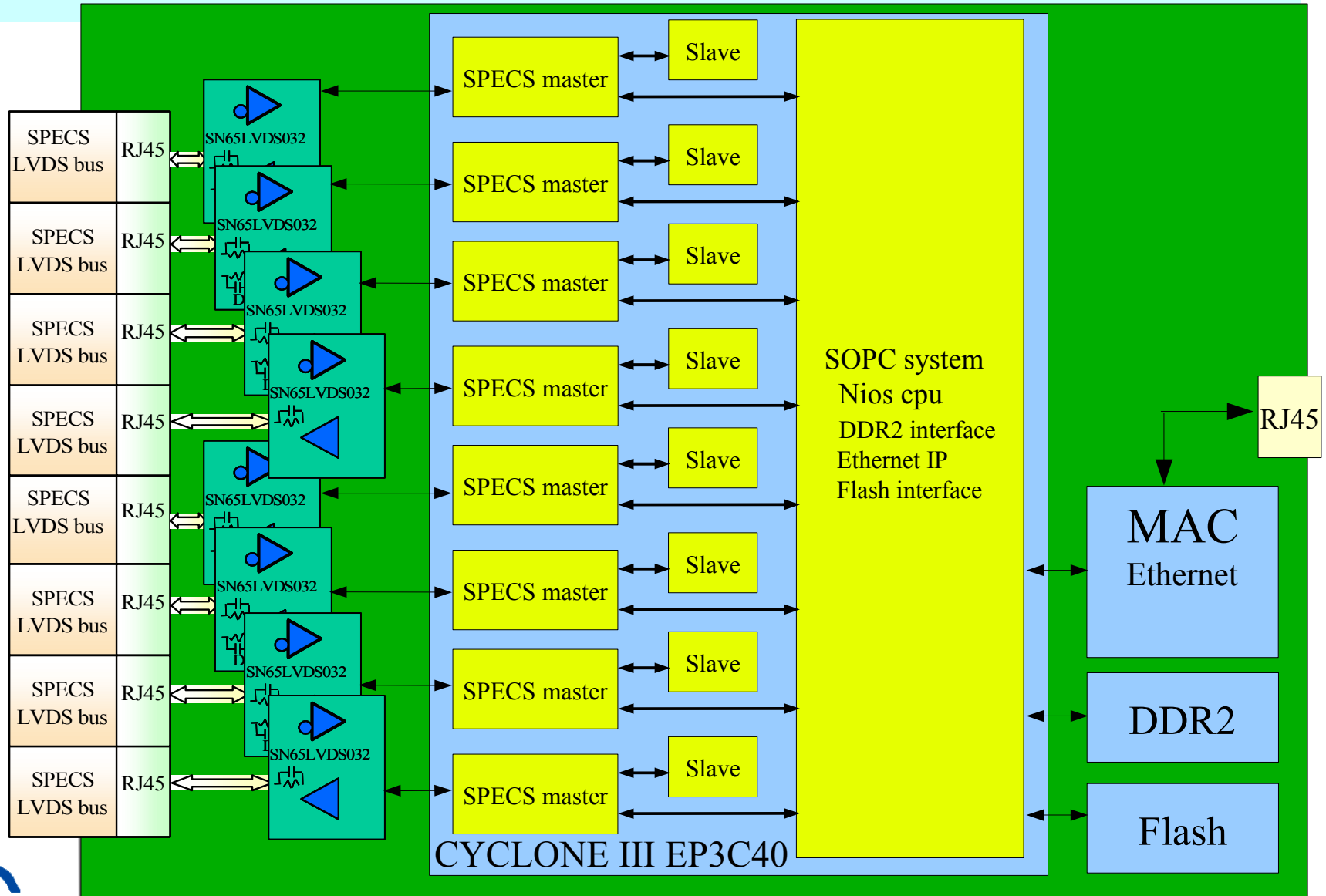
- Ethernet reconfiguration.
- Cyclone III EP3C25F324.
- Base on NIOS II processor.

Soft

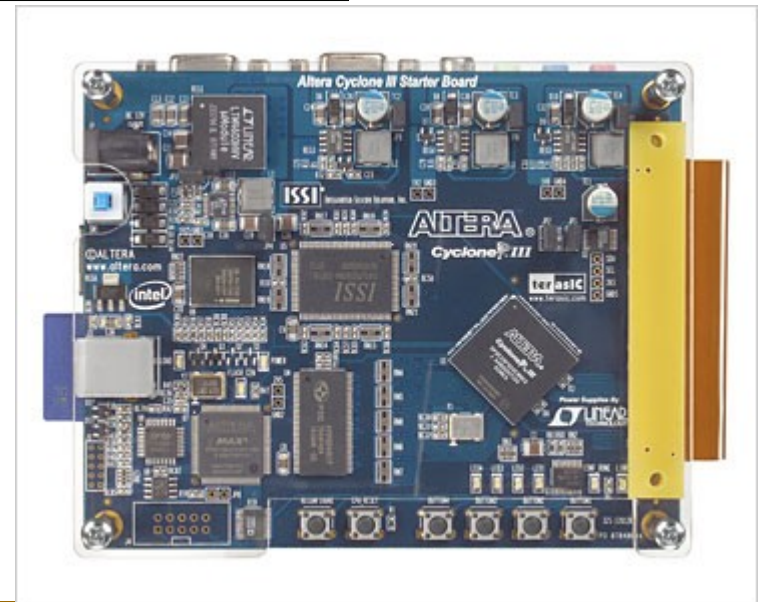
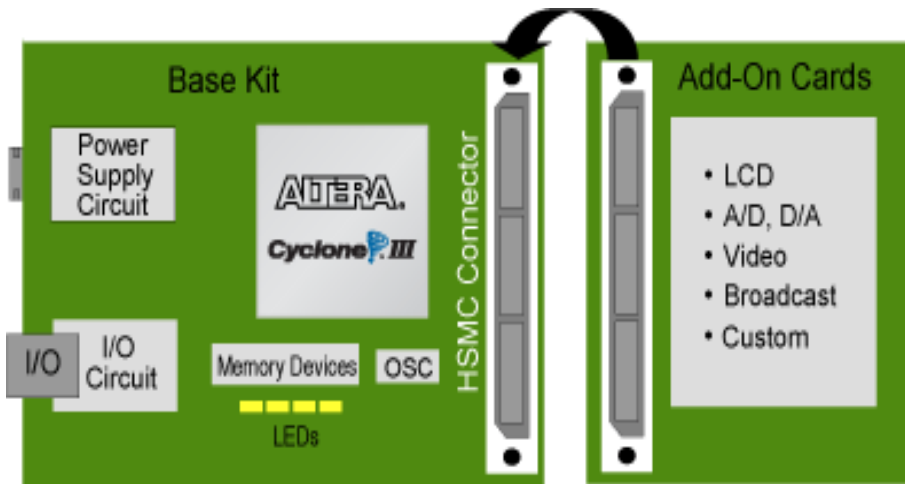
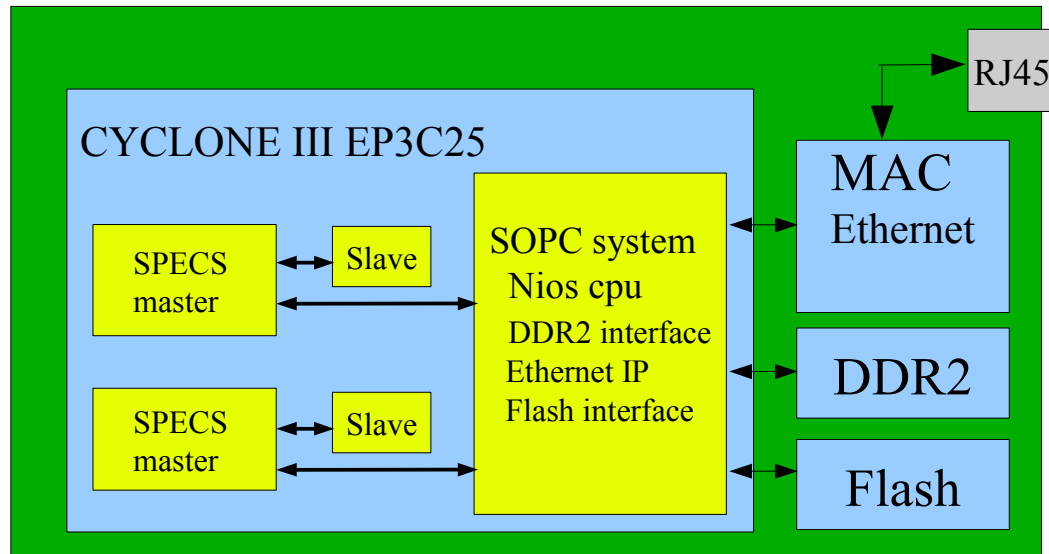
- OS μ clinux.
- DIM server.
- SPECS library.
- SPECS users library.



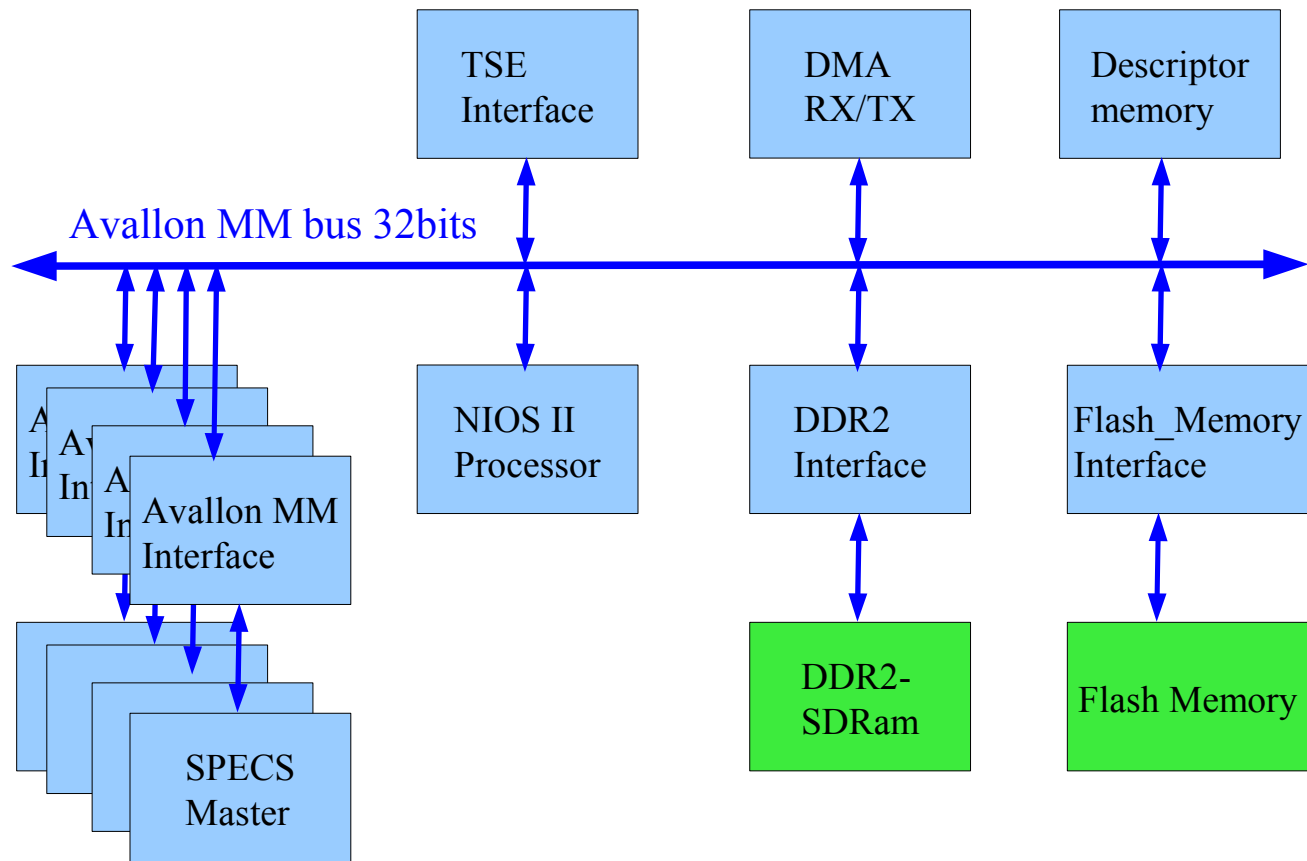
Ethernet SPECS master



Ethernet SPECS master status



SPECS master firmware



Conclusion

- We have different options for the FCTS system:
 - Full custom backplane and boards
 - Standard ATCA crate backplane and custom boards.
 - Fully standard ATCA system
- At this time, there is no strong argument againsts the adequate custom solution
 - This will of course be further studied
- Off-detector ECS board development.
 - Ethernet-based master is now running
 - Slave mezzanine is being studied